



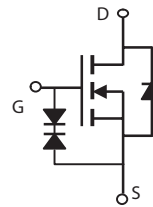
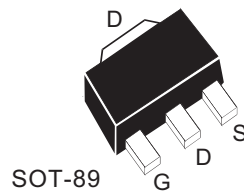
## N-Channel Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
40V	1.3A	390 @ V <sub>GS</sub> =10V
		550 @ V <sub>GS</sub> =4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	40	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>A</sub> =25°C	1.3
		T <sub>A</sub> =70°C	1.0
I <sub>DM</sub>	-Pulsed <sup>b</sup>	5.2	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	0.25	mJ
P <sub>D</sub>	Maximum Power Dissipation	T <sub>A</sub> =25°C	1.25
		T <sub>A</sub> =70°C	0.8
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	100	°C/W
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# STK400

Ver 1.0

## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±10	uA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	1.8	3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =0.65A		300	390	m ohm
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.55A		400	550	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =0.65A		1.4		S
<b>DYNAMIC CHARACTERISTICS <sup>c</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V f=1.0MHz		40		pF
C <sub>OSS</sub>	Output Capacitance			17.5		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			9.5		pF
<b>SWITCHING CHARACTERISTICS <sup>c</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =20V I <sub>D</sub> =0.65A V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		7.8		ns
t <sub>r</sub>	Rise Time			11.2		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			105		ns
t <sub>f</sub>	Fall Time			14		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =0.65A, V <sub>GS</sub> =10V		1.70		nC
		V <sub>DS</sub> =20V, I <sub>D</sub> =0.65A, V <sub>GS</sub> =4.5V		1.15		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =0.65A, V <sub>GS</sub> =10V		0.42		nC
Q <sub>gd</sub>	Gate-Drain Charge			0.61		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =0.7A		0.9	1.3	V
<b>Notes</b>						
a.Surface Mounted on FR4 Board, t ≤ 10sec.						
b.Pulse Test:Pulse Width ≤ 300us, Duty Cycle ≤ 2%.						
c.Guaranteed by design, not subject to production testing.						
d.Starting T <sub>J</sub> =25°C, L=0.5mH, V <sub>DD</sub> = 20V.(See Figure13)						

Jan,12,2011

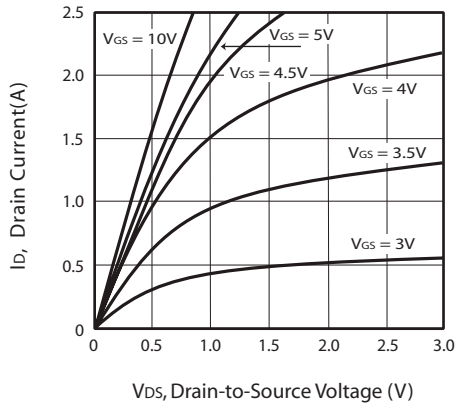


Figure 1. Output Characteristics

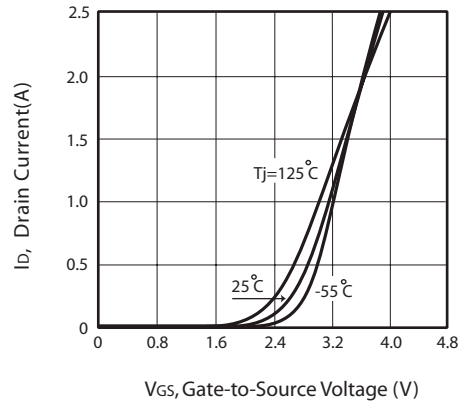


Figure 2. Transfer Characteristics

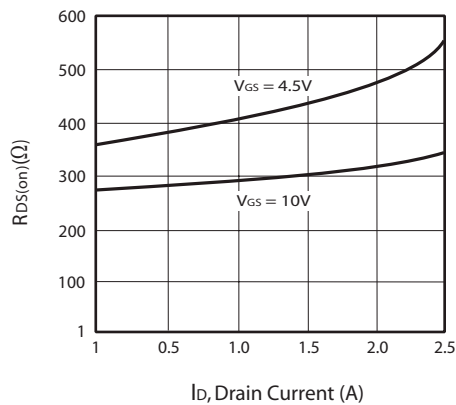


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

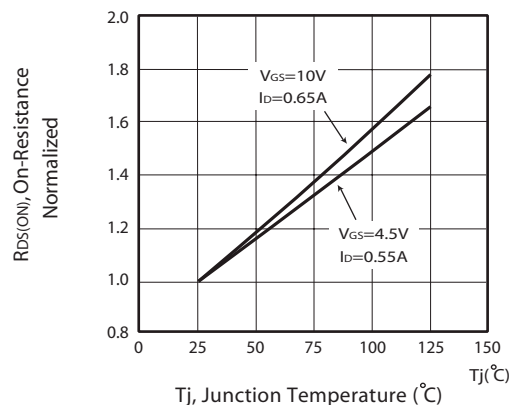


Figure 4. On-Resistance Variation with Drain Current and Temperature

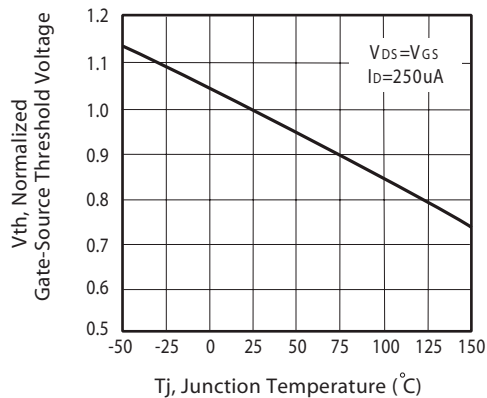


Figure 5. Gate Threshold Variation with Temperature

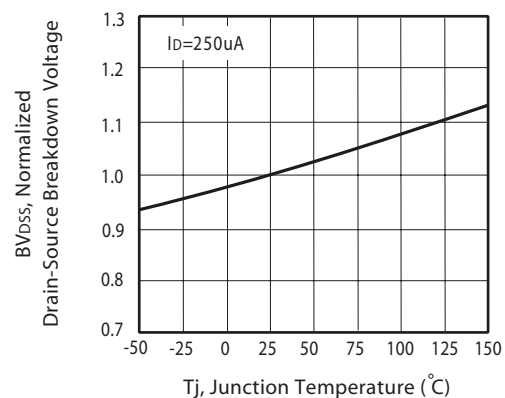


Figure 6. Breakdown Voltage Variation with Temperature

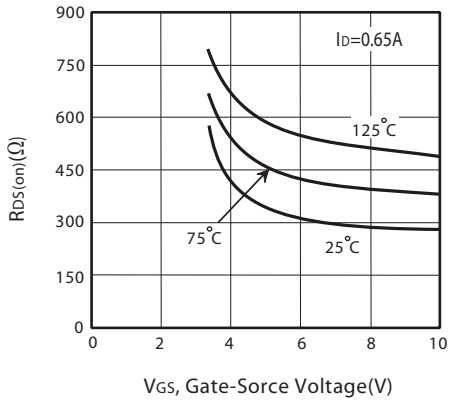


Figure 7. On-Resistance vs. Gate-Source Voltage

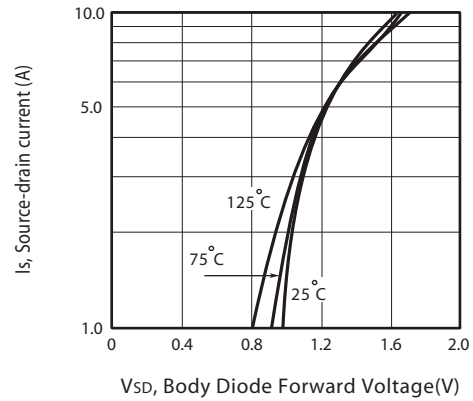


Figure 8. Body Diode Forward Voltage Variation with Source Current

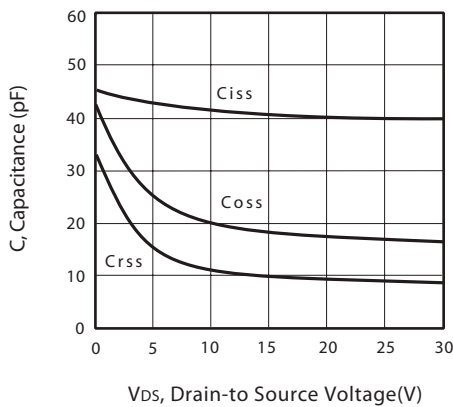


Figure 9. Capacitance

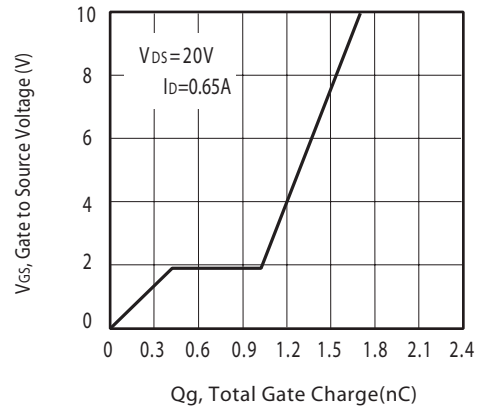


Figure 10. Gate Charge

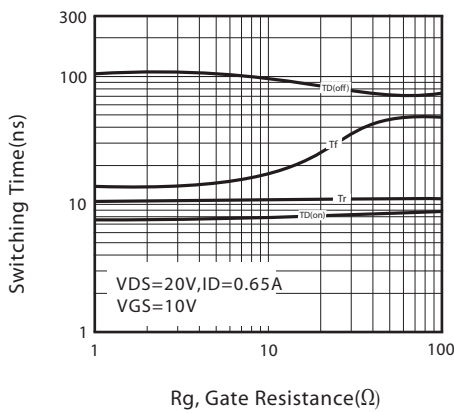


Figure 11. switching characteristics

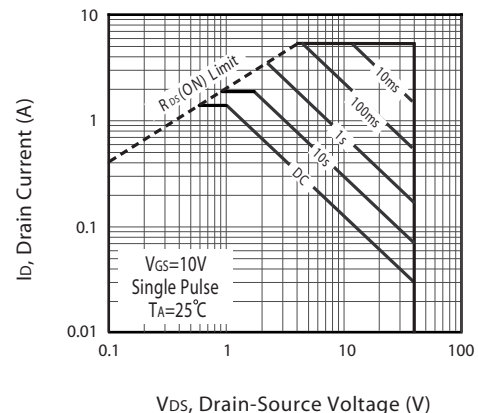
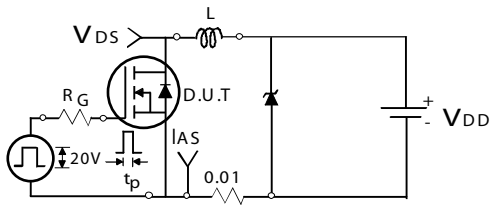
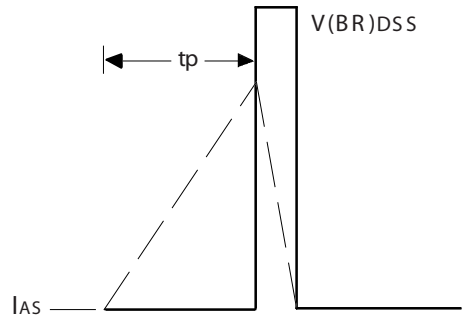


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

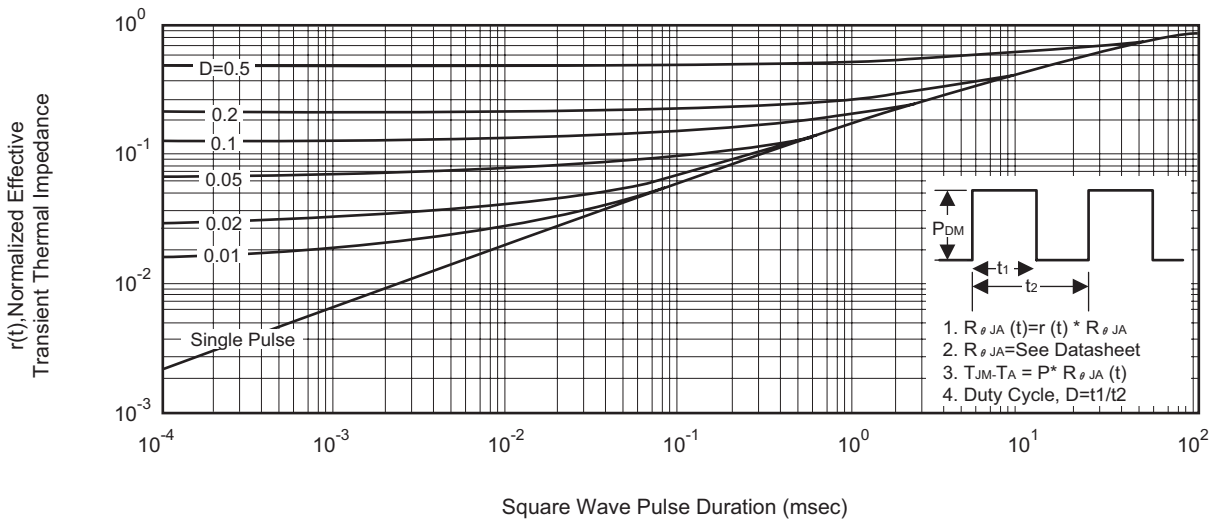
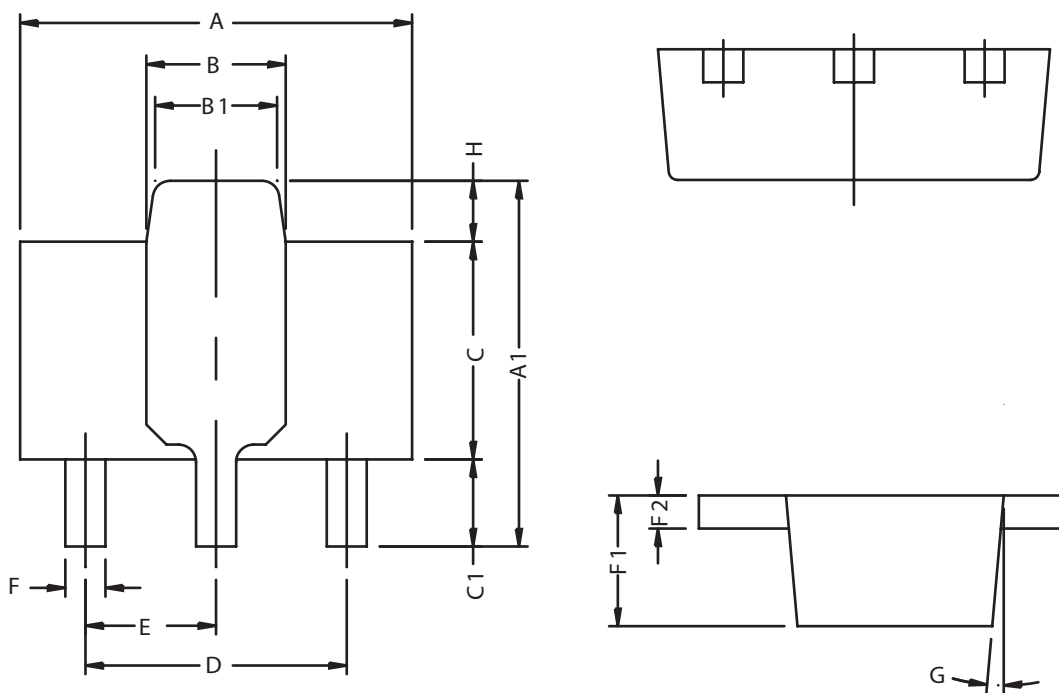


Figure 14. Normalized Thermal Transient Impedance Curve

## PACKAGE OUTLINE DIMENSIONS

### SOT-89



REF.	DIMENSIONS	
	Millimeters	
	MIN.	MAX.
A	4.40	4.60
A1	4.05	4.25
B	1.50	1.70
B1	1.30	1.50
C	2.40	2.60
C1	0.89	1.20
D	3.00 REF.	
E	1.50 REF.	
F	0.40	0.52
F1	1.40	1.60
F2	0.35	0.41
G	5° TYP.	
H	0.70 REF.	

