



## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

VDSS	ID	RDS(ON) ( $\Omega$ ) Typ
200V	1.4A	1.22 @ VGS=10V
		1.29 @ VGS=4.5V

### FEATURES

- Super high dense cell design for low  $R_{DS(ON)}$ .
- Rugged and reliable.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Limit	Units	
$V_{DS}$	Drain-Source Voltage	200	V	
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V	
$I_D$	Drain Current-Continuous <sup>a c</sup>	$T_A=25^\circ\text{C}$	1.4	A
		$T_A=70^\circ\text{C}$	1.1	A
$I_{DM}$	-Pulsed <sup>c</sup>	9	A	
$E_{AS}$	Single Pulse Avalanche Energy <sup>d</sup>	3.75	mJ	
$P_D$	Maximum Power Dissipation <sup>a</sup>	$T_A=25^\circ\text{C}$	3	W
		$T_A=70^\circ\text{C}$	1.9	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$	

### THERMAL CHARACTERISTICS

Symbol	Parameter	Limit	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	42	$^\circ\text{C/W}$

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## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>OFF CHARACTERISTICS</b>							
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	200			V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =160V , V <sub>GS</sub> =0V			1	uA	
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA	
<b>ON CHARACTERISTICS</b>							
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	1.8	3	V	
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =0.7A		1.22	1.53	ohm	
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =0.7A		1.29	1.74	ohm	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =0.7A		1.3		S	
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>							
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		245		pF	
C <sub>OSS</sub>	Output Capacitance				25		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance				13		pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>							
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =100V I <sub>D</sub> =0.7A V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		8.6		ns	
t <sub>r</sub>	Rise Time			8.8		ns	
t <sub>D(OFF)</sub>	Turn-Off Delay Time			15		ns	
t <sub>f</sub>	Fall Time			3.5		ns	
Q <sub>g</sub>	Total Gate Charge		V <sub>DS</sub> =100V, I <sub>D</sub> =0.7A, V <sub>GS</sub> =10V		3.9		nC
		V <sub>DS</sub> =100V, I <sub>D</sub> =0.7A, V <sub>GS</sub> =4.5V		2.4		nC	
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =100V, I <sub>D</sub> =0.7A,		0.9		nC	
Q <sub>gd</sub>	Gate-Drain Charge	V <sub>GS</sub> =10V		1.3		nC	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>							
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =1A		0.83	1.2	V	

### Notes

- Surface Mounted on FR4 Board of 1 inch<sup>2</sup> , 1oz.
- Guaranteed by design, not subject to production testing.
- Drain current limited by maximum junction temperature.
- Starting T<sub>J</sub>=25°C, L=0.3mH, V<sub>DD</sub> = 50V.(See Figure13)

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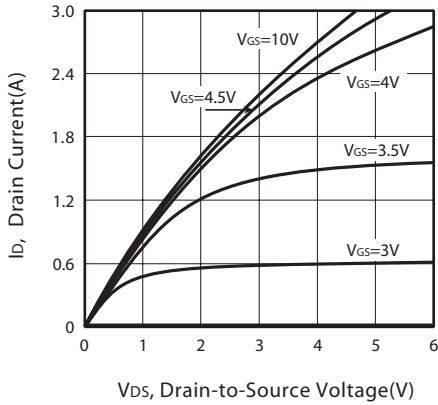


Figure 1. Output Characteristics

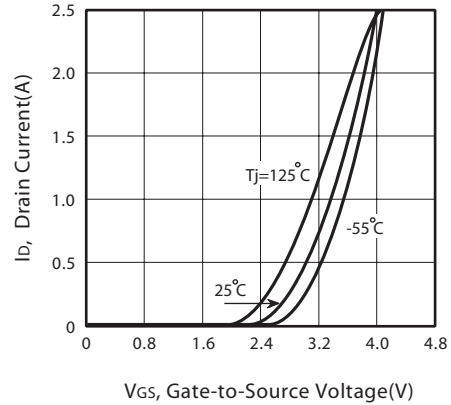


Figure 2. Transfer Characteristics

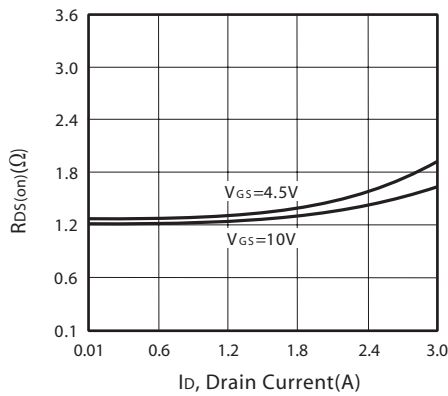


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

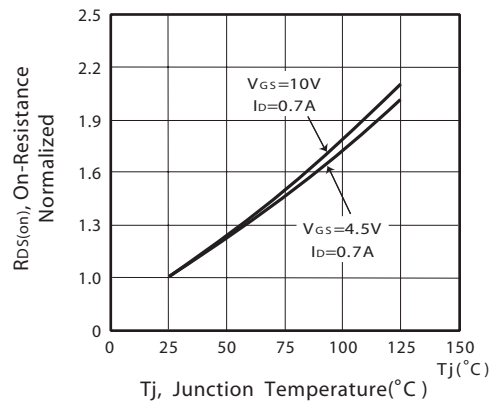


Figure 4. On-Resistance Variation with Drain Current and Temperature

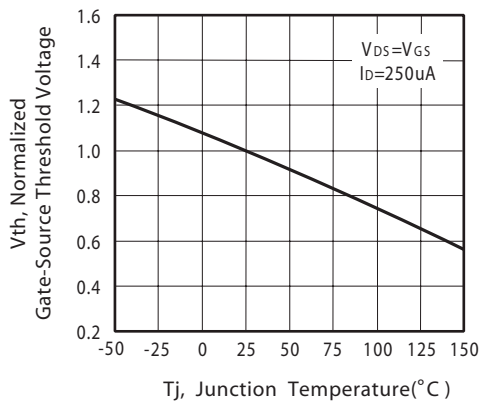


Figure 5. Gate Threshold Variation with Temperature

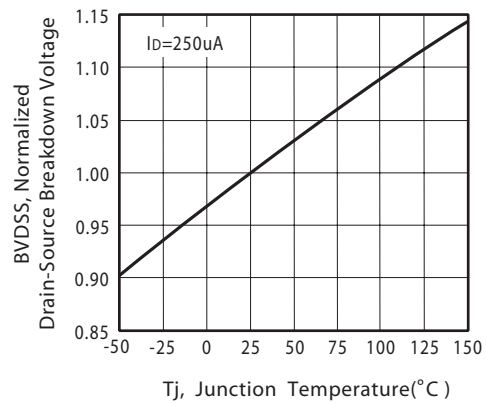


Figure 6. Breakdown Voltage Variation with Temperature

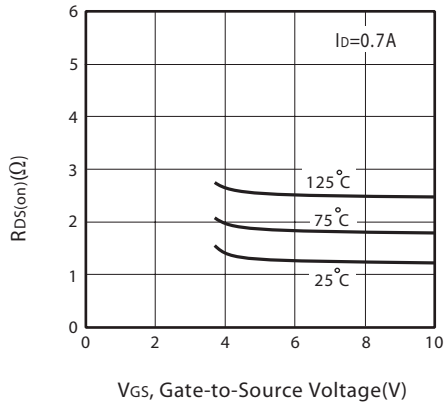


Figure 7. On-Resistance vs. Gate-Source Voltage

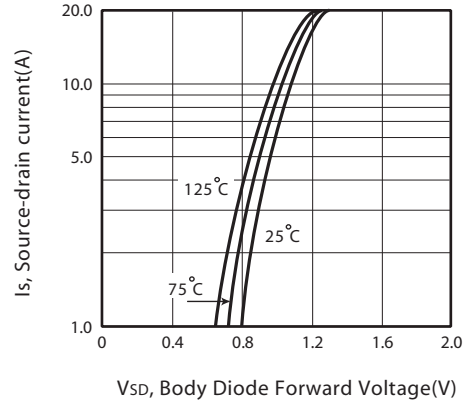


Figure 8. Body Diode Forward Voltage Variation with Source Current

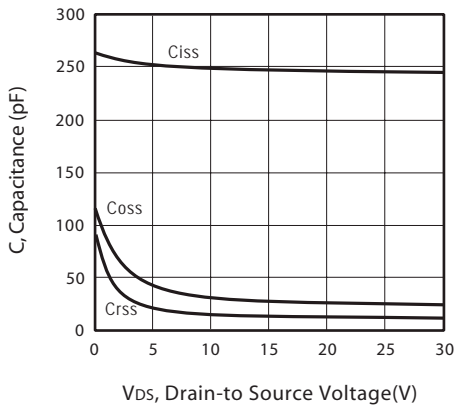


Figure 9. Capacitance

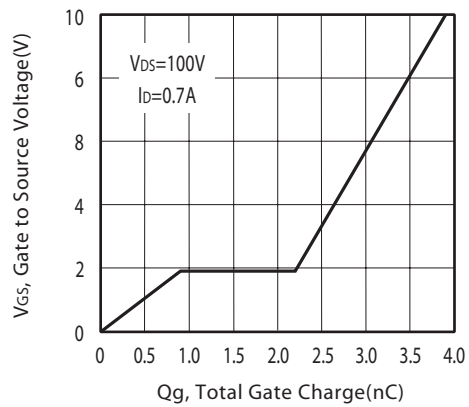


Figure 10. Gate Charge

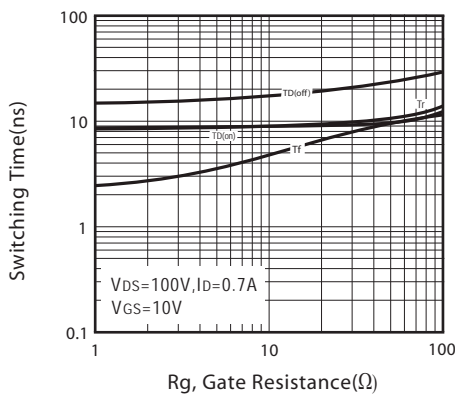


Figure 11. switching characteristics

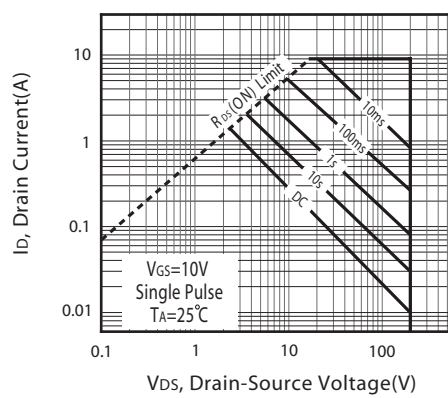
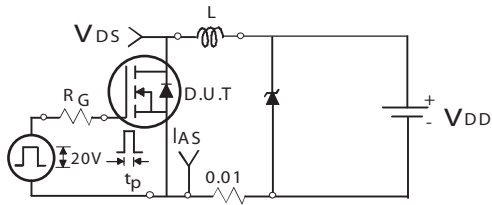
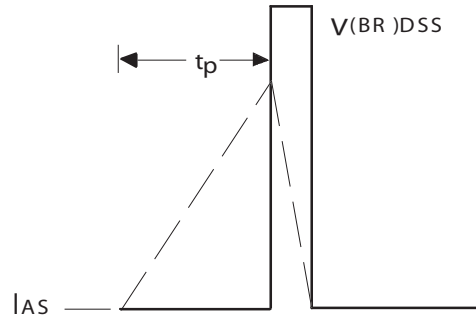


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

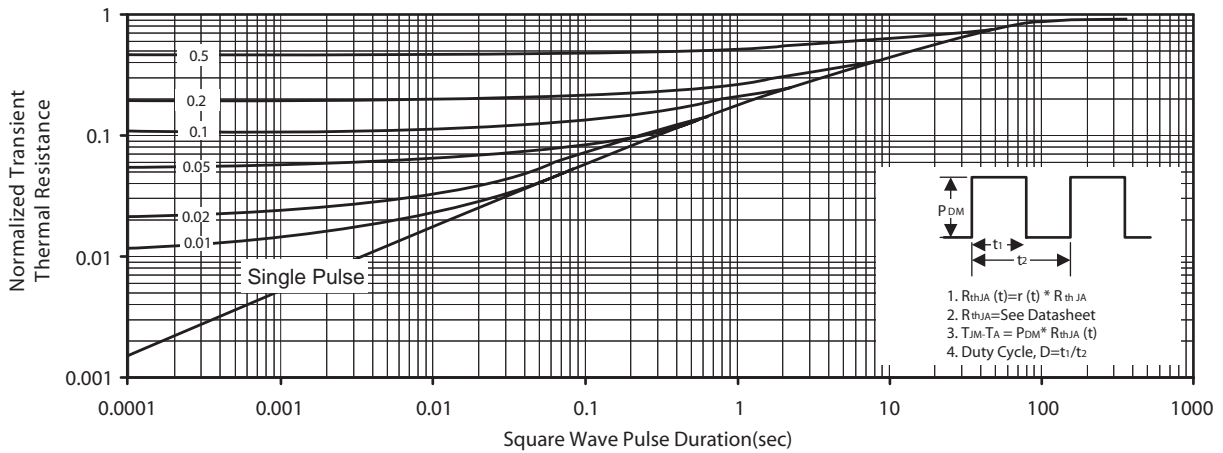
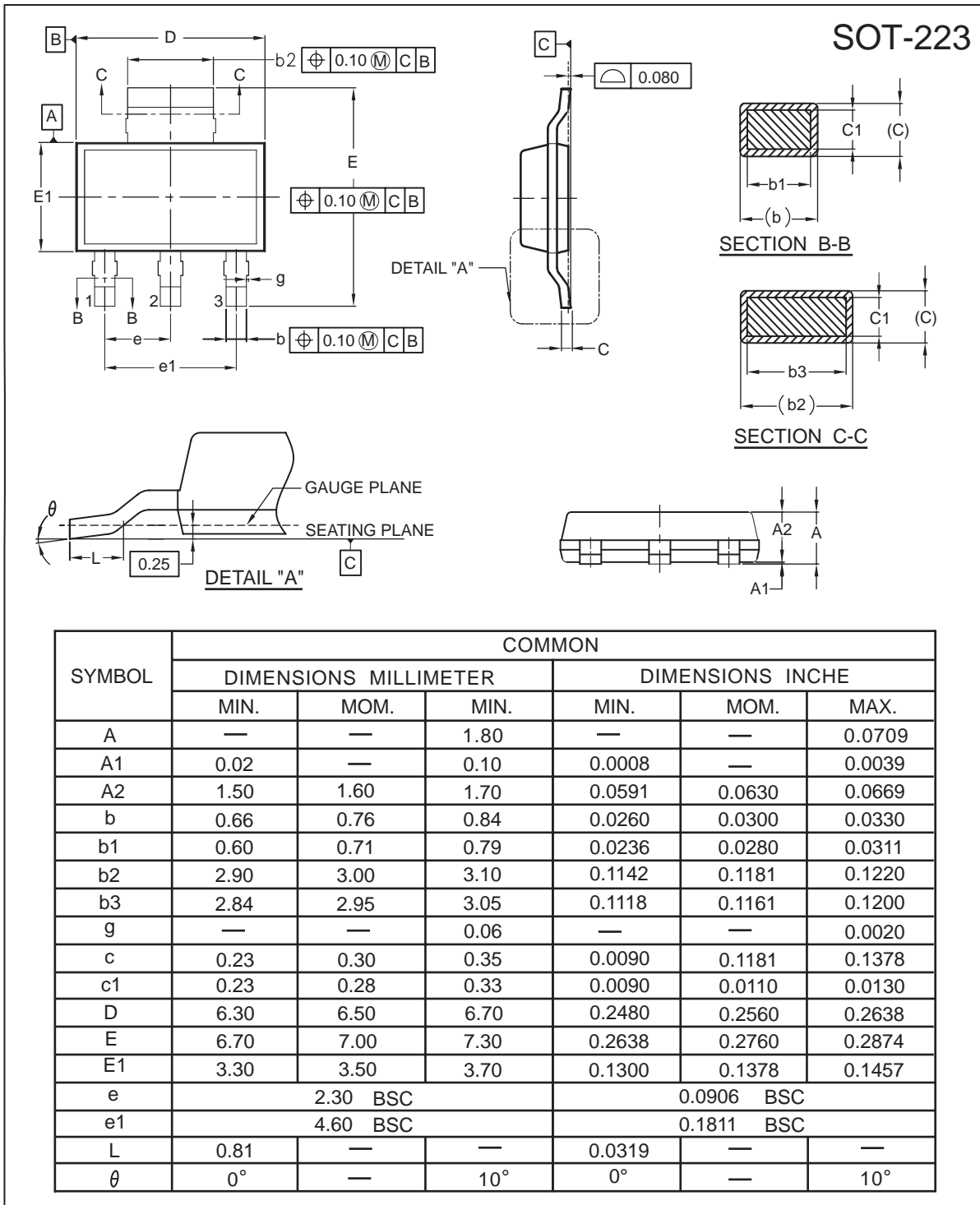


Figure 14. Normalized Thermal Transient Impedance Curve

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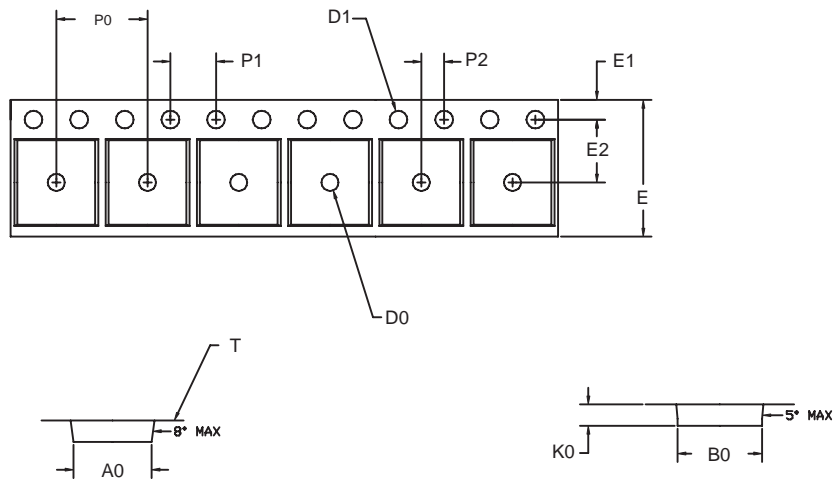
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## SOT-223 Tape and Reel Data

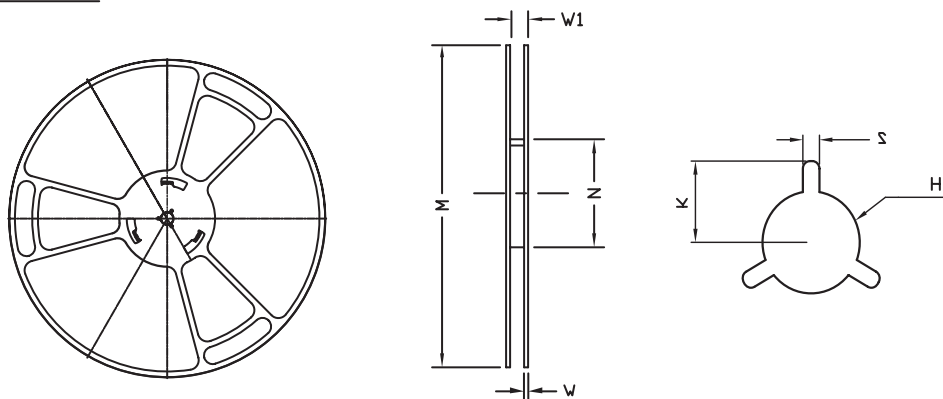
### SOT-223 Carrier Tape



unit:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
---	6.83 ±0.1	7.42 ±0.1	1.88 ±0.1	1.50 +0.25	1.60 +0.1	12.0 +0.3 -0.1	1.75 ±0.1	5.50 ±0.5	8.0 ±0.1	4.00 ±0.1	2.00 ±0.05	0.292 ±0.02

### SOT-223 Reel



UNIT:mm

REEL SIZE	M	N	W	W1	H	K	S	G	R	V
φ 330 ± 0.5	---	φ 97.0 ± 1.0	2.2	13.0 + 1.5	φ 13.0 + 0.5 - 0.2	10.6	2.0 ± 0.5	---	---	---

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## TOP MARKING DEFINITION

