



## N-Channel Logic Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

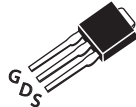
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
40V	47A	9 @ V <sub>GS</sub> =10V
		11 @ V <sub>GS</sub> =4.5V

### FEATURES

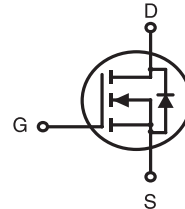
- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- TO-252 and TO251 Package.



STU SERIES  
TO-252AA(D-PAK)



STD SERIES  
TO-251(I-PAK)



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	40	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	47
		T <sub>C</sub> =70°C	38
I <sub>DM</sub>	-Pulsed <sup>b</sup>	138	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	169	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> =25°C	42
		T <sub>C</sub> =70°C	27
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case <sup>a</sup>	3	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	50	°C/W

# STU/D438A

Ver 1.0

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	1.6	3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =24A		7	9	m ohm
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =21A		8.5	11	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =24A		70		S
<b>DYNAMIC CHARACTERISTICS <sup>c</sup></b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V f=1.0MHz		1460		pF
C <sub>oss</sub>	Output Capacitance			245		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			175		pF
<b>SWITCHING CHARACTERISTICS <sup>c</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =20V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> =6 ohm		24		ns
t <sub>r</sub>	Rise Time			30		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			67		ns
t <sub>f</sub>	Fall Time			25		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =24A, V <sub>GS</sub> =10V		25		nC
		V <sub>DS</sub> =20V, I <sub>D</sub> =24A, V <sub>GS</sub> =4.5V		12.5		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =24A,		2.5		nC
Q <sub>gd</sub>	Gate-Drain Charge	V <sub>GS</sub> =10V		7		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS <sup>c</sup></b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =20A		0.8	1.3	V

### Notes

- Surface Mounted on FR4 Board, t ≤ 10sec.
- Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.
- Starting T<sub>J</sub>=25°C, L=0.5mH, V<sub>DD</sub> = 20V. (See Figure13)

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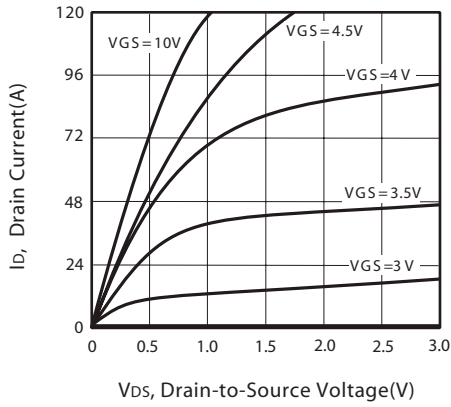


Figure 1. Output Characteristics

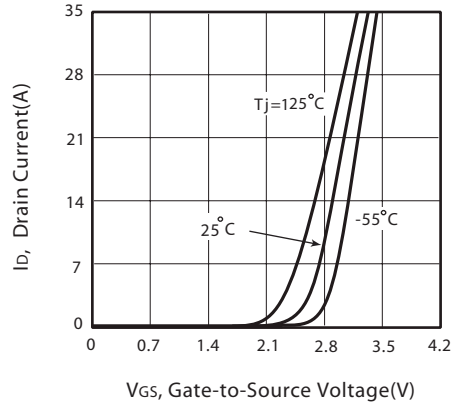


Figure 2. Transfer Characteristics

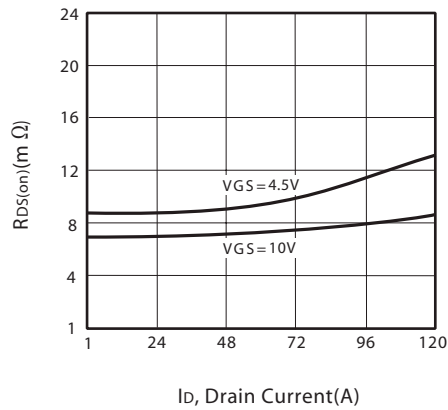


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

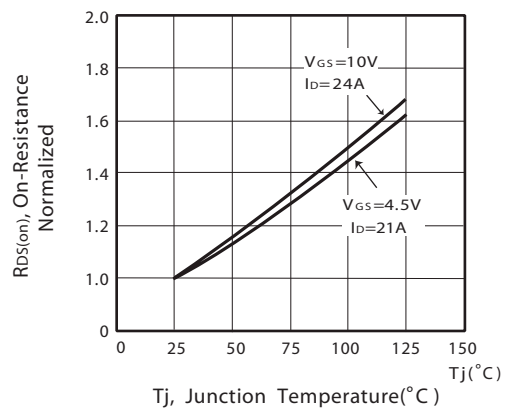


Figure 4. On-Resistance Variation with Drain Current and Temperature

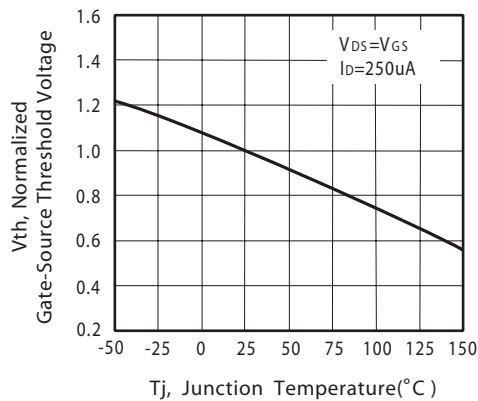


Figure 5. Gate Threshold Variation with Temperature

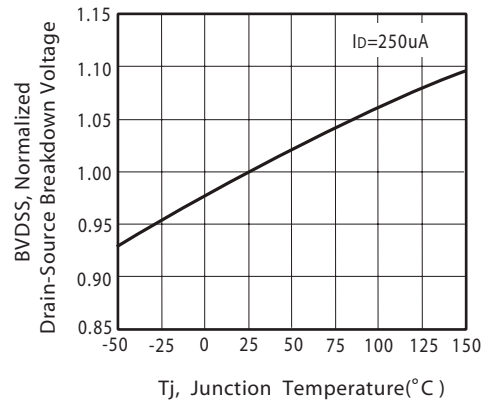


Figure 6. Breakdown Voltage Variation with Temperature

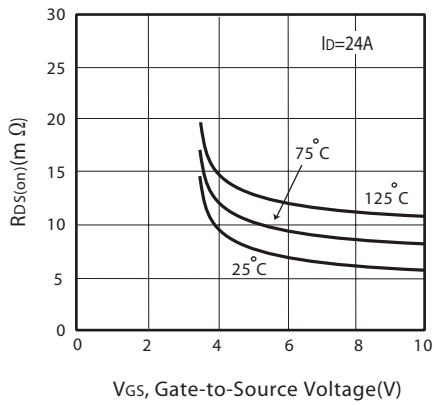


Figure 7. On-Resistance vs. Gate-Source Voltage

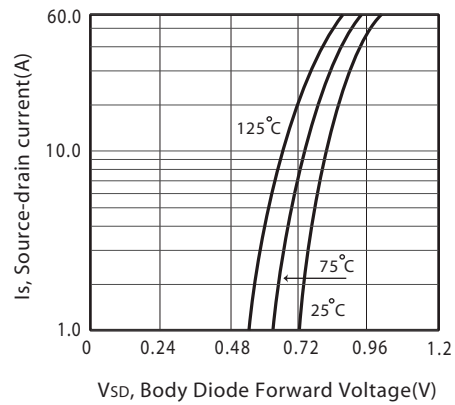


Figure 8. Body Diode Forward Voltage Variation with Source Current

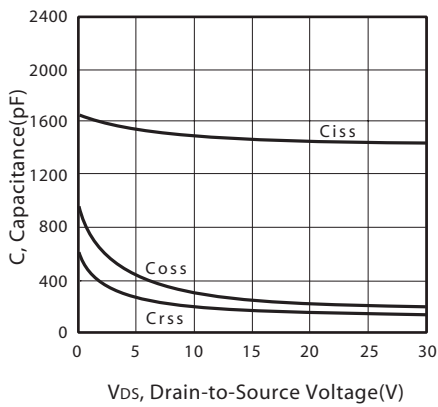


Figure 9. Capacitance

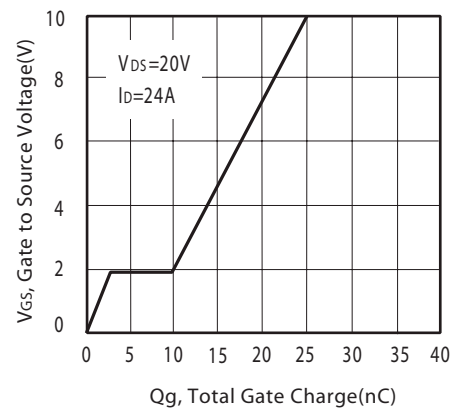


Figure 10. Gate Charge

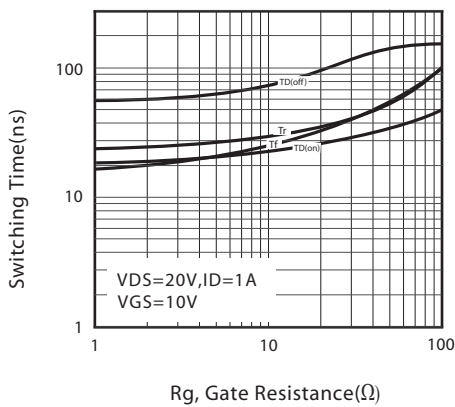


Figure 11. switching characteristics

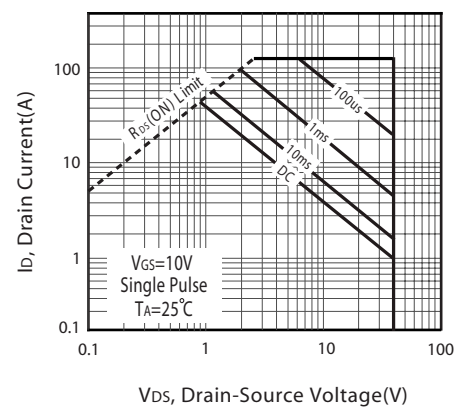
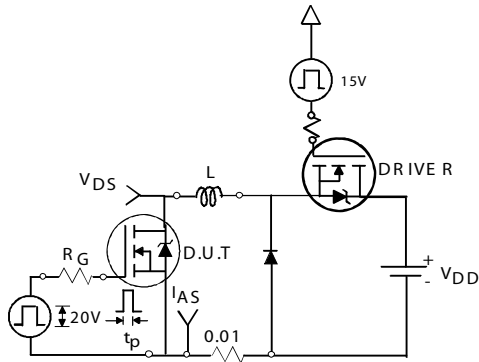
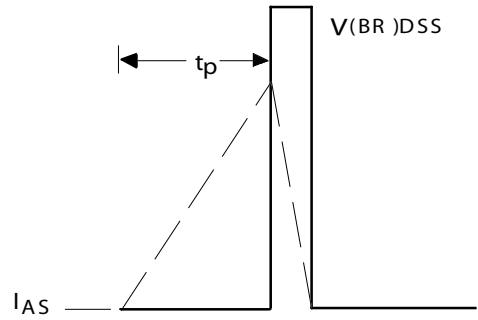


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

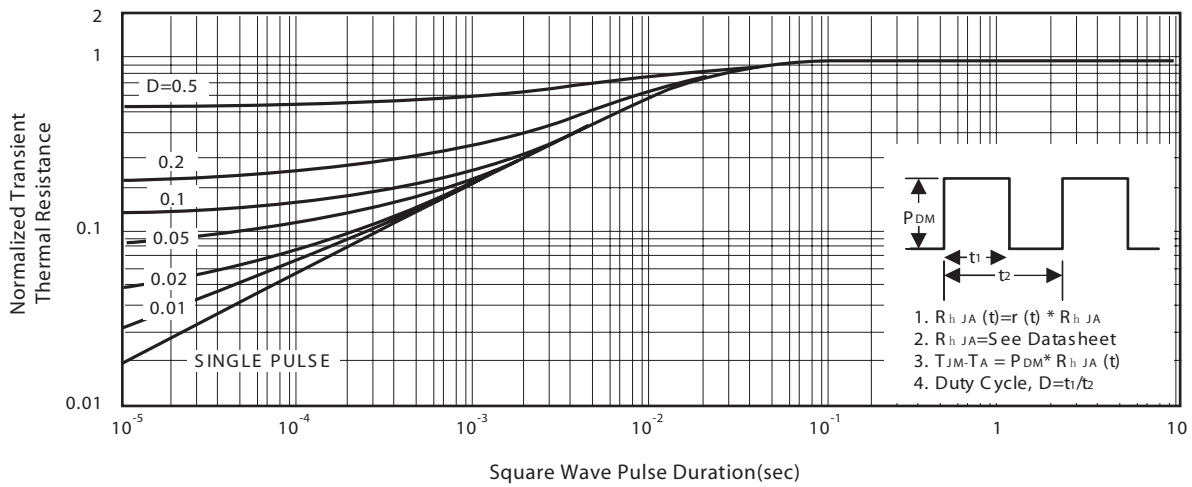
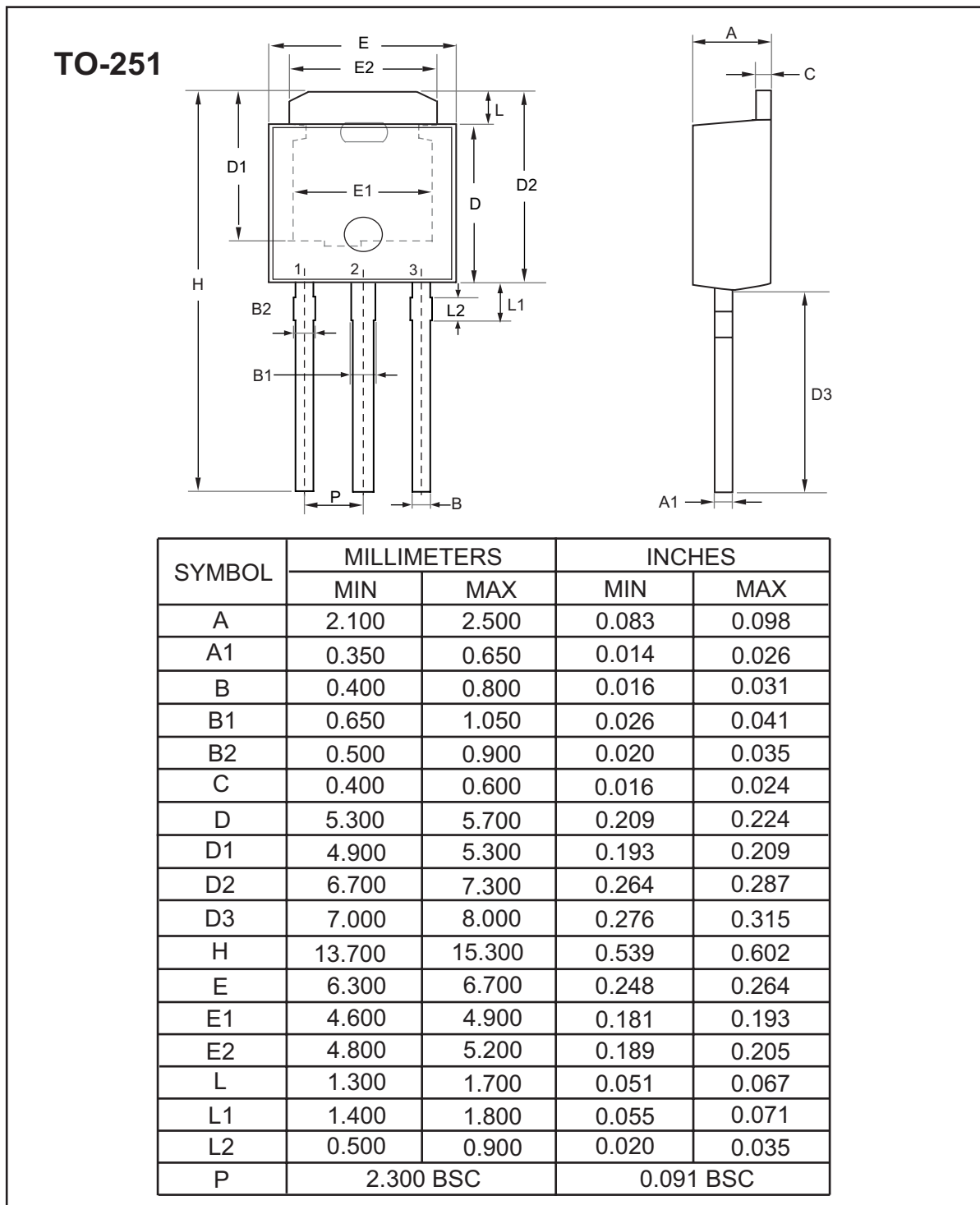


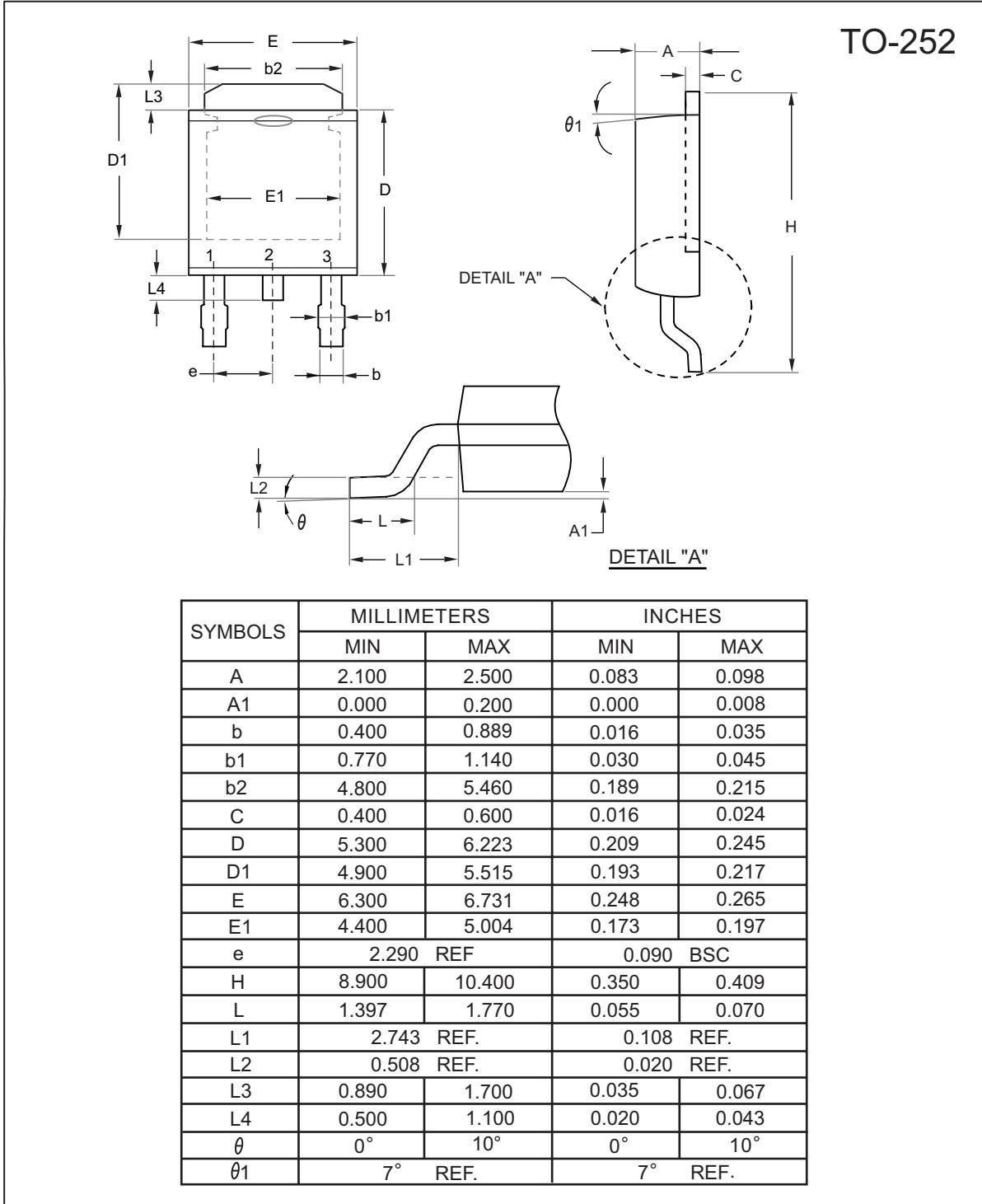
Figure 14. Normalized Thermal Transient Impedance Curve

## PACKAGE OUTLINE DIMENSIONS



# STU/D438A

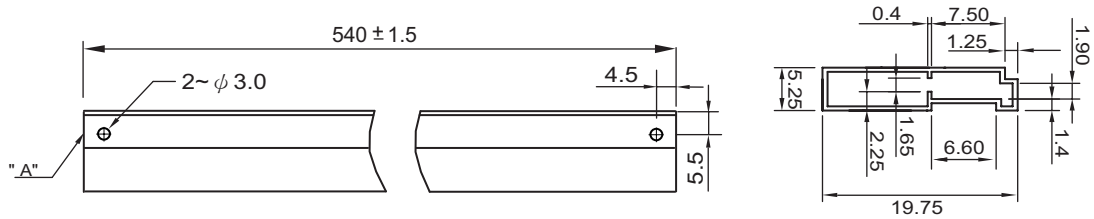
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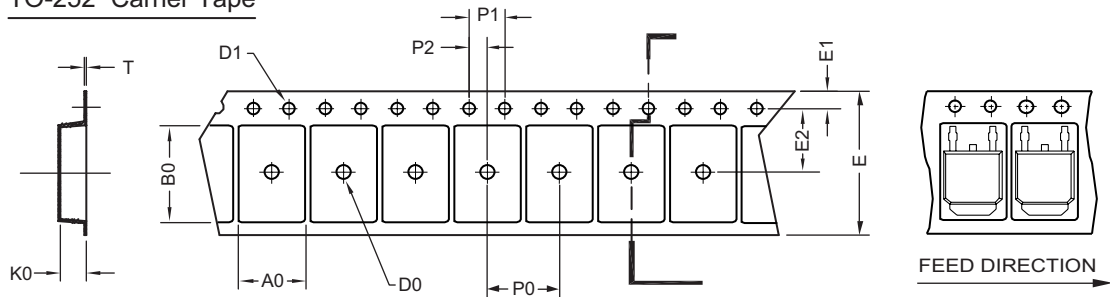
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## TO-251 Tube/TO-252 Tape and Reel Data

### TO-251 Tube



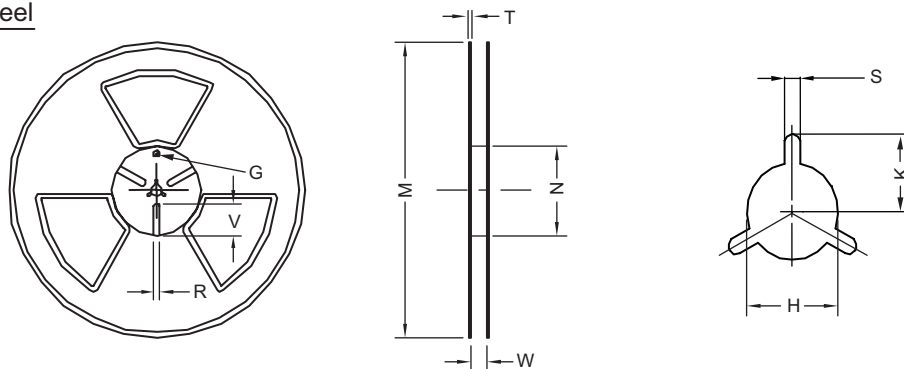
### TO-252 Carrier Tape



UNIT:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO-252 (16 mm)	6.96 ±0.1	10.49 ±0.1	2.79 ±0.1	φ 2	φ 1.5 + 0.1 - 0	16.0 ±0.3	1.75 ±0.1	7.5 ±0.15	8.0 ±0.1	4.0 ±0.1	2.0 ±0.15	0.3 ±0.05

### TO-252 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W	T	H	K	S	G	R	V
16 mm	φ 330	φ 330 ± 0.5	φ 97 ± 1.0	17.0 + 1.5 - 0	2.2	φ 13.0 + 0.5 - 0.2	10.6	2.0 ±0.5	---	---	---