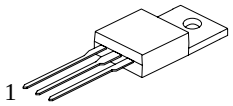
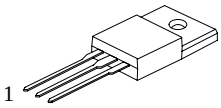
19.4A, 200V, 0.18Ω , N-CHANNEL POWER MOSFET

P :



TO-220

F :



TO-220F

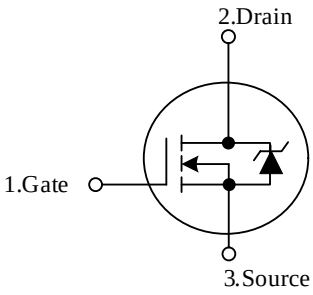
■ DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

■ FEATURES

* 19.4A, 200V, Low $R_{DS(ON)}$ (0.18Ω)
* Single Pulse Avalanche Energy Rated
* Rugged - SOA is Power Dissipation Limited
* Fast Switching Speeds
* Linear Transfer Characteristics
* High Input Impedance

■ SYMBOL



■ ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
FTK640P	TO-220	G	D	S	Tube
FTK640F	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

MOSFET

■ ABSOLUTE MAXIMUM RATINGS (T_C = 25˚C, unless otherwise specified)

PARAMET		SYMBOL	RATINGS	UNIT
Drain-Source Voltage (T_J = 25˚C ~ 125˚C)		V_{DS}	200	V
Drain to Gate Voltage (R_{GS} = 20kΩ, T_J = 25˚C ~ 125˚C)		V_{DGR}	200	V
Gate to Source Voltage		I_{GS}	±30	V
Drain Current	Continuous	I_D	19.4	A
	T_A = 100°C	I_D	12.3	A
	Pulsed	I_{DM}	77	A
Maximum Power Dissipation (T_c = 25°C) (FTK640P / FTK640F)		P_D	125 / 40	W
Derating factor			1.0 / 0.32	W/˚C
Single Pulse Avalanche Energy Rating (V_{DD} = 50V, starting T_J = 25˚C, L = 3.3mH, R_G=25Ω, I_{AS} = 19.4A)		E_{AS}	580	mJ
Operating Temperature Range		T_J	-40 ~ +150	˚C
Storage Temperature Range		T_{STG}	-40 ~ +150	˚C

Note: 1. Signified recommend operating range that indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits.
2. Absolute maximum ratings indicate limits beyond which damage to the device may occur.

■ ELECTRICAL SPECIFICATIONS (T_C = 25˚C , unless Otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 16)	200			V
Gate to Threshold Voltage	$V_{GS(THR)}$	V_{GS} = V_{DS}, I_D = 250μA	2.2		4.0	V
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ X $R_{DS(ON)MAX}$, V_{GS} = 10V	18			A
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V			1	μA
		V_{DS} =0.8xRated BV_{DSS},V_{GS}=0V, T_J=125˚C			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V			±100	nA
Drain to Source On Resistance (Note 1)	$R_{DS(ON)}$	I_D = 9.7A, V_{GS} = 10V		0.15	0.18	Ω
Forward Transconductance (Note 1)	g_{FS}	V_{DS} > 10V, I_D = 11A	6.7	10		S
Turn-On Delay Time	$t_{DLY(ON)}$	V_{DD} = 100V, I_D ≈ 19.4A, R_{GS} = 25Ω,		20	50	ns
Rise Time	t_R			190	390	ns
Turn-Off Delay Time	$t_{DLY(OFF)}$			55	120	ns
Fall Time	t_F			80	170	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10V, I_D = 19.4A, V_{DS} = 0.8 X Rated BV_{DSS}		31	40	nC
Gate to Source Charge	Q_{GS}			8.6		nC
Gate to Drain “Miller” Charge	Q_{GD}			13.5		nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V,f = 1.0MHz		1220	1600	pF
Output Capacitance	C_{OSS}			220	290	pF
Reverse - Transfer Capacitance	C_{RSS}			30	40	pF

Note: 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.
3. Gate Charge is Essentially Independent of Operating Temperature.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient (FTK640P)	θ_{JA}	62	˚C / W
Thermal Resistance Junction-Case (FTK640P)	θ_{Jc}	1.0	

■ SOURCE TO DRAIN DIODE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage (Note 1)	V_{SD}	I_{SD} = 19.4A, V_{GS} = 0V			1.5	V
Continuous Source to Drain Current	I_{SD}	Note 2			19.4	A
Pulse Source to Drain Current	I_{SDM}	Note 2			77.7	A
Reverse Recovery Time	t_{RR}	I_{SD} = 19.4A,		140		ns
Reverse Recovery Charge	Q_{RR}	dI_{SD}/dt =100 A/μs		0.69		μC

Note:

1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.

Typical Performance Curves Unless Otherwise Specified

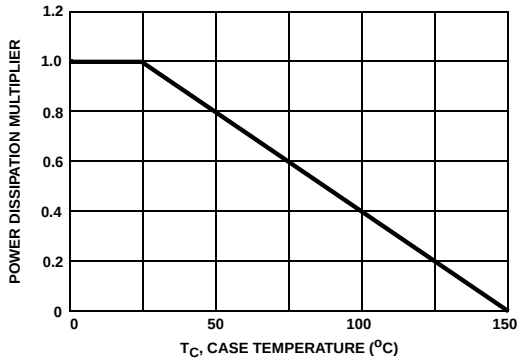


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

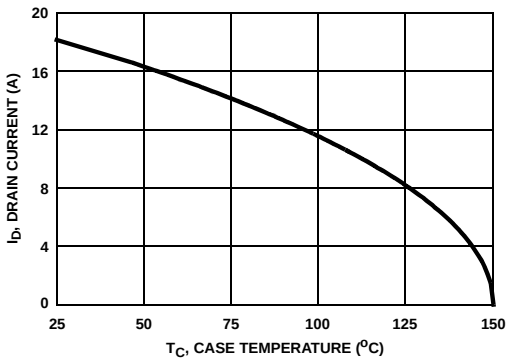


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

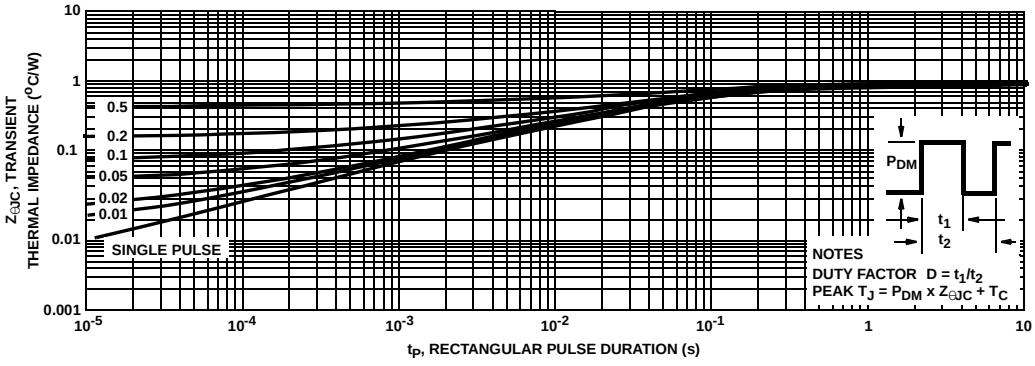


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

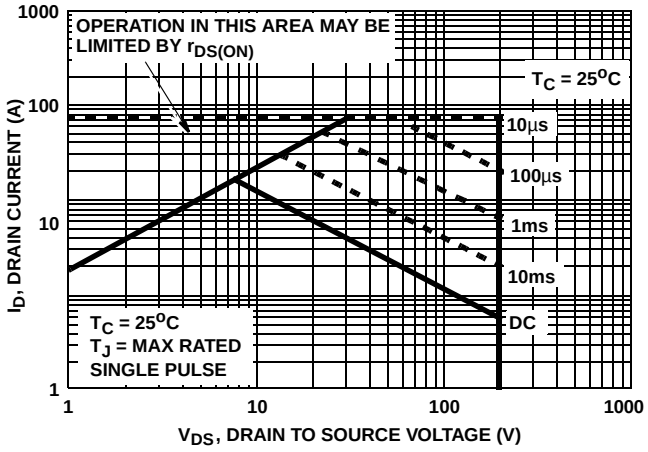


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

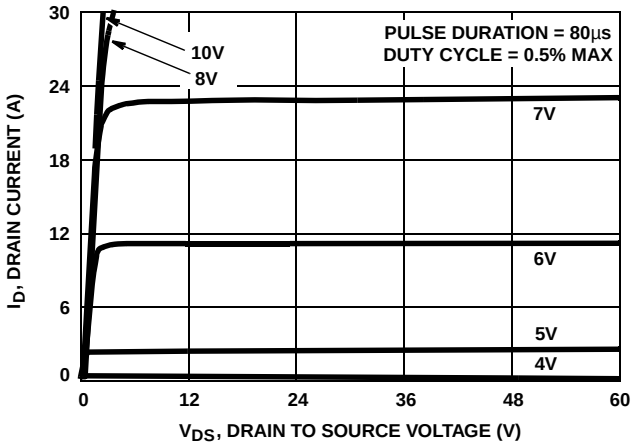


FIGURE 5. OUTPUT CHARACTERISTICS

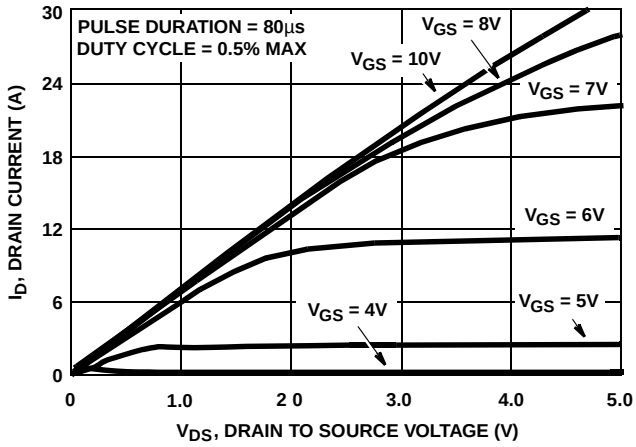


FIGURE 6. SATURATION CHARACTERISTICS

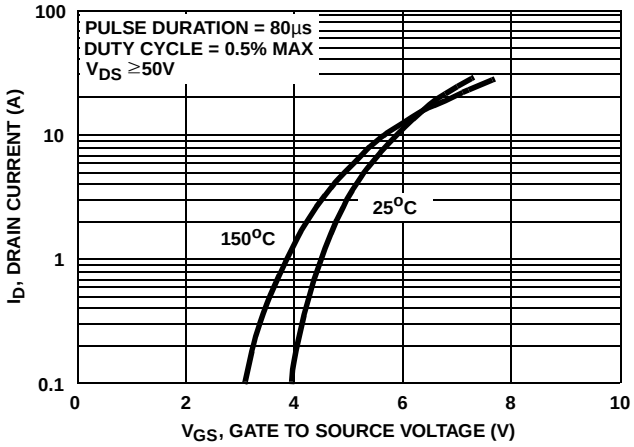


FIGURE 7. TRANSFER CHARACTERISTICS

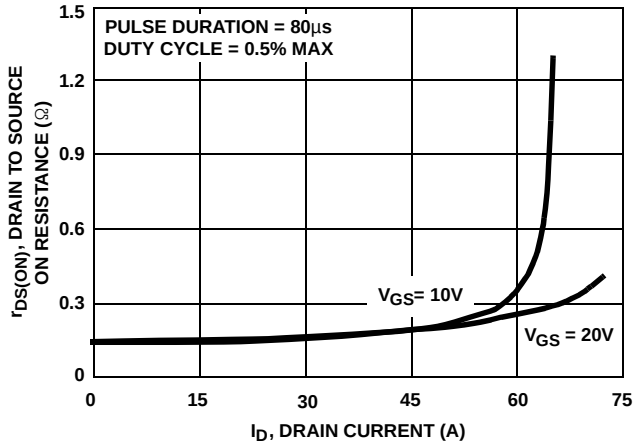


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

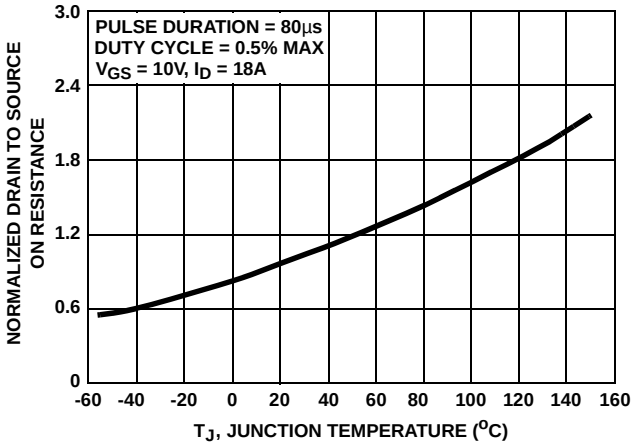


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

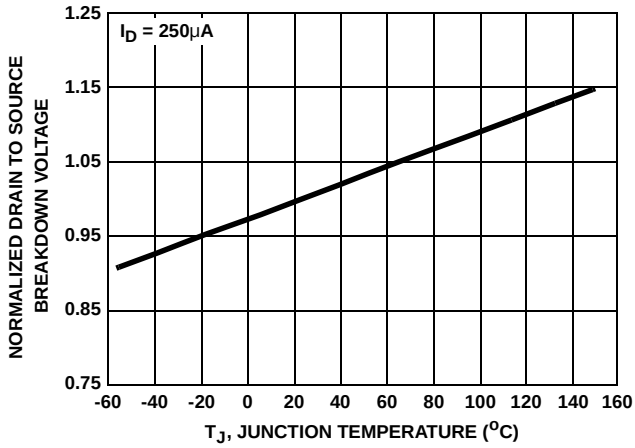


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

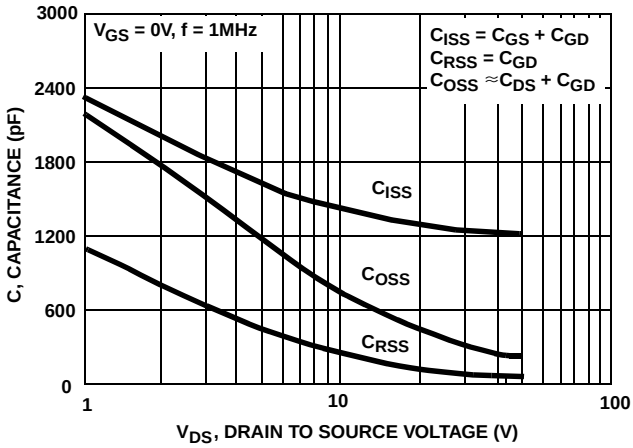


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

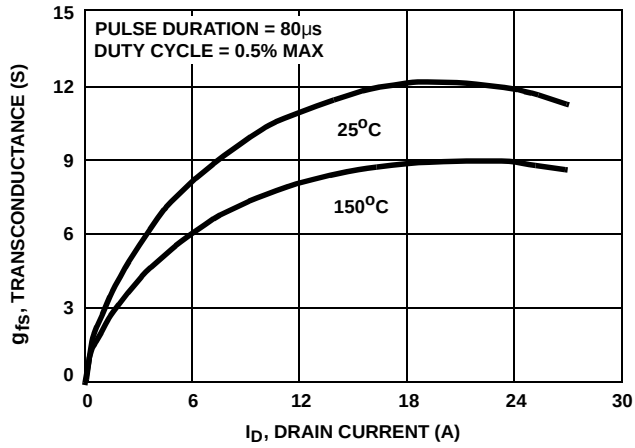


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

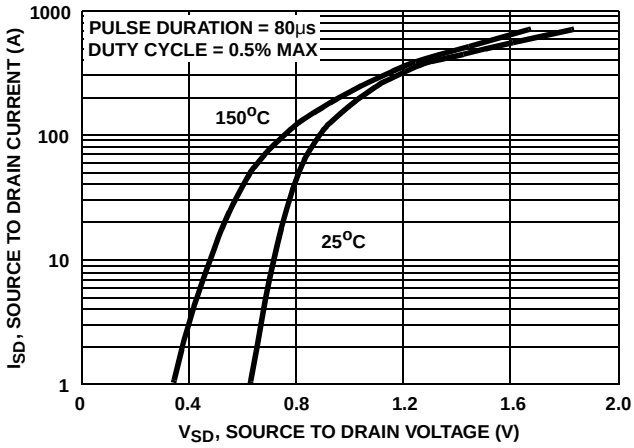


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

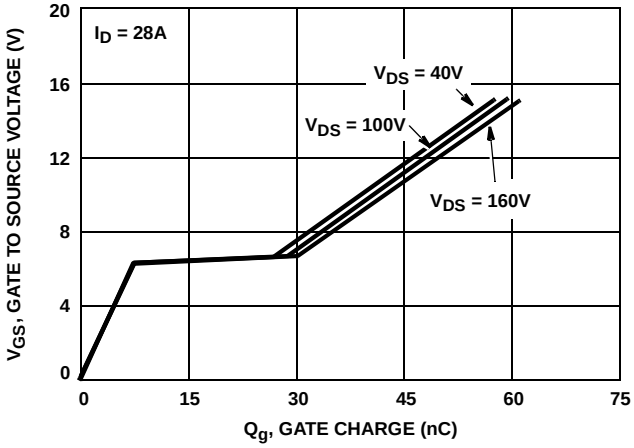


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

■ TEST CIRCUITS AND WAVEFORMS

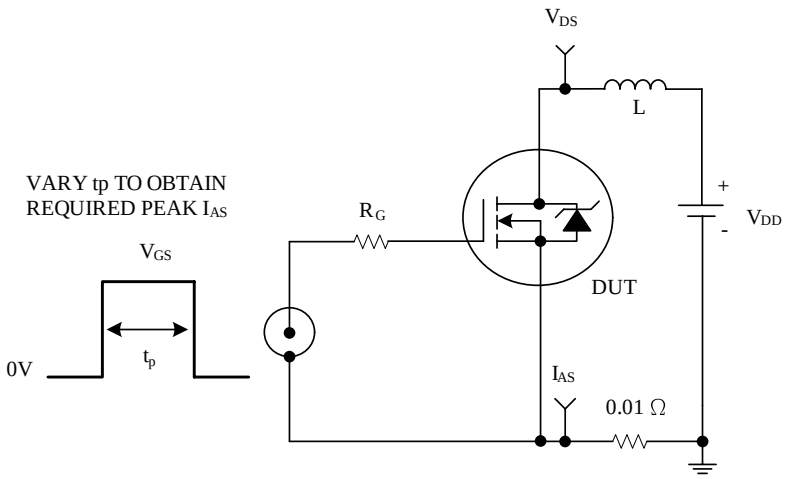


FIGURE 1. UNCLAMPED ENERGY TEST CIRCUIT

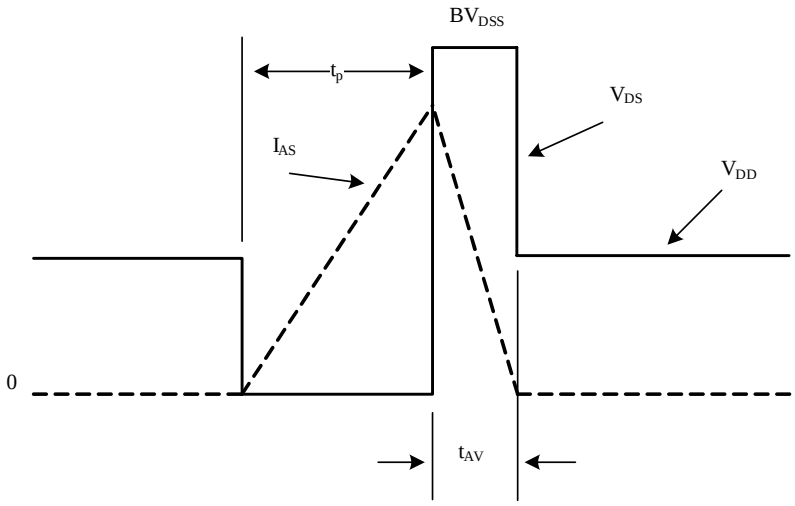


FIGURE 2. UNCLAMPED ENERGY WAVEFORMS

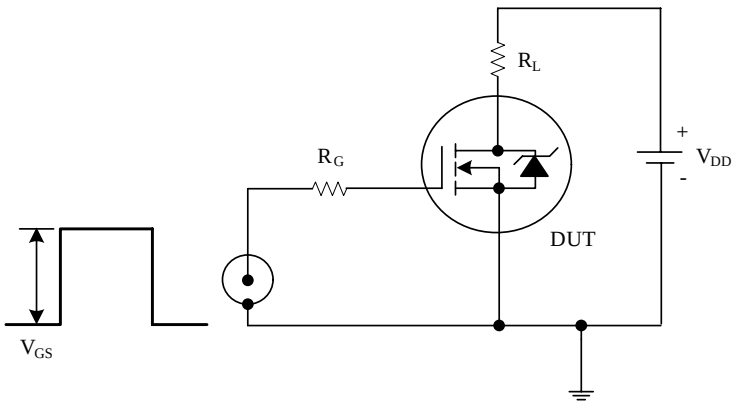


FIGURE 3. SWITCHING TIME TEST CIRCUIT

■ TEST CIRCUITS AND WAVEFORMS(cont.)

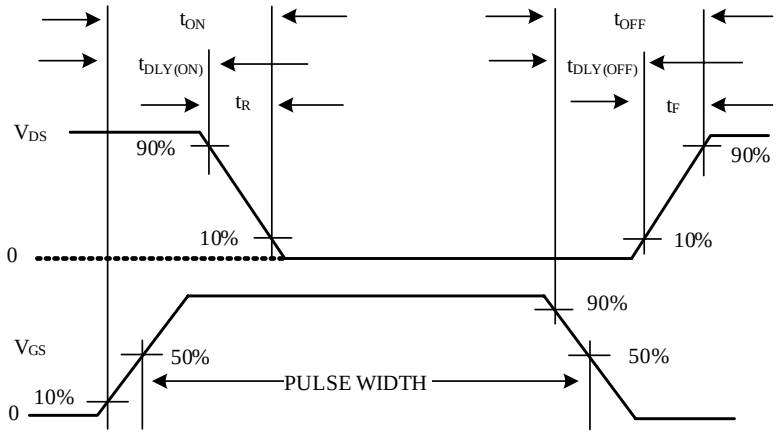


FIGURE 4. RESISTIVE SWITCHING WAVEFORMS

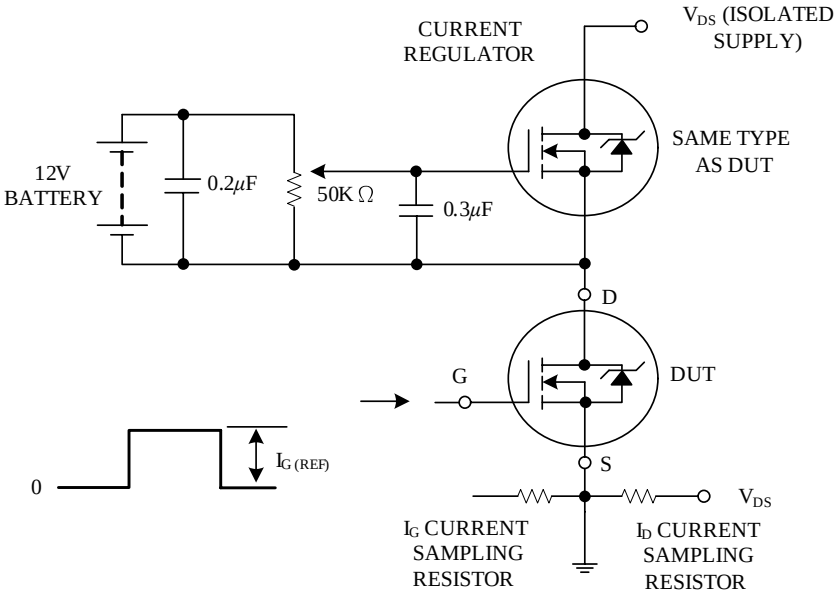


FIGURE 5. GATE CHARGE TEST CIRCUIT

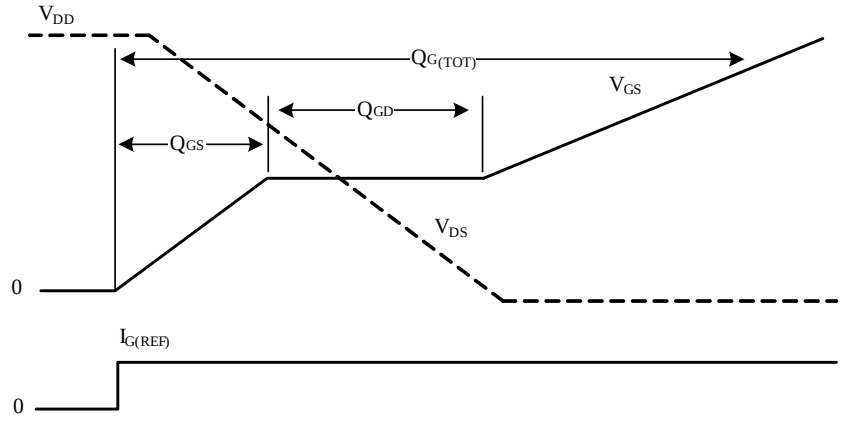


FIGURE 6. GATE CHARGE WAVEFORMS