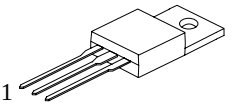
8.0 Amps, 800 Volts N-Channel MOS-FET

DESCRIPTION

These N-Channel enhancement mode power field effect Transistors are produced using planar stripe, DMOS technology.

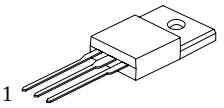
This advanced technology has been especially tailored to minimize on - state resistance , provide superior switching performance,and Withstand high energy pulse in the avalanche and commutaion mode .These devices are well suited for high efficiency switch mode power supply，electronic lamp ballasts based on half bridge topology.

P :



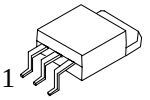
TO-220

F :



TO-220F

DD :

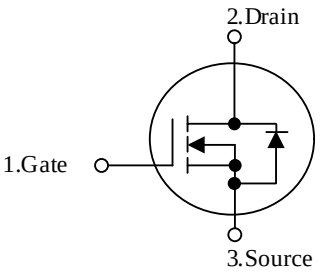


TO-263

FEATURES

* $R_{DS(ON)}$ = 1.9Ω@V_{GS} = 10V
* Fast switching capability
* Avalanche energy tested
* Improved dv/dt capability, high ruggedness

SYMBOL



ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
FTK8N80P	TO-220	G	D	S	Tube
FTK8N80F	TO-220F	G	D	S	Tube
FTK8N80DD	TO-263	G	D	S	Reel & Taping

Note: Pin Assignmen: G: Gate D: Drain S: Source

■ ABSOLUTE MAXIMUM RATINGS (T_C = 25˚C, unless otherwise specified)

PARAMET		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	800	V
Gate-Source Voltage		V_{GSS}	±30	V
Avalanche Current (Note 1)		I_{AR}	7.5	A
Continuous Drain Current	T_C = 25°C	I_D	7.5	A
	T_C = 100°C		4.2	
Pulsed Drain Current (Note 1)		I_{DM}	28	A
Avalanche Energy	Single Pulse(Note 2)	E_{AS}	580	mJ
	Repetitive Limited by $T_{J(MAX)}$	E_{AR}	16.7	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Power Dissipation (TO-220,TO-263/ TO-220F)	T_C = 25°C	P_D	142 / 48	W
	Derate above 25°C		1.14 / 0.38	W / ˚C
Junction Temperature		T_J	+150	˚C
Operating and Storage Temperature		T_{STG}	-55 ~ +150	˚C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-Ambient		θ_{JA}			62.5	˚C / W
Junction-to-Case	TO-220, TO-263	θ_{Jc}			0.88	
	TO-220F	θ_{Jc}			2.6	

■ ELECTRICAL CHARACTERISTICS (T_C = 25˚C , unless Otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS} = 0V, I_D = 250μA	800			V
Drain-Source Leakage Current		I_{DSS}	V_{DS} = 800V, V_{GS} = 0V			10	μA
Gate-Body Leakage Current	Forward	I_{GSSF}	V_{GS} = 30V, V_{DS} = 0V			100	nA
	Reverse	I_{GSSR}	V_{GS} = -30V, V_{DS} = 0V			-100	nA
Breakdown Voltage Temperature Coefficient		ΔBV_{DSS} / ΔT_J	I_D = 250μA, Referenced to 25°C		0.93		V / ˚C
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS} = 10V, I_D = 3.50A			1.9	Ω
Forward Transconductance		g_{FS}	V_{DS} = 40V, I_D = 3.5A (Note 4)		5.5		S
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz		1290		pF
Output Capacitance		C_{OSS}			120		pF
Reverse Transfer Capacitance		C_{RSS}			10		pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		$t_{D(ON)}$	V_{DD} = 300V, I_D = 7A, R_G = 25Ω (Note 4,5)		35		ns
Turn-On Rise Time		t_R			100		ns
Turn-Off Delay Time		$t_{D(OFF)}$			50		ns
Turn-Off Fall Time		t_F			60		ns
Total Gate Charge		Q_G	V_{DS} = 640V,I_D = 7A, V_{GS} = 10V (Note 4,5)		28		nC
Gate-Source Charge		Q_{GS}			8.2		nC
Gate-Drain Charge		Q_{GD}			12		nC

■ ELECTRICAL CHARACTERISTICS (T_J = 25˚C , unless Otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 7.0 A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				6.6	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				26	A
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 7.0A,		650		ns
Reverse Recovery Charge	Q_{RR}	d_{IF}/dt =100 A/μs (Note 4)		7.0		μC

Note:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 25mH, I_{AS} = 6.6A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ 8.0A, di/dt ≤ 200A/μs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Fig1. I_D - V_{DS}

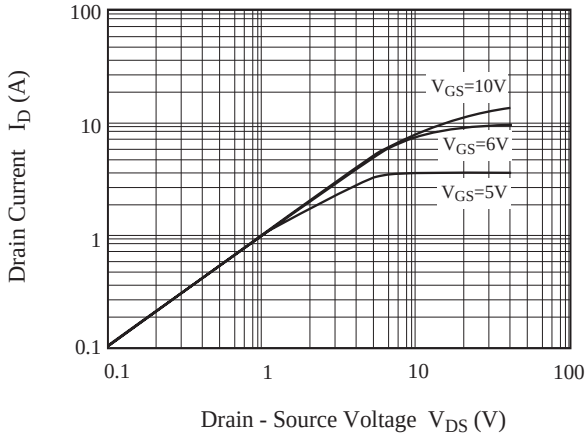


Fig2. I_D - V_{GS}

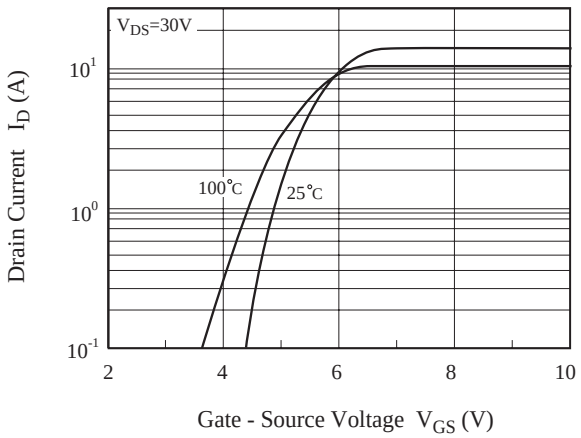


Fig3. BV_{DSS} - T_j

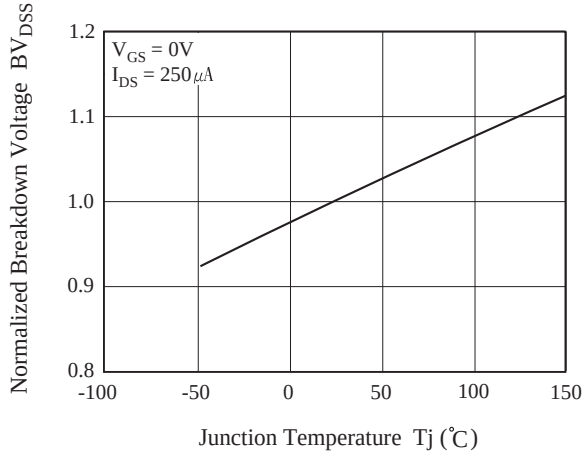


Fig4. $R_{DS(ON)}$ - I_D

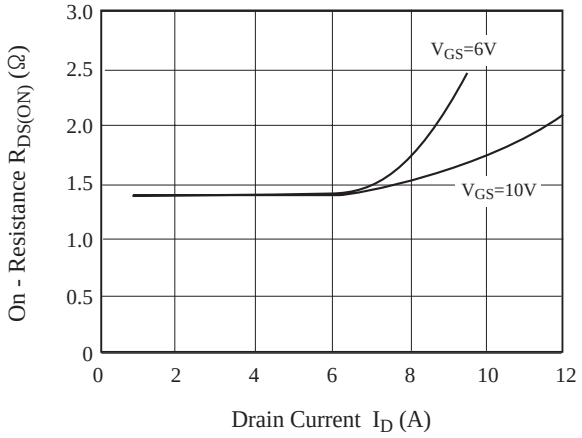


Fig5. I_S - V_{SD}

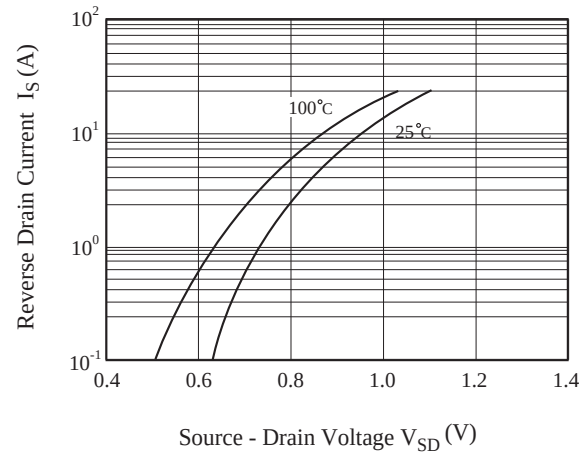


Fig6. $R_{DS(ON)}$ - T_j

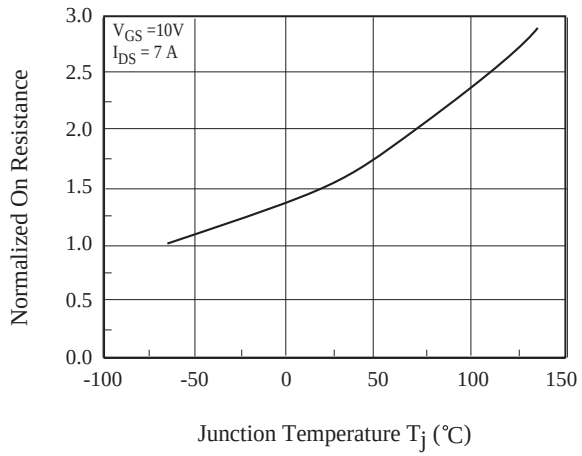


Fig 7. C - V_{DS}

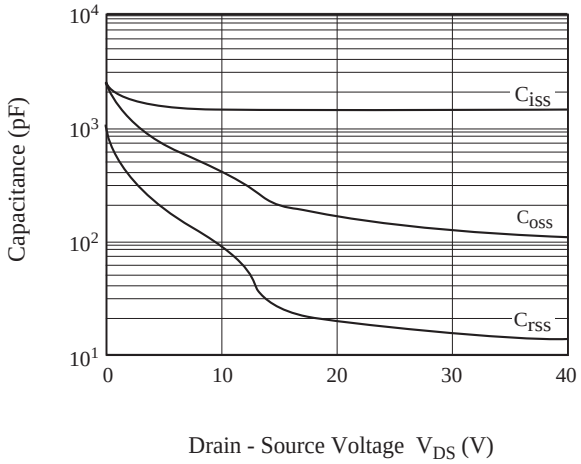


Fig8. Q_g- V_{GS}

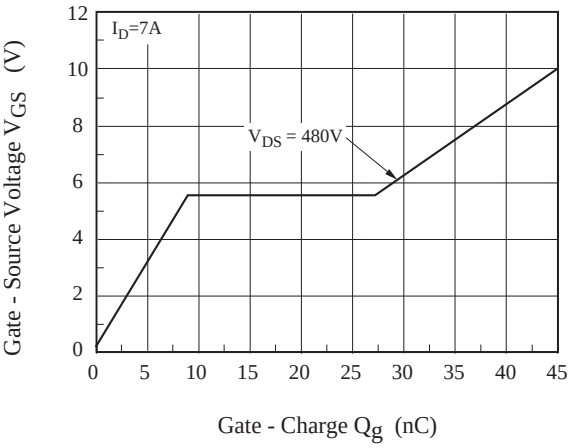


Fig9. Safe Operation Area

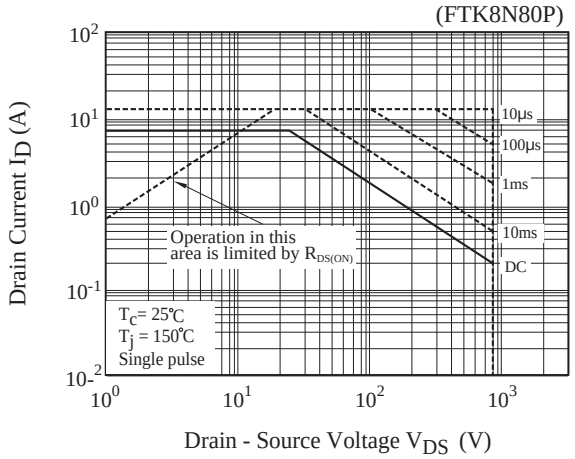


Fig10. Safe Operation Area

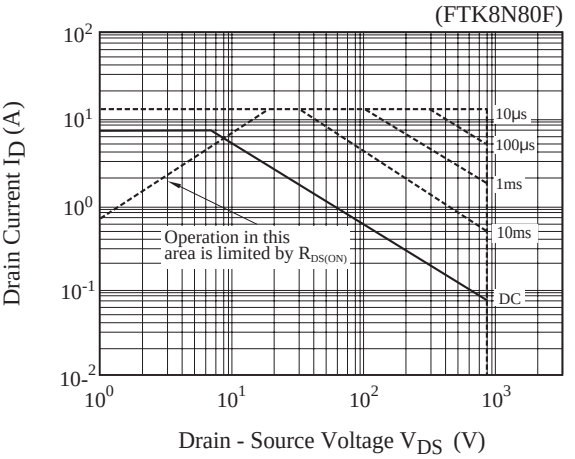


Fig11. Transient Thermal Response Curve

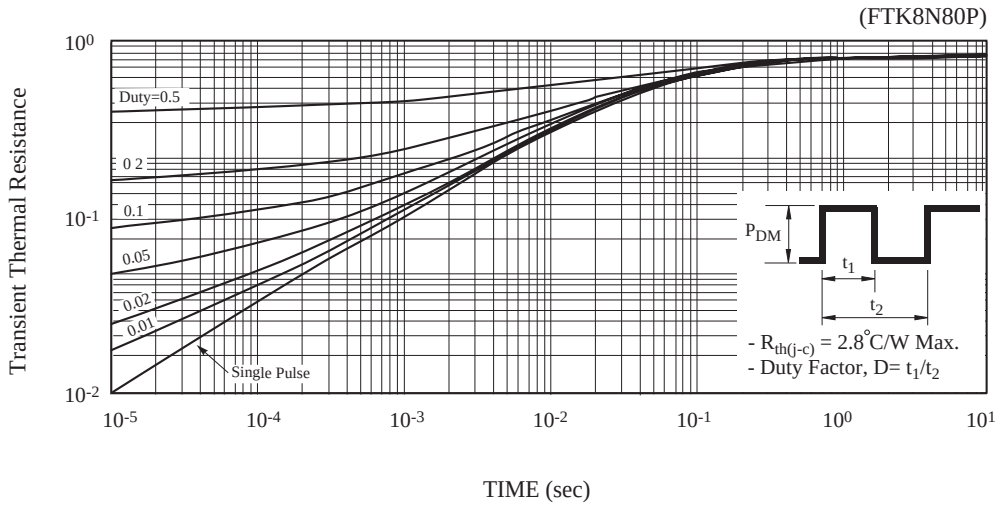
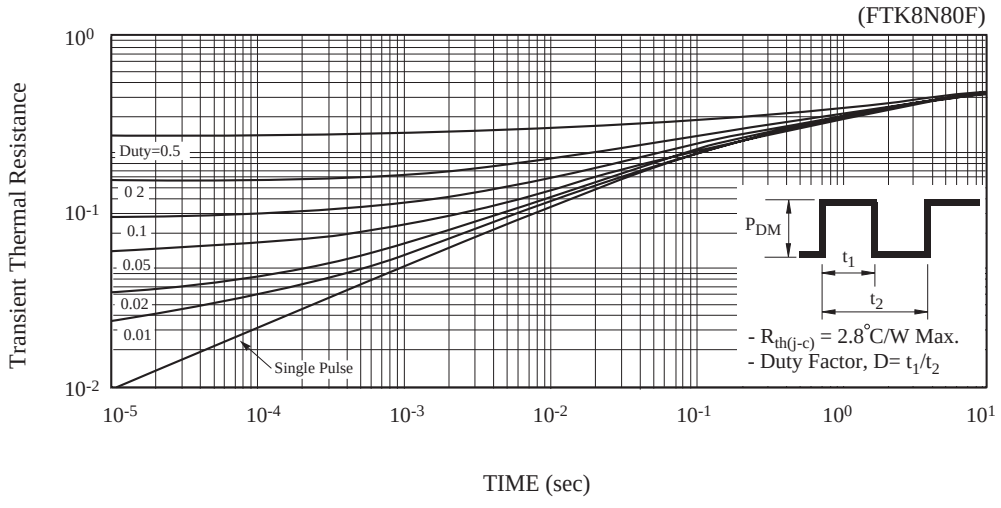


Fig12. Transient Thermal Response Curve



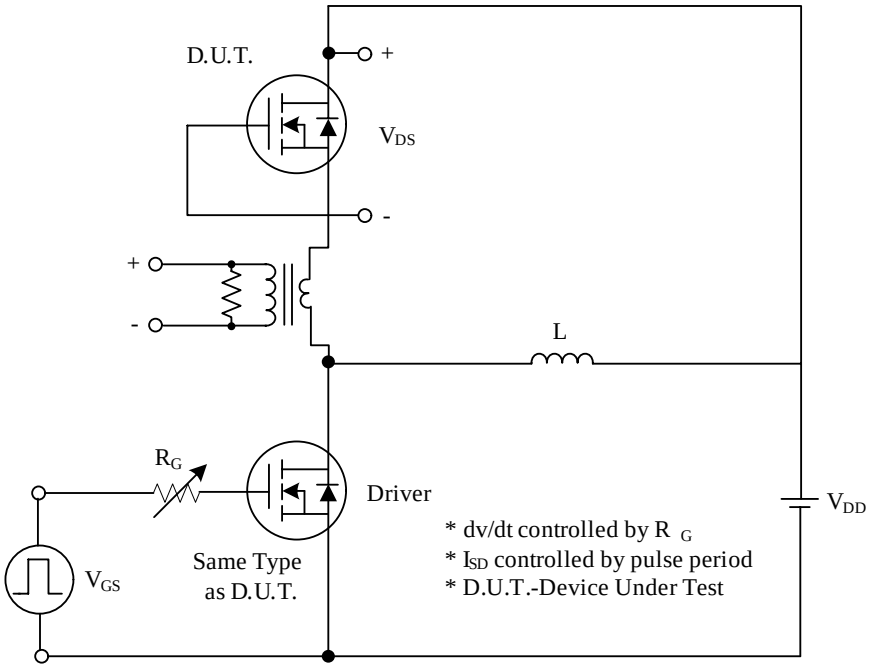


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

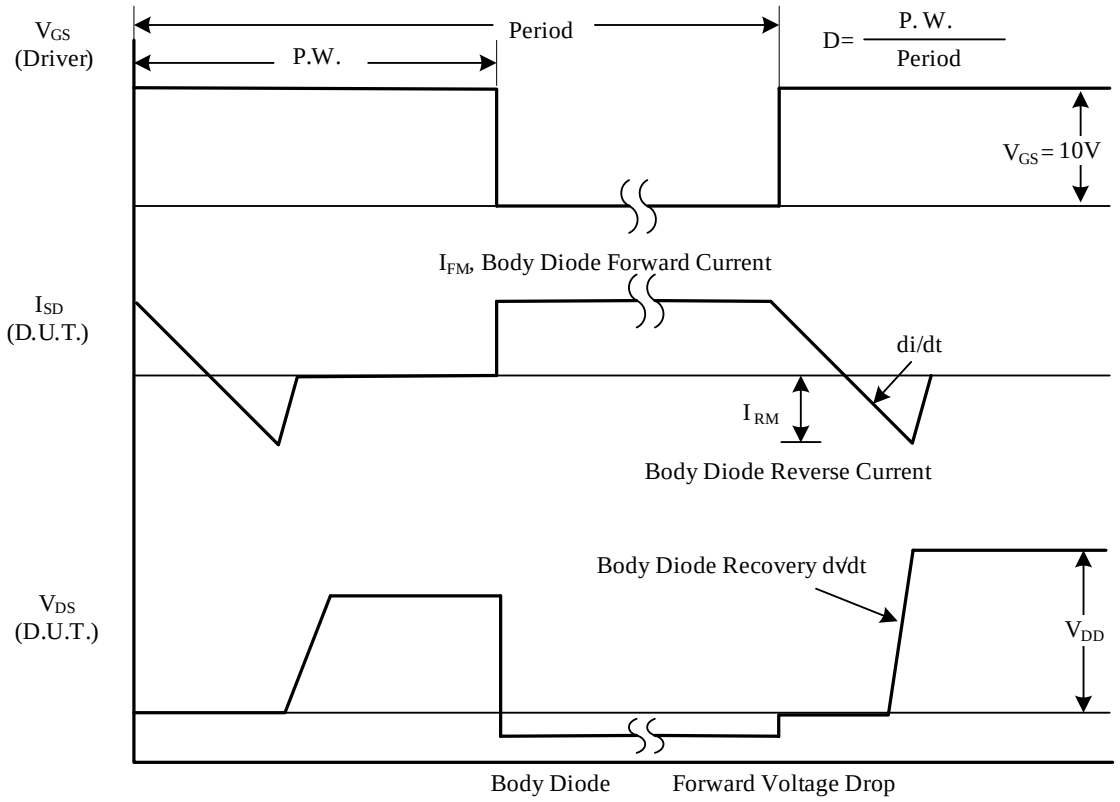


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

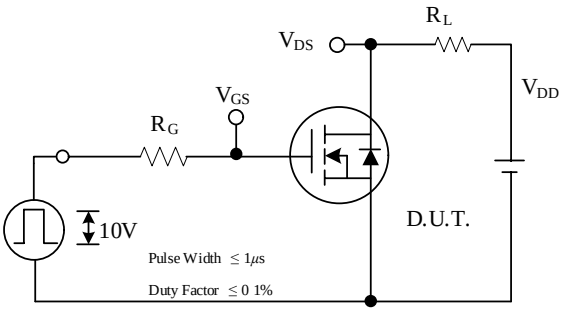


Fig. 2A Switching Test Circuit

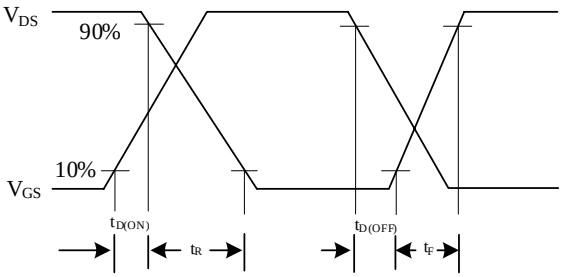


Fig. 2B Switching Waveforms

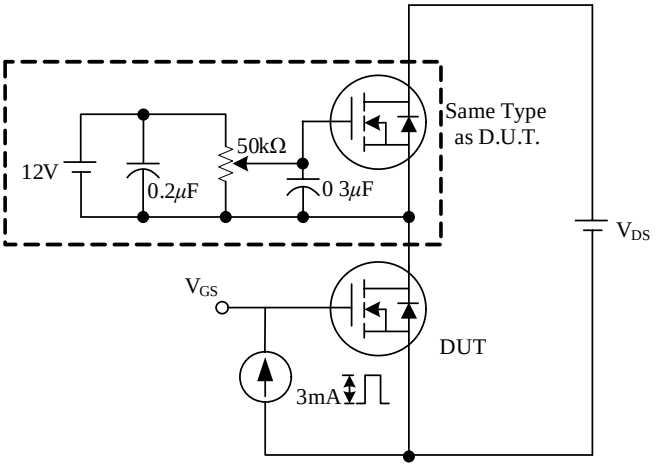


Fig. 3A Gate Charge Test Circuit

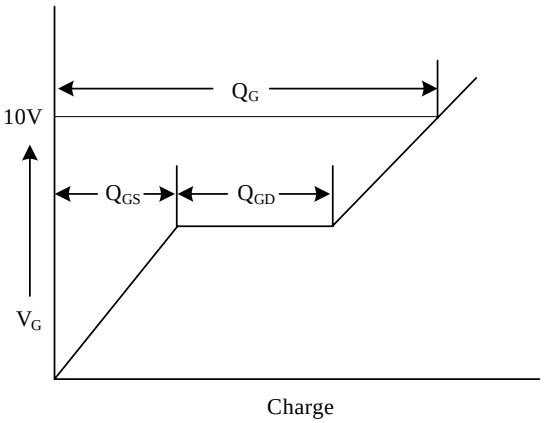


Fig. 3B Gate Charge Waveform

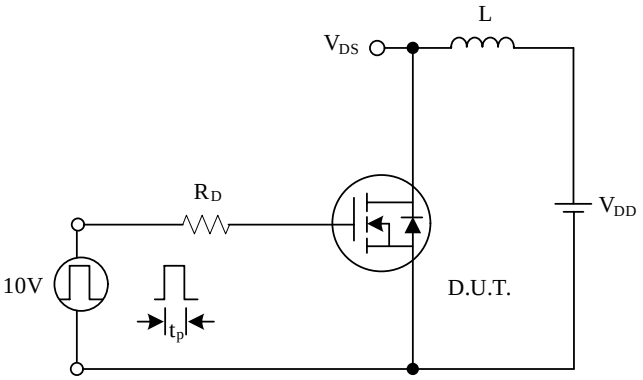


Fig. 4A Unclamped Inductive Switching Test Circuit

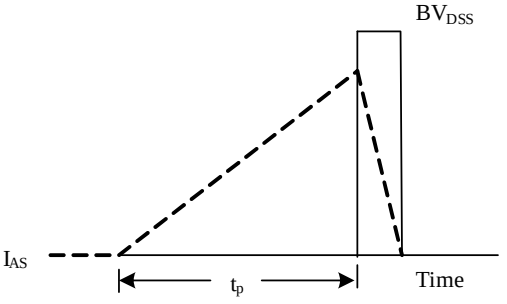


Fig. 4B Unclamped Inductive Switching Waveforms