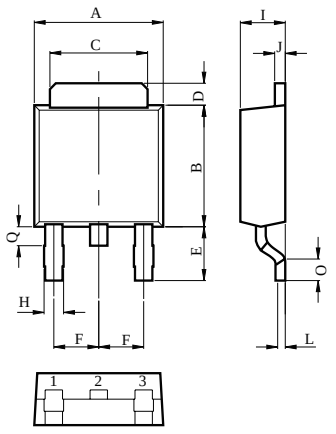
FTK40P04 P-Channel Power MOSFET

DESCRIPTION

The FTK40P04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge.

This device is well suited for high current load applications.



DIM	MILLIMETERS
A	6 50 ± 0 2
B	5 60 ± 0 2
C	5 20 ± 0 2
D	1 50 ± 0 2
E	2 70 ± 0 2
F	2 30 ± 0 1
H	1 00 MAX
I	2 30 ± 0 2
J	0 5 ± 0 1
L	0 50 ± 0 10
O	1 6 ± 0 2
Q	0 95 MAX

1 GATE
2 DRAIN
3 SOURCE

D-PAK (TO-252)

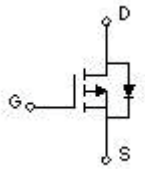
FEATURES

- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

APPLICATIONS

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply

EQUIVALENT CIRCUIT



MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain- Source Voltage	V_{DS}	- 40	V
Gate- Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	- 40	A
Pulsed Drain Current	I_{DM}	- 160	A
Single Pulsed Avalanche Energy	$E_{AS}^{(1)}$	544	mJ
Power Dissipation	P_D	1.25	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	100	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature Range	T_{stg}	- 55 ~ +150	℃
Lead Temperature for Soldering Purposes(1/8'' from case for 10s)	T_L	260	℃

(1).E_{AS} condition: V_{DD}=- 20V,L=1mH, R_G=25Ω, Starting T_J = 25°C

Electrical characteristics (T_a=25℃ unless otherwise noted)

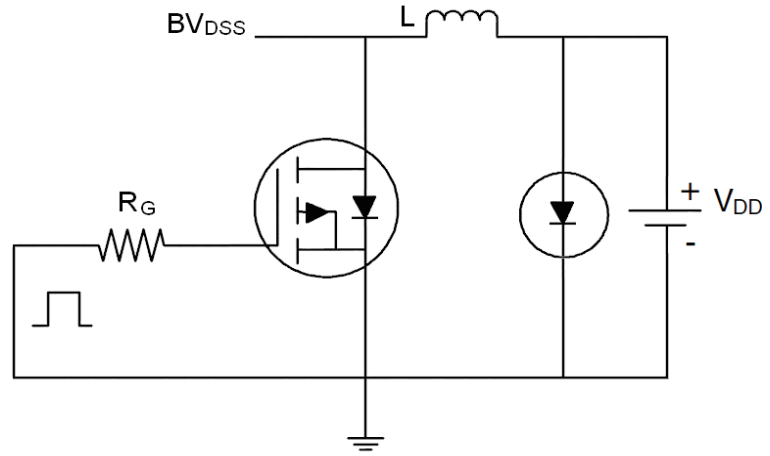
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	V_{GS} = 0V, I_D=-250μA	-40			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-40V, V_{GS}=0V			-1	μA
Gate-body leakage current	V_{GSS}	V_{DS} =0V, V_{GS} =±20V			±100	nA
On characteristics (note1)						
Gate-threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D=-250μA	-1.5		-3	V
Static drain-source on-sate resistance	$R_{DS(on)}$	V_{GS} =-10V, I_D=-12A		12	14	mΩ
Forward transconductance	g_{FS}	V_{DS} =-5V, I_D=-12A	34			S
Dynamic characteristics (note 2)						
Input capacitance	C_{iss}	V_{DS} =-20V,V_{GS}=0V, f =1MHz		2960		pF
Output capacitance	C_{oss}			370		
Reverse transfer capacitance	C_{rss}			310		
Switching characteristics (note 2)						
Total gate charge	Q_g	V_{DS}=-20V, V_{GS}=-10V, I_D=-12A		72		nC
Gate-source charge	Q_{gs}			14		
Gate-drain charge	Q_{gd}			15		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-20V, I_D=-20A V_{GS}=-10V,R_G=3Ω,		10		ns
Turn-on rise time	t_r			18		
Turn-off delay time	$t_{d(off)}$			38		
Turn-off fall time	t_f			24		
Drain-Source Diode Characteristics						
Drain-source diode forward voltage(note1)	V_{SD}	V_{GS} =0V, I_S =-20A			-1.2	V
Continuous drain-source diode forward current (note3)	I_S				-40	A
Pulsed drain-source diode forward current	I_{SM}				-160	A

Notes:

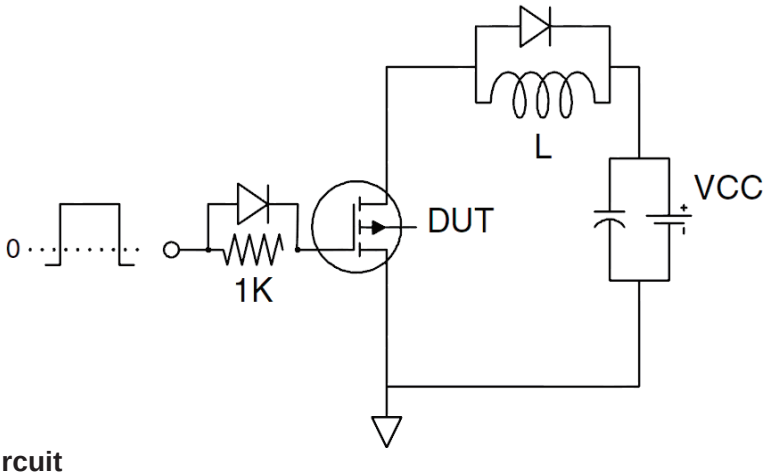
1. Pulse Test : Pulse Width≤300μs, duty cycle≤2%.
2. Guaranteed by design, not subject to production.
3. Surface Mounted on FR4 Board,≤10 sec.

Test Circuit

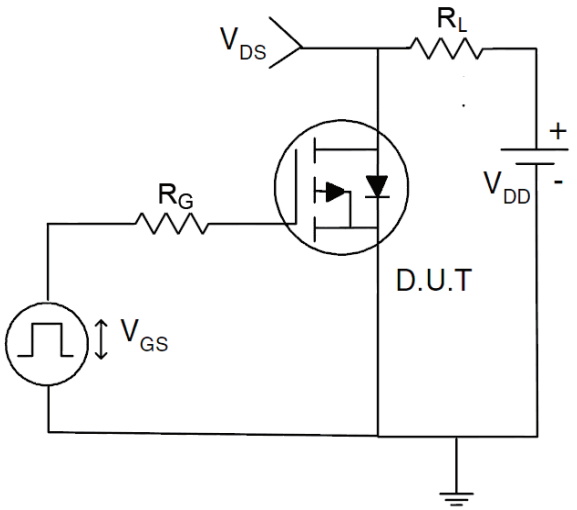
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (curves)

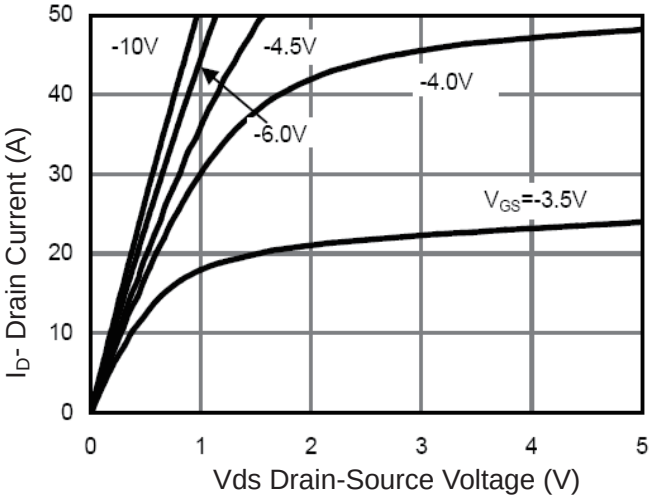


Figure 1 Output Characteristics

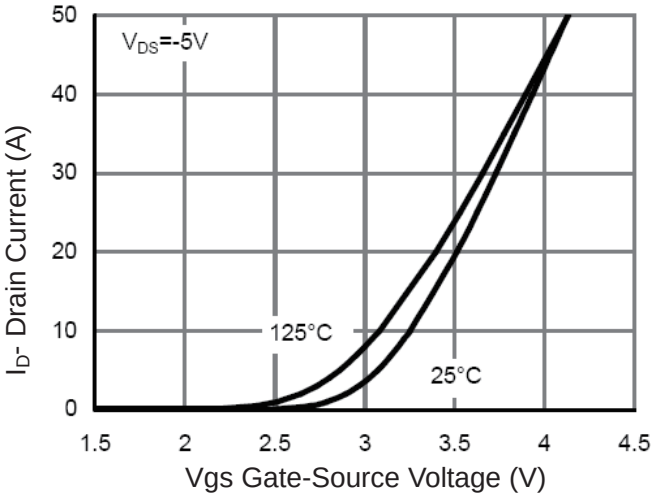


Figure 2 Transfer Characteristics

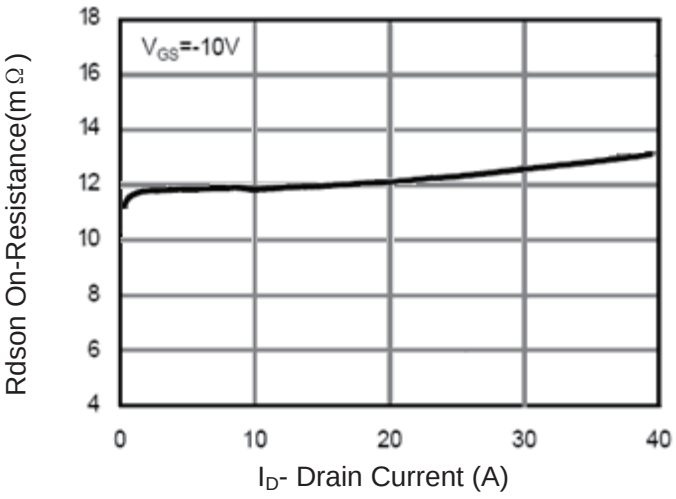


Figure 3 Rdson- Drain Current

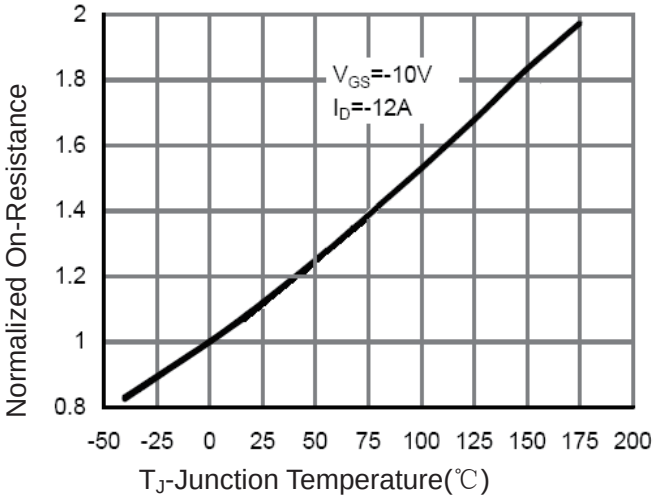


Figure 4 Rdson-Junction Temperature

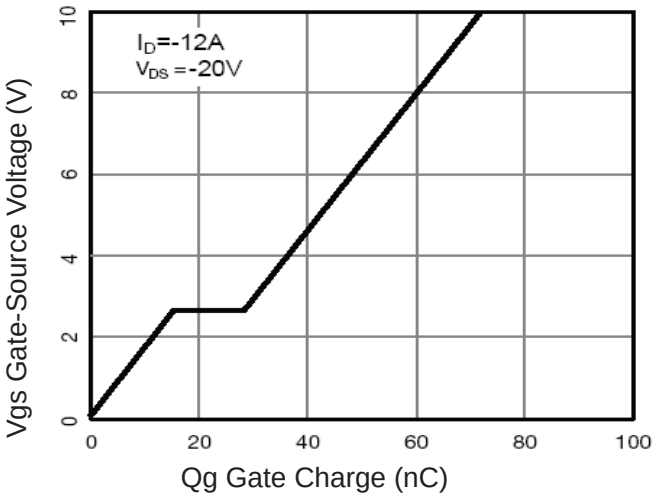


Figure 5 Gate Charge

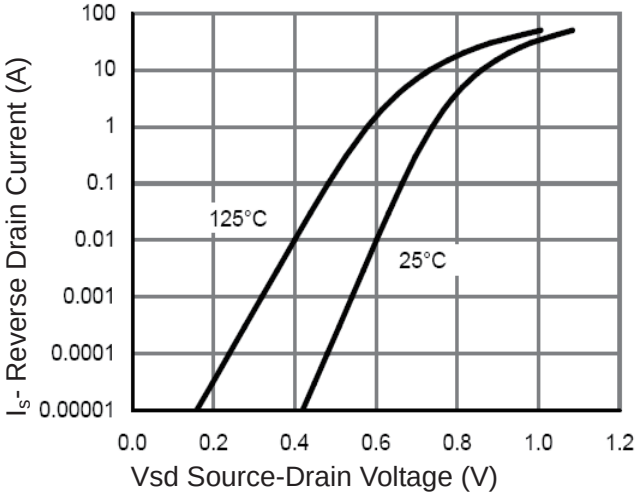


Figure 6 Source- Drain Diode Forward

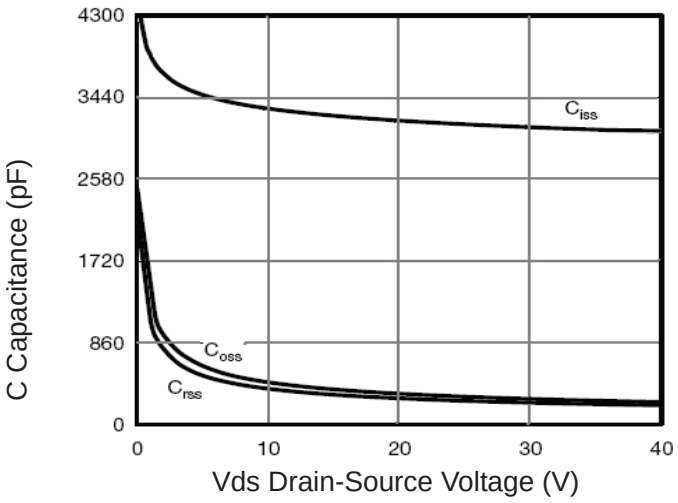


Figure 7 Capacitance vs Vds

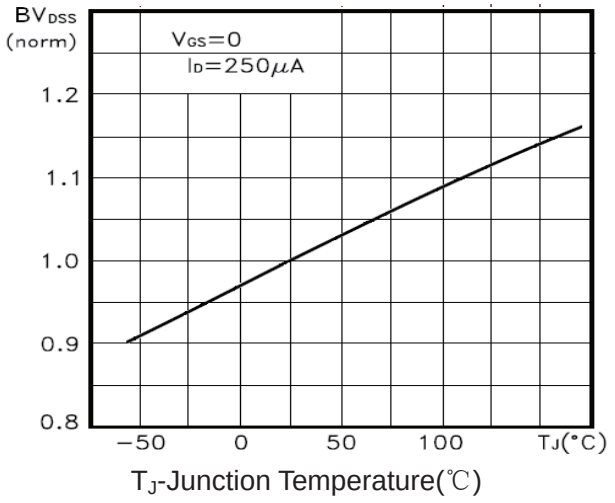


Figure 9 BV_{DSS} vs Junction Temperature

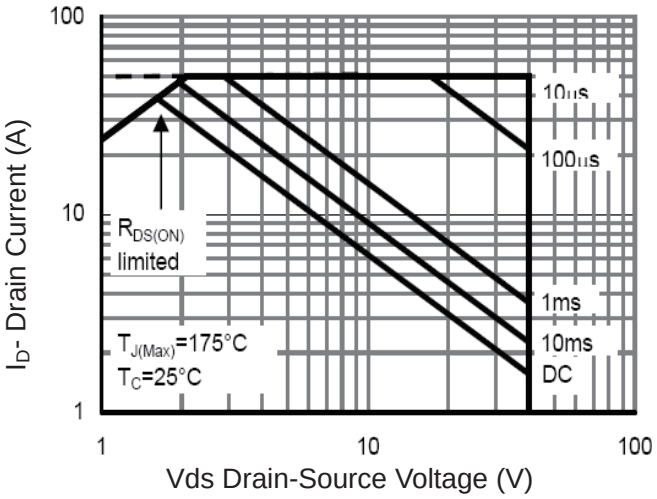


Figure 8 Safe Operation Area

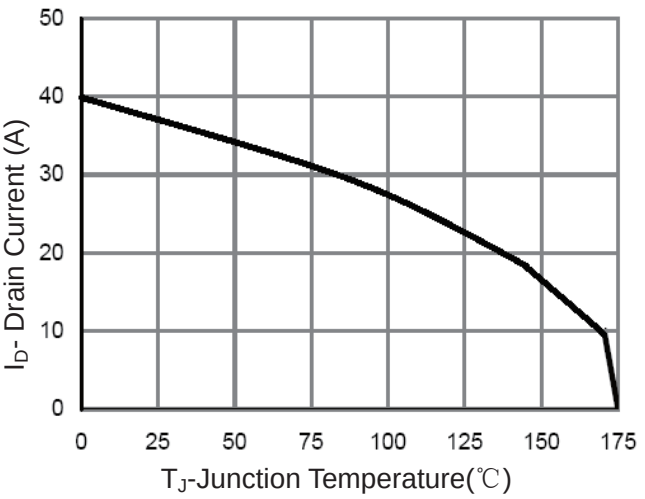


Figure 10 ID Current Derating vs Junction Temperature

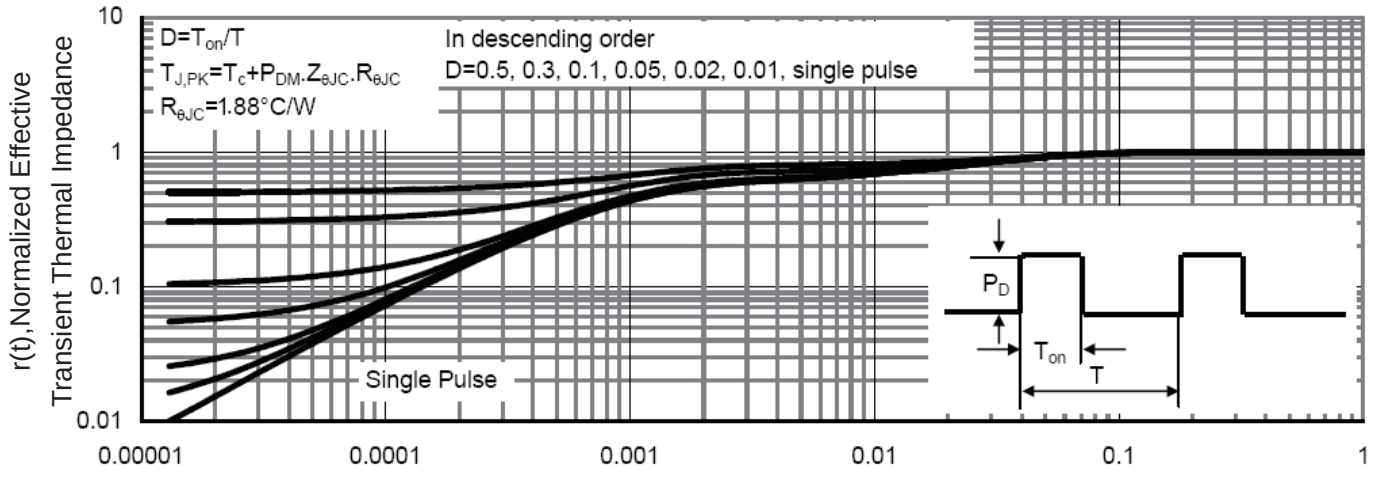


Figure 11 Normalized Maximum Transient Thermal Impedance