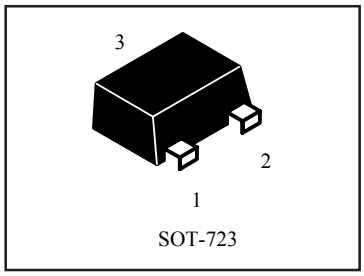
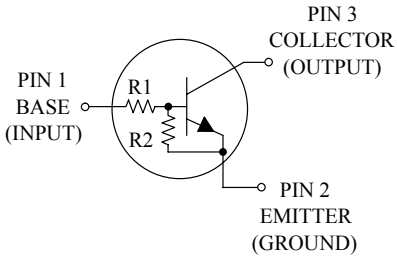
Bias Resistor Transistors

NPN Silicon Surface Mount Transistors
With Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT-723 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SOT-723 Package can be Soldered using Wave or Reflow.
- Available in 4 mm, 8000 Unit Tape & Reel





MAXIMUM RATINGS (T_A = 25 C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25 C Derate above 25 C	P_D	260 (Note 1) 600 (Note 2) 2.0 (Note 1) 4.8 (Note 2)	mW mW/ C
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	480 (Note 1) 205 (Note 2)	C/W
Junction Temperature	T_J	150	C
Storage Temperature Range	Tstg	–55 to +150	C

1. FR–4 @ Minimum Pad
2. FR–4 @ 1.0 x 1.0 inch Pad

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping
DTC701T5G	8J	4.7	4.7	SOT−723	8000/Tape & Reel
DTC702T5G	8A	10	10		
DTC703T5G	8B	22	22		
DTC704T5G	8C	47	47		
DTC705T5G	8M	2.2	47		
DTC706T5G	8K	4.7	47		
DTC707T5G	8D	10	47		
DTC708T5G	8L	22	47		
DTC709T5G	8P	47	22		
DTC710T5G	8F	4.7	∞		
DTC711T5G	94	10	∞		
DTC714T5G	8T	47	∞		
DTC717T5G	8H	2.2	2.2		
DTC722T5G	8N	100	100		

ELECTRICAL CHARACTERISTICS (T_A = 25 C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter−Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	DTC701	I_{EBO}	−	−	1.5	mAdc
	DTC702		−	−	0.5	
	DTC703		−	−	0.2	
	DTC704		−	−	0.1	
	DTC705		−	−	0.2	
	DTC706		−	−	0.18	
	DTC707		−	−	0.2	
	DTC708		−	−	0.13	
	DTC709		−	−	0.13	
	DTC710		−	−	1.9	
	DTC711		−	−	0.9	
	DTC714		−	−	0.2	
	DTC717		−	−	2.3	
	DTC722		−	−	0.05	
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	Vdc
Collector−Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	Vdc
ON CHARACTERISTICS (Note 3)						
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	DTC701	h_{FE}	15	30	−	
	DTC702		35	60	−	
	DTC703		60	100	−	
	DTC704		80	140	−	
	DTC705		80	140	−	
	DTC706		80	200	−	
	DTC707		80	140	−	
	DTC708		80	150	−	
	DTC709		80	140	−	
	DTC710		160	350	−	
	DTC711		160	350	−	
	DTC714		160	350	−	
	DTC717		8.0	15	−	
	DTC722		80	150	−	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA)		$V_{CE(sat)}$	−	−	0.25	Vdc
(I_C = 10 mA, I_B = 1 mA)	DTC701 / DTC706 / DTC708 / DTC710 / DTC711 / DTC714					
(I_C = 10 mA, I_B = 5 mA)	DTC717					
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2 5 V, R_L = 1.0 k Ω)	DTC701		−	−	0.2	
	DTC702		−	−	0.2	
	DTC703		−	−	0.2	
	DTC705		−	−	0.2	
	DTC706		−	−	0.2	
	DTC707		−	−	0.2	
	DTC708		−	−	0.2	
	DTC710		−	−	0.2	
	DTC711		−	−	0.2	
	DTC717		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 3 5 V, R_L = 1.0 k Ω)	DTC704		−	−	0.2	
	DTC714		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 k Ω)	DTC709		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 5 5 V, R_L = 1.0 k Ω)	DTC722		−	−	0.2	

3. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 4)					
Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 k Ω) (V_{CC} = 5.0 V, V_B = 0 25 V, R_L = 1.0 k Ω) DTC706 DTC710 DTC711 DTC714	V_{OH}	4.9	–	–	Vdc
Input Resistor DTC701 DTC702 DTC703 DTC704 DTC705 DTC706 DTC707 DTC708 DTC709 DTC710 DTC711 DTC714 DTC717 DTC722	R1	3.3 7.0 15.4 32.9 1.54 3.3 7.0 15.4 32.9 3.3 7.0 32.9 1.5 70	4.7 10 22 47 2 2 4.7 10 22 47 4.7 10 47 2.2 100	6.1 13 28.6 61.1 2.86 6.1 13 28.6 61.1 6.1 13 61.1 2.9 130	kΩ
Resistor Ratio DTC701 / DTC717 DTC702 / DTC703 / DTC704 / DTC722 DTC705 DTC706 DTC707 DTC708 DTC709 DTC710 / DTC711 / DTC714	R_1/R_2	0.8 0.8 0.038 0.055 0.17 0.38 1.7 –	1.0 1.0 0.047 0.1 0.21 0.47 2.1 –	1.2 1.2 0.056 0.185 0.25 0.56 2.6 –	

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

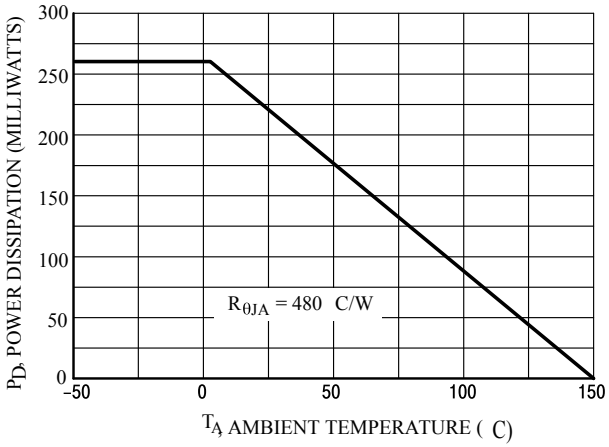


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS − DTC702

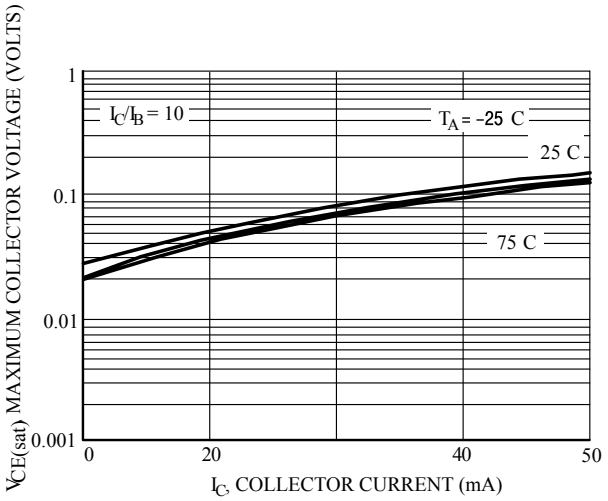


Figure 2. $V_{CE(sat)}$ versus I_C

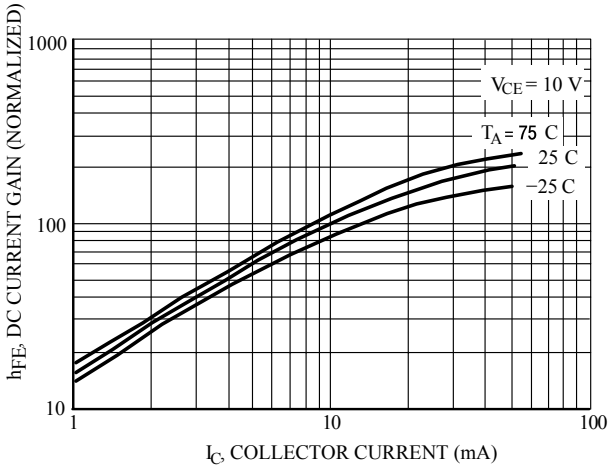


Figure 3. DC Current Gain

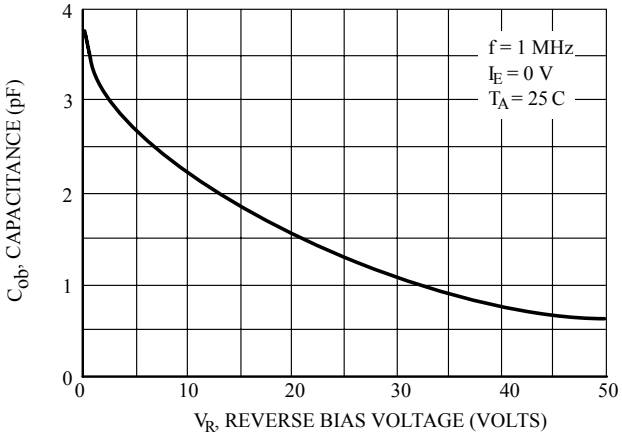


Figure 4. Output Capacitance

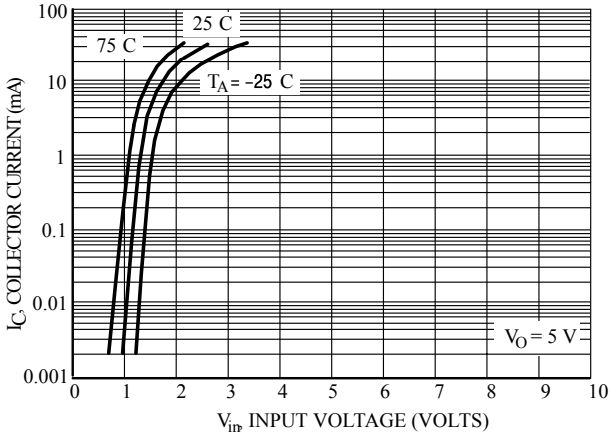


Figure 5. Output Current versus Input Voltage

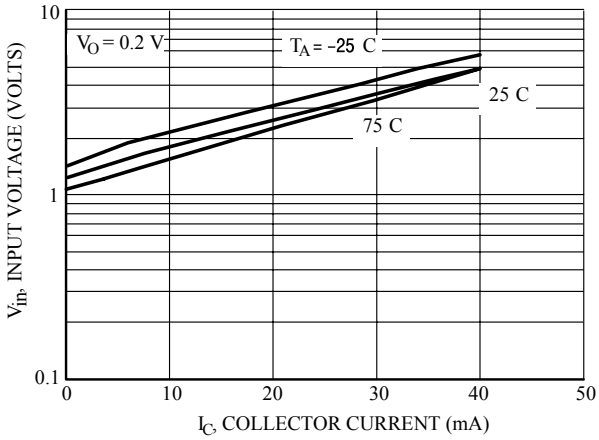


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC703

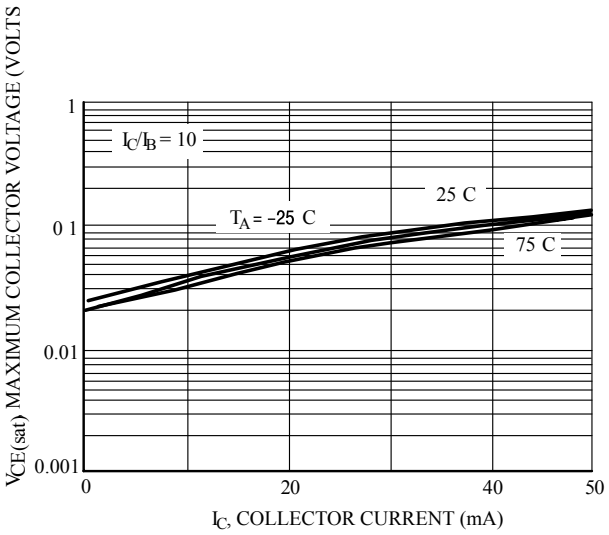


Figure 7. $V_{CE(sat)}$ versus I_C

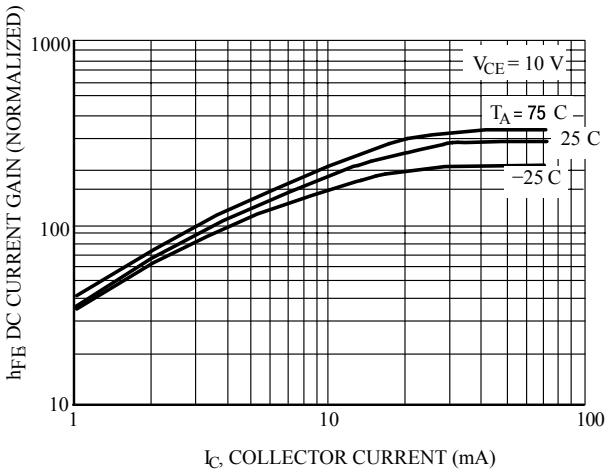


Figure 8. DC Current Gain

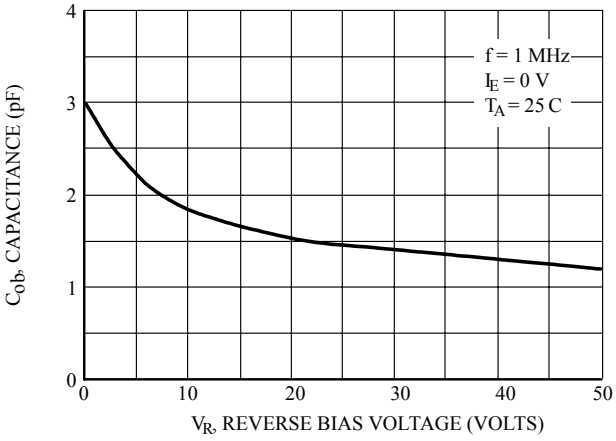


Figure 9. Output Capacitance

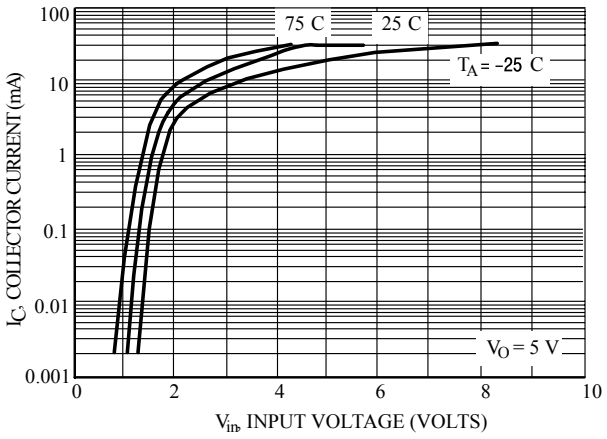


Figure 10. Output Current versus Input Voltage

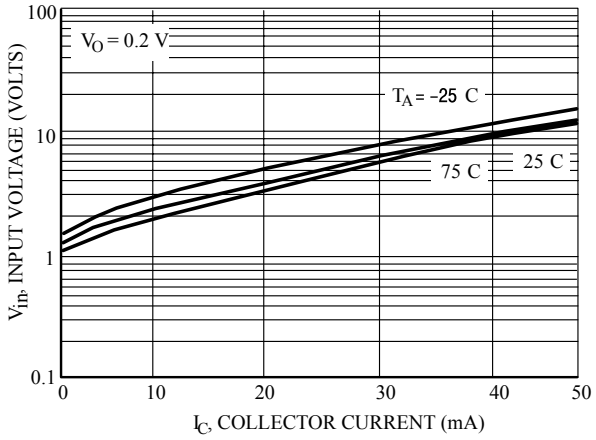


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC704

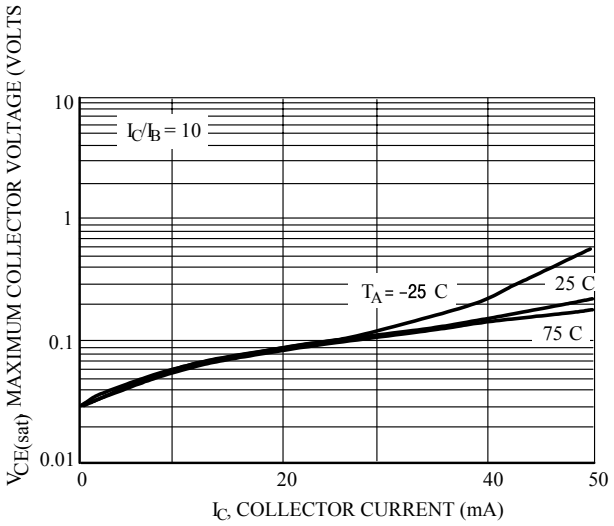


Figure 12. $V_{CE(sat)}$ versus I_C

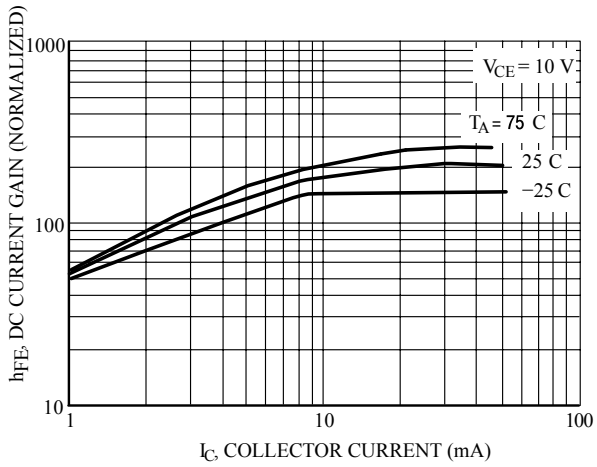


Figure 13. DC Current Gain

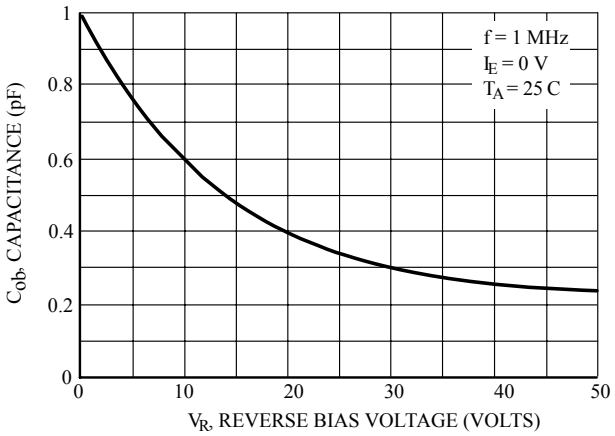


Figure 14. Output Capacitance

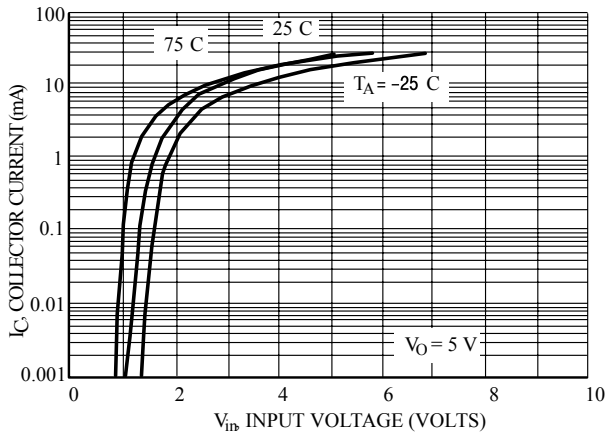


Figure 15. Output Current versus Input Voltage

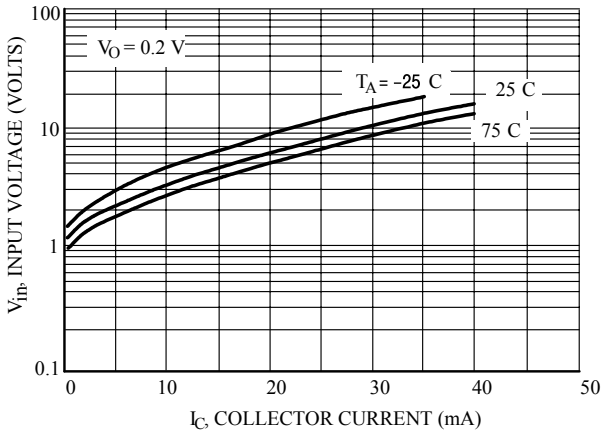


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC707

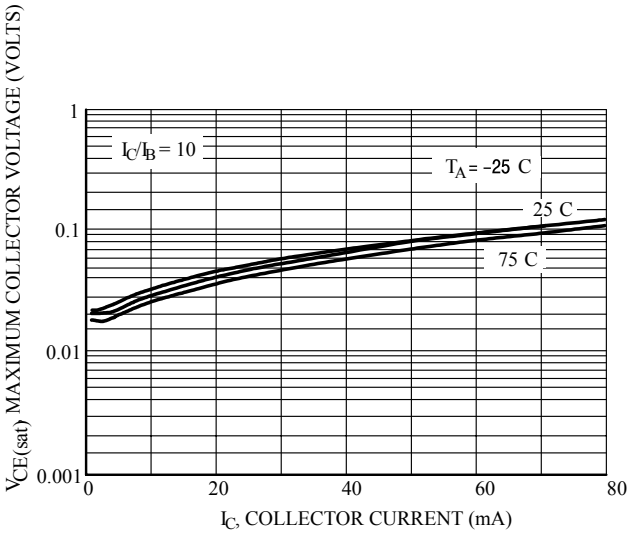


Figure 17. $V_{CE(sat)}$ versus I_C

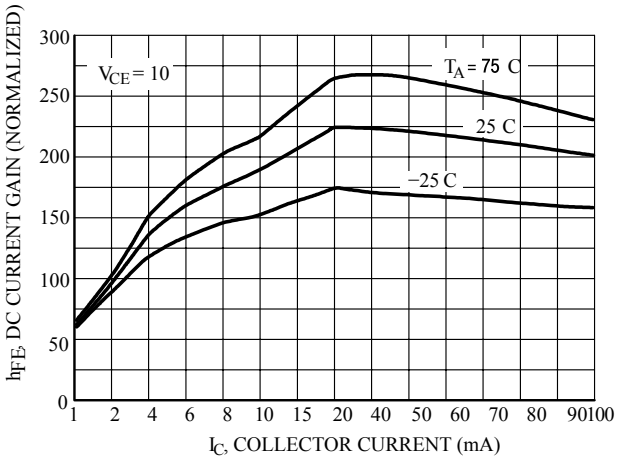


Figure 18. DC Current Gain

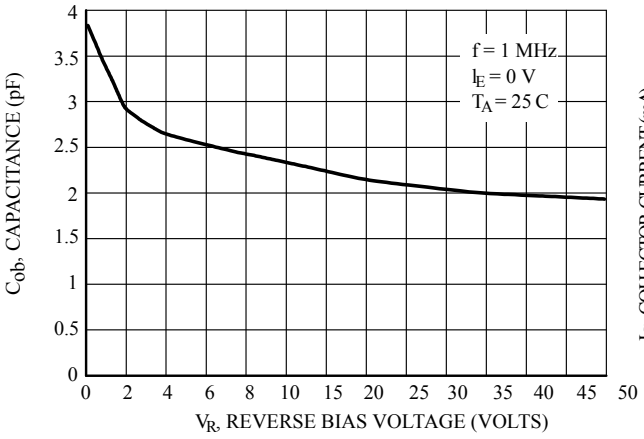


Figure 19. Output Capacitance

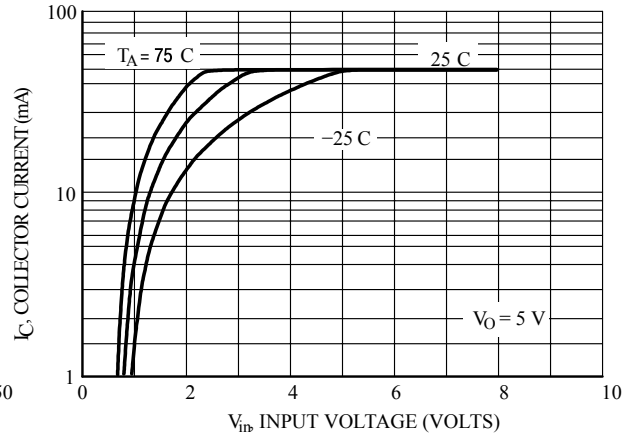


Figure 20. Output Current versus Input Voltage

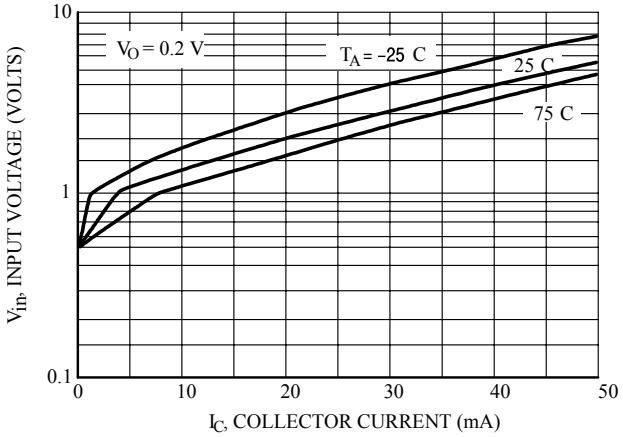


Figure 21. Input Voltage versus Output Current

TYPICAL APPLICATIONS FOR NPN BRTs

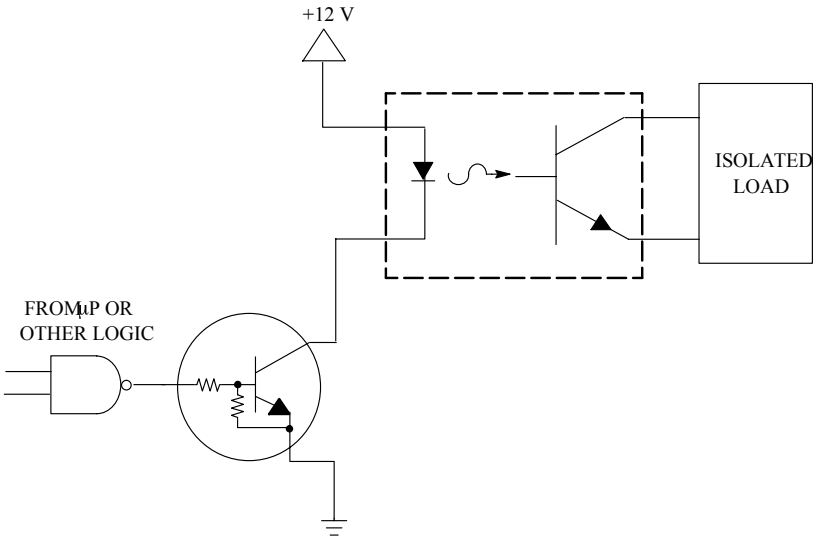


Figure 22. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

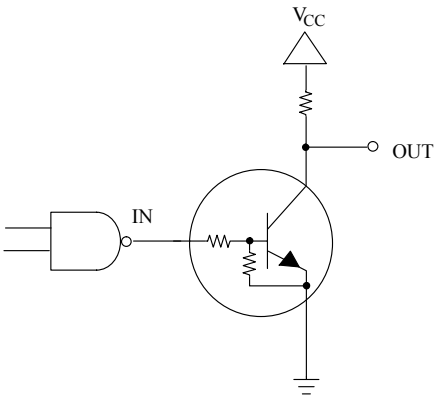


Figure 23. Open Collector Inverter:
Inverts the Input Signal

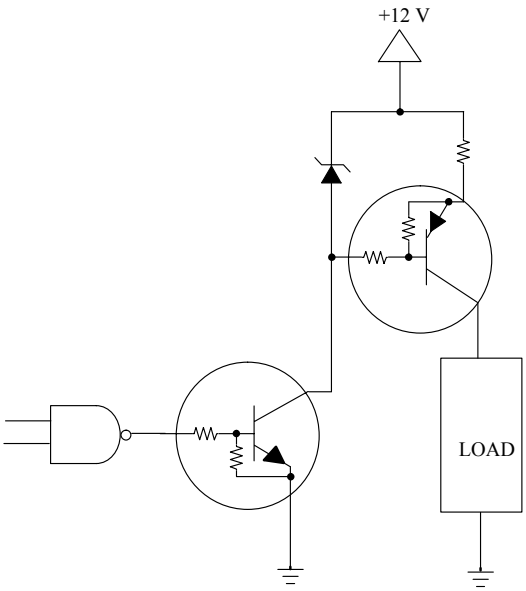
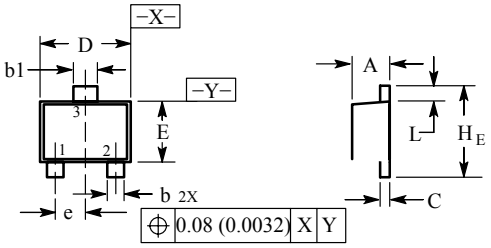


Figure 24. Inexpensive, Unregulated Current Source

PACKAGE DIMENSIONS

SOT−723

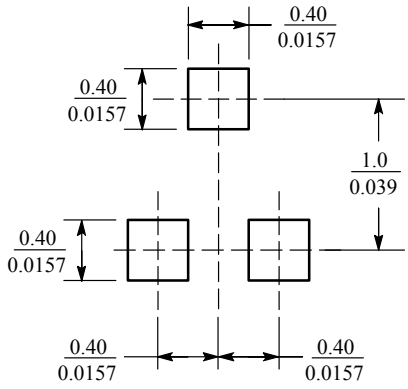


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PIN 1. BASE
2. EMITTER
3. COLLECTOR

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
b	0.15	0.20	0.27	0.0059	0.0079	0.0106
b1	0.25	0.3	0.35	0.010	0.012	0.014
C	0.07	0.12	0.17	0.0028	0.0047	0.0067
D	1.15	1.20	1.25	0.045	0.047	0.049
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.40 BSC			0.016 BSC		
H_E	1.15	1.20	1.25	0.045	0.047	0.049
L	0.15	0.20	0.25	0.0059	0.0079	0.0098

SOLDERING FOOTPRINT



$\left(\frac{mm}{inches}\right)$