

**20V P-Channel Enhancement Mode MOSFET**

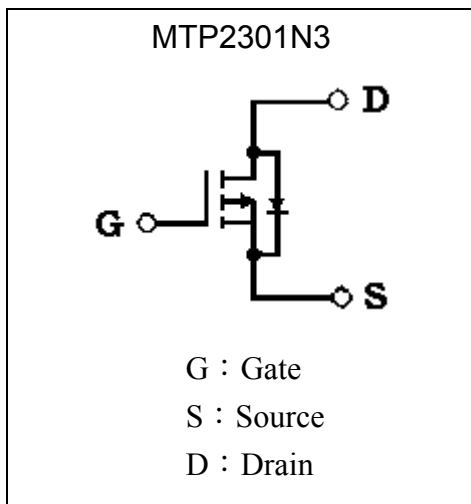
# MTP2301N3

$BV_{DSS}$	-20V
$I_D$	-3.4A
$R_{DSON(TYP)}@V_{GS}=-4.5V, I_D=-2.8A$	79mΩ
$R_{DSON(TYP)}@V_{GS}=-2.5V, I_D=-2A$	116mΩ

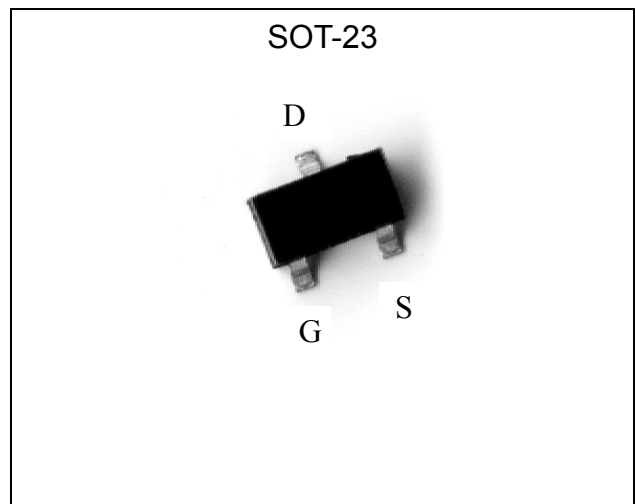
**Features**

- Advanced trench process technology
- High density cell design for ultra low on resistance
- Excellent thermal and electrical capabilities
- Compact and low profile SOT-23 package
- Pb-free lead plating and halogen-free package

**Equivalent Circuit**

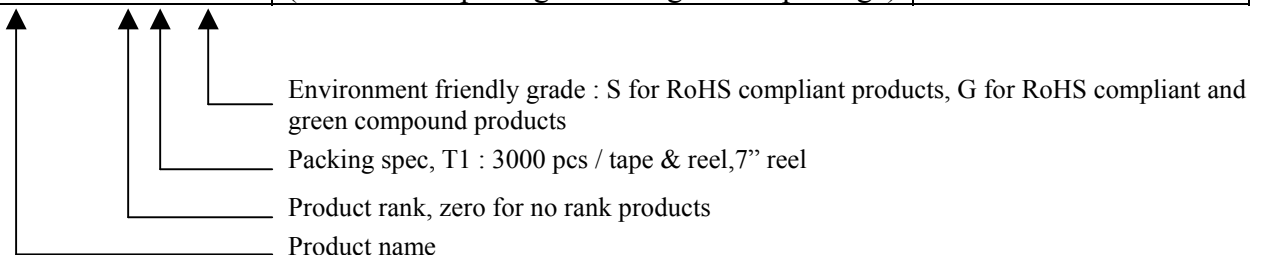


**Outline**



**Ordering Information**

Device	Package	Shipping
MTP2301N3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel





**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	VDS	-20	V
Gate-Source Voltage	VGS	±8	V
Continuous Drain Current @TA=25°C, VGS=-4.5V	ID	-3.4	A
Continuous Drain Current @TA=70°C, VGS=-4.5V		-2.7	
Pulsed Drain Current	IDM	-10	
Maximum Power Dissipation	PD	Ta=25°C	1.38 (Note)
		Ta=70°C	0.88 (Note)
Operating Junction and Storage Temperature Range	Tj ; Tstg	-55~+150	°C

**Thermal Performance**

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient(PCB mounted)	Rth,ja	90 (Note)	°C/W
Lead Temperature, for 5 second soldering(1/8" from case)	TL	260	°C

Note : Surface mounted on 1 in ²FR-4 board with 2 oz. copper, t ≤ 5sec; 270 °C/W when mounted on minimum copper pad.

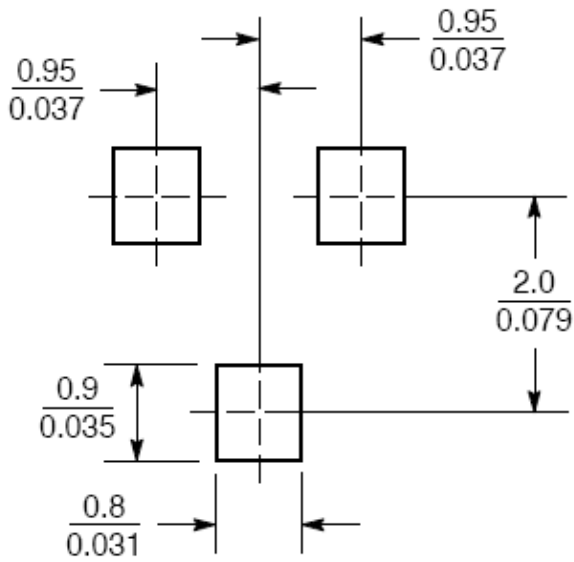
**Electrical Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BVDSS	-20	-	-	V	VGS=0, ID=-250µA
VGS(th)	-0.45	-	-	V	VDS=VGS, ID=-250µA
IGSS	-	-	±100	nA	VGS=±8V, VDS=0
IDSS	-	-	-1	µA	VDS=-16V, VGS=0
*RDS(ON)	-	79	100	mΩ	ID=-2.8A, VGS=-4.5V
	-	116	150		ID=-2A, VGS=-2.5V
*GFS	-	6.3	-	S	VDS=-5V, ID=-2.8A
<b>Dynamic</b>					
Ciss	-	446	-	pF	VDS=-10V, VGS=0, f=1MHz
Coss	-	57	-		
Crss	-	52	-		
td(ON)	-	9.2	20	ns	VDD=-10V, ID=-1A, RL=6Ω, VGEN=-4.5V, RG=6Ω
tr	-	7.3	60		
td(OFF)	-	38	50		
tf	-	12	20		
Qg	-	3	10	nC	VDS=-10V, ID=-3A, VGS=-2.5V,
Qgs	-	0.8	-		
Qgd	-	1.1	-		

Source-Drain Diode					
$I_S$	-	-	-1.6	A	-
$V_{SD}$	-	-0.86	-1.2	V	$V_{GS}=0V, I_S=-1.6A$
$t_{rr}^*$	-	30	-	ns	$I_F=-3A, dI_F/dt=100A/\mu s$
$Q_{rr}^*$	-	25	-	nC	

\*Pulse Test : Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$

**Recommended Soldering Footprint**

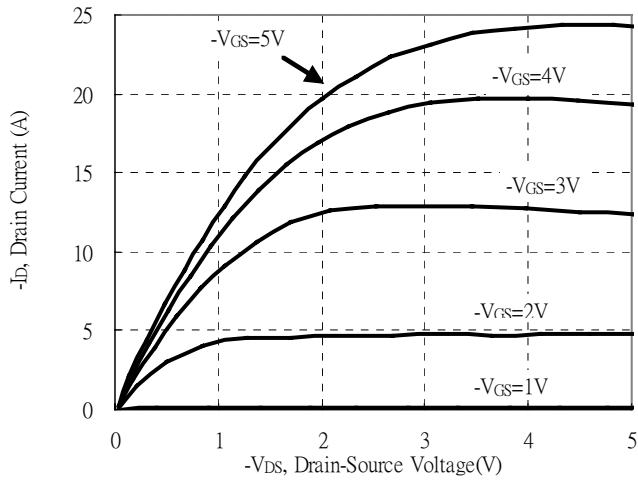


Unit :  $\frac{mm}{inches}$

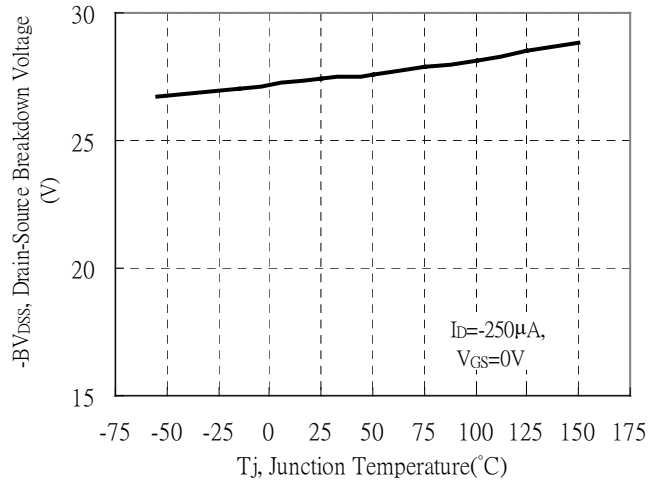


### Typical Characteristics

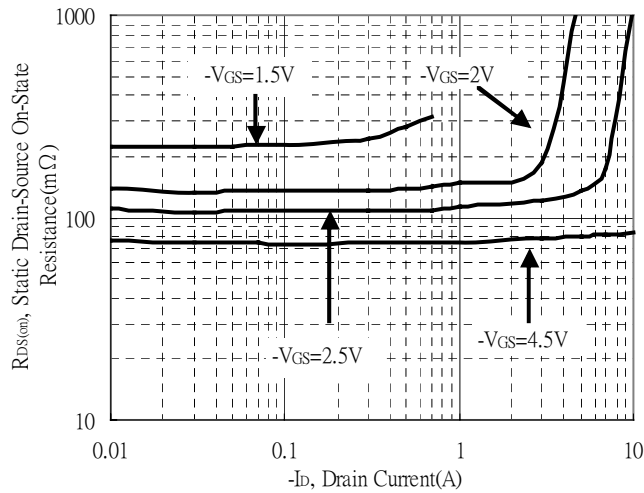
Typical Output Characteristics



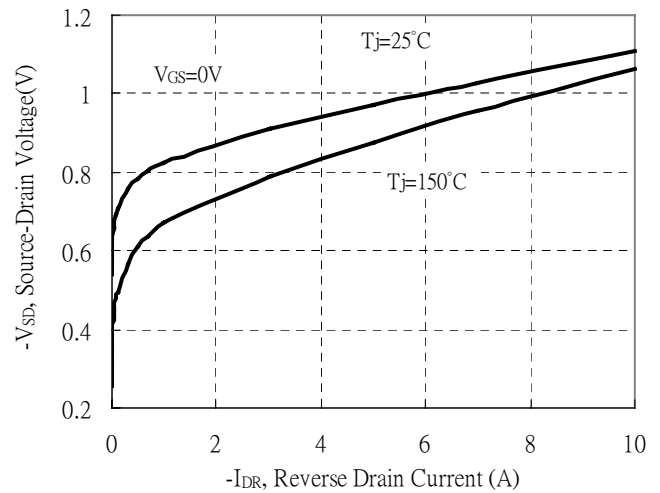
Brekdown Voltage vs Ambient Temperature



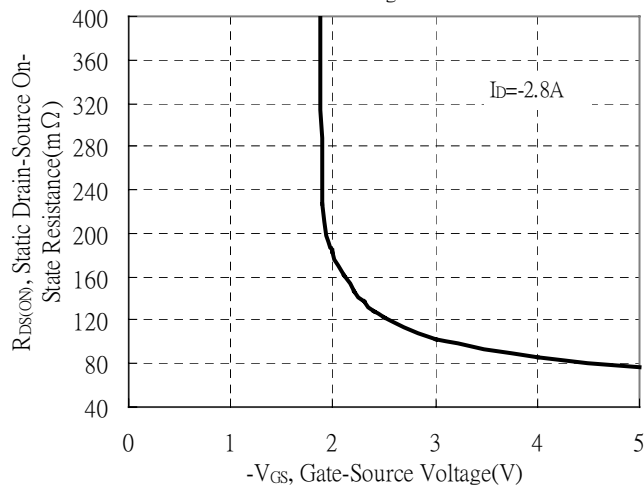
Static Drain-Source On-State resistance vs Drain Current



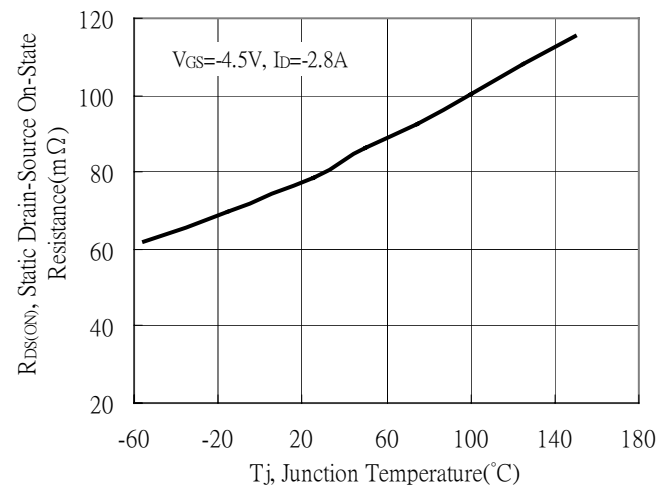
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

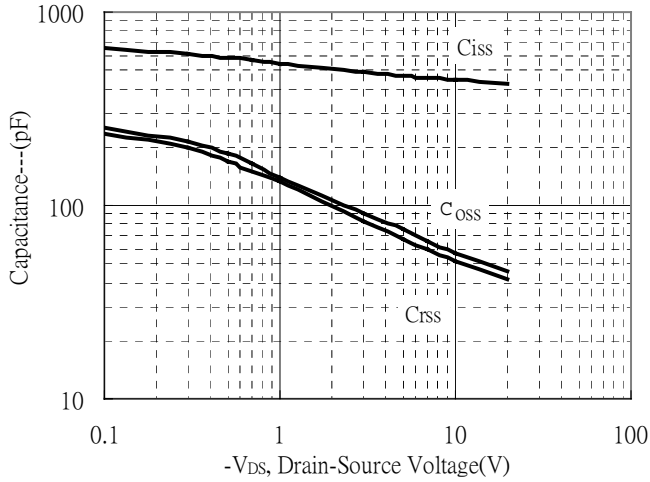


Drain-Source On-State Resistance vs Junction Temperature

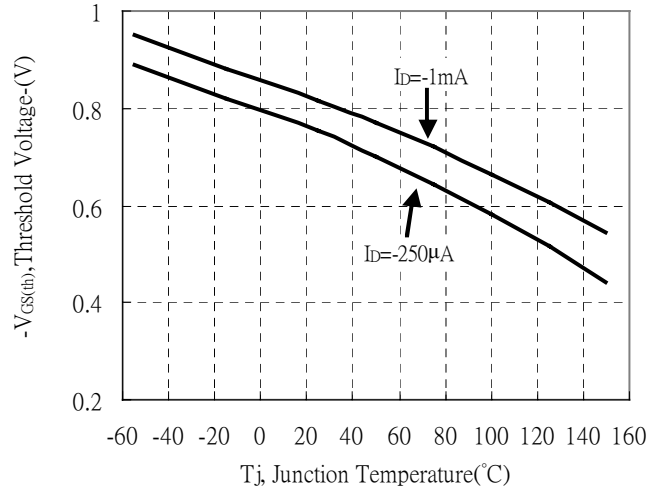


## Typical Characteristics(Cont.)

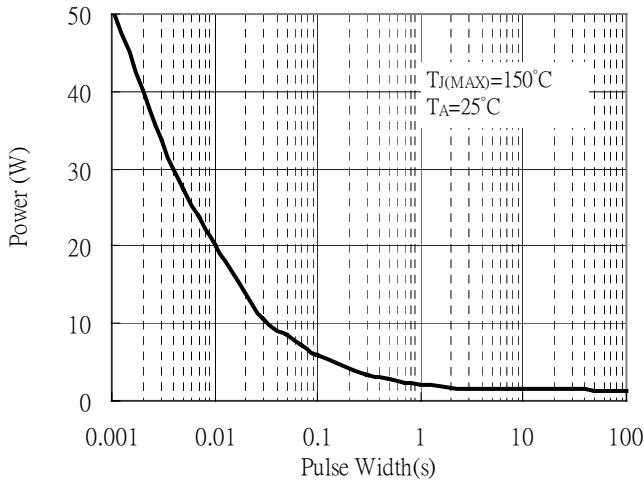
Capacitance vs Drain-to-Source Voltage



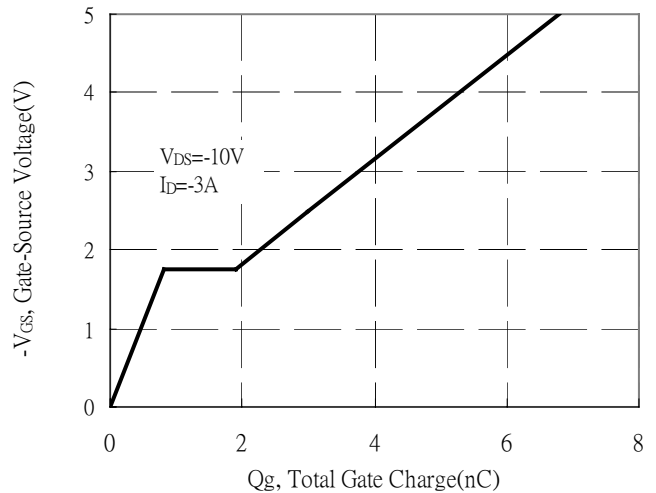
Threshold Voltage vs Junction Temperature



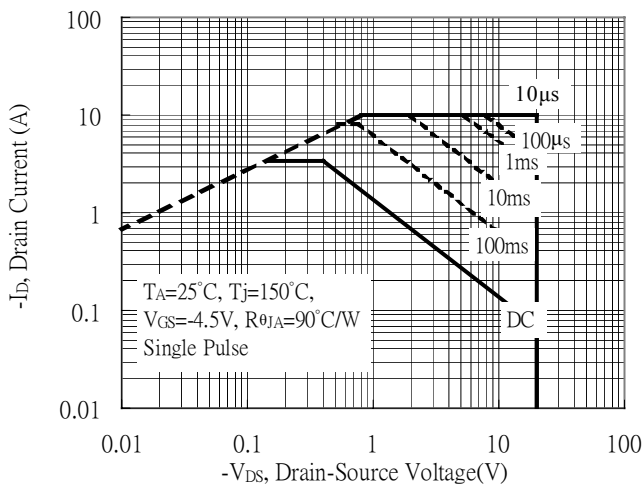
Single Pulse Power Rating, Junction to Ambient  
 (Note 1 on page 2)



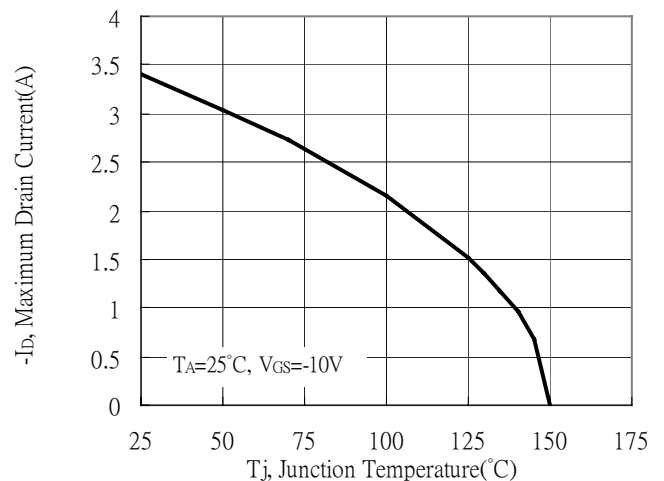
Gate Charge Characteristics



Maximum Safe Operating Area



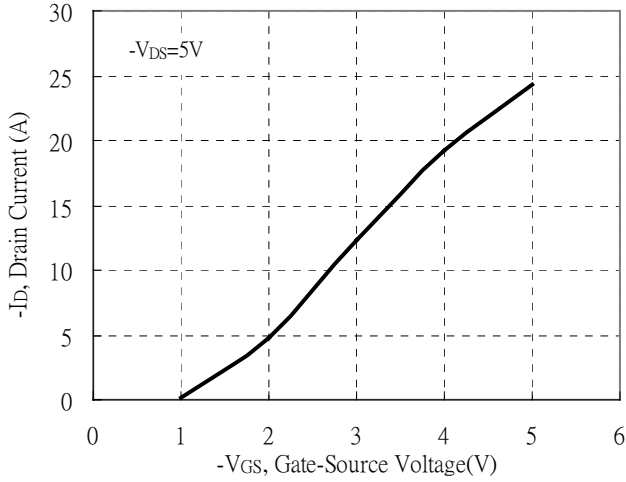
Maximum Drain Current vs Junction Temperature



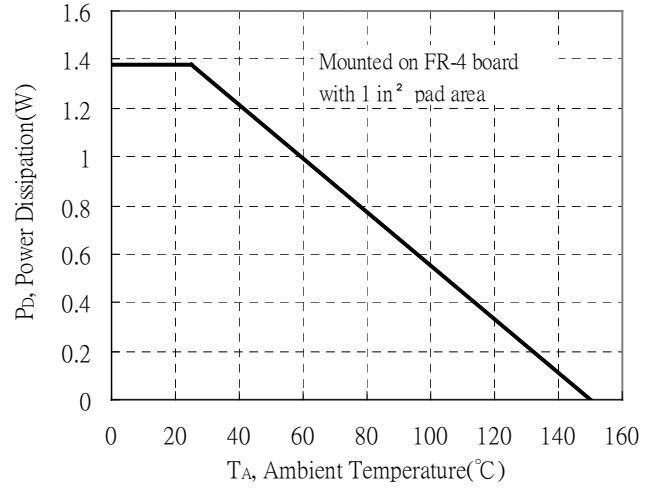


### Typical Characteristics(Cont.)

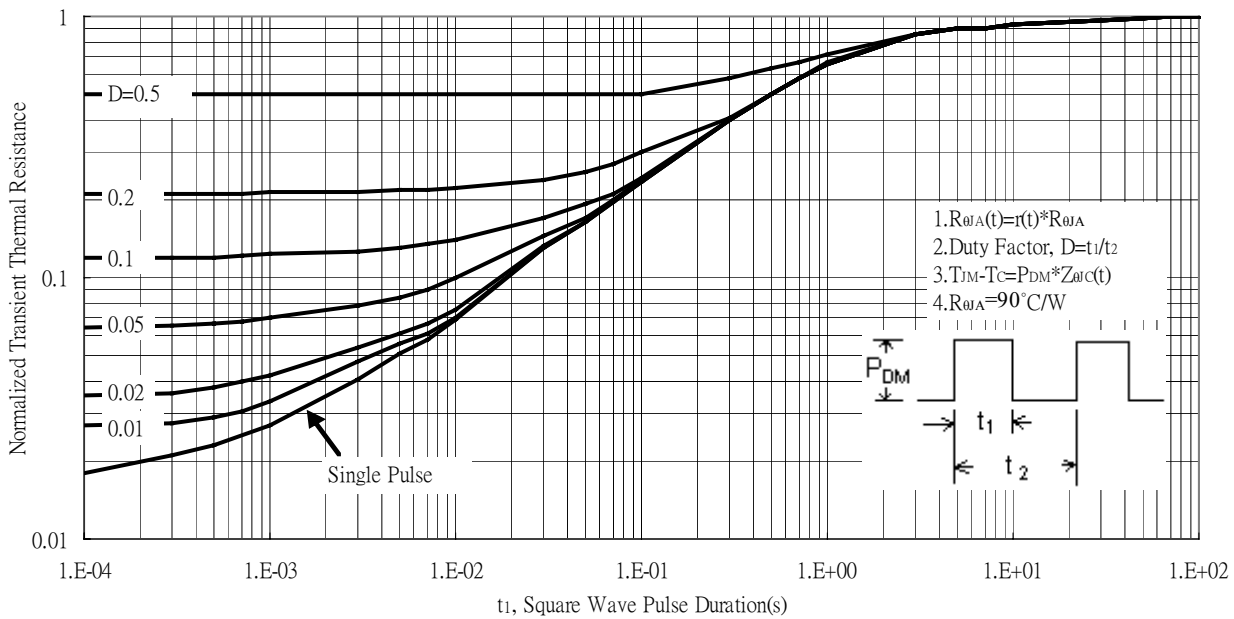
Typical Transfer Characteristics



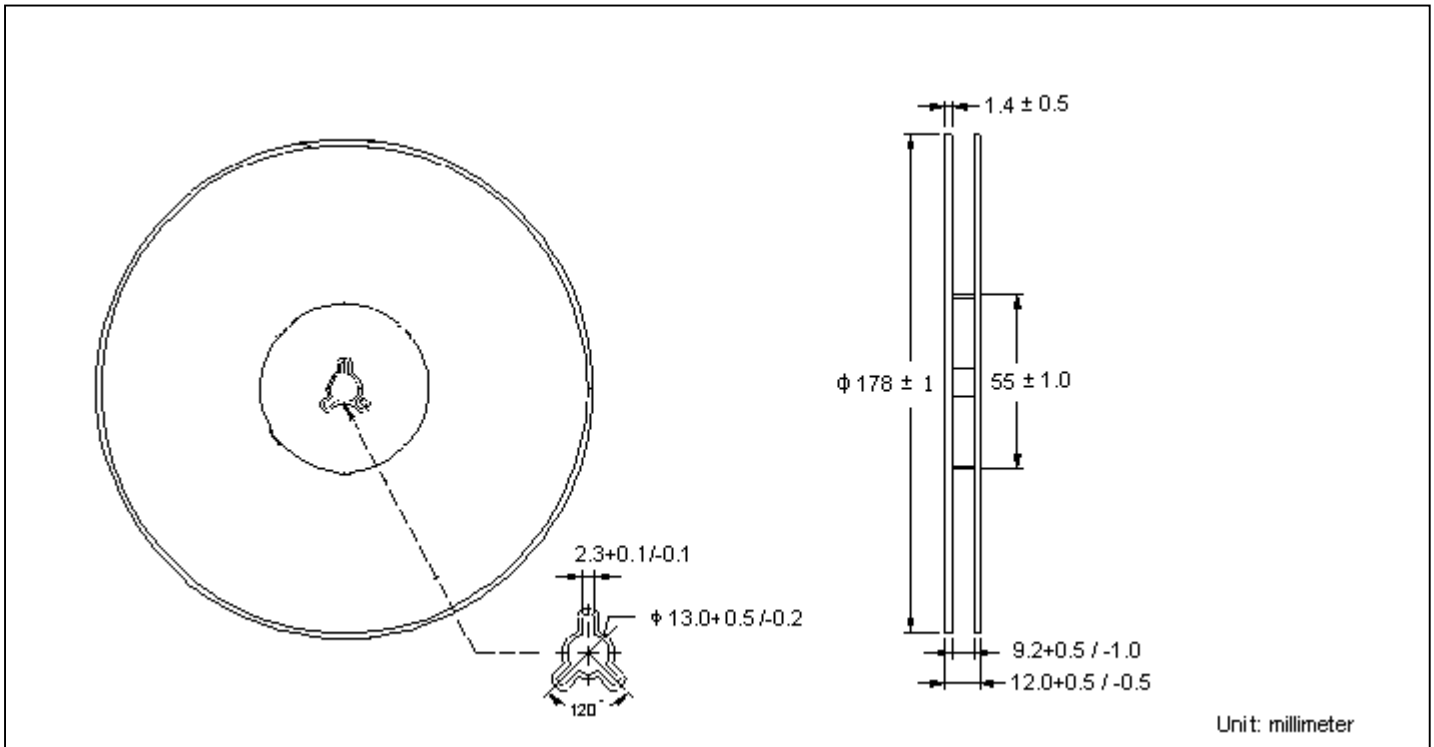
Power Derating Curve



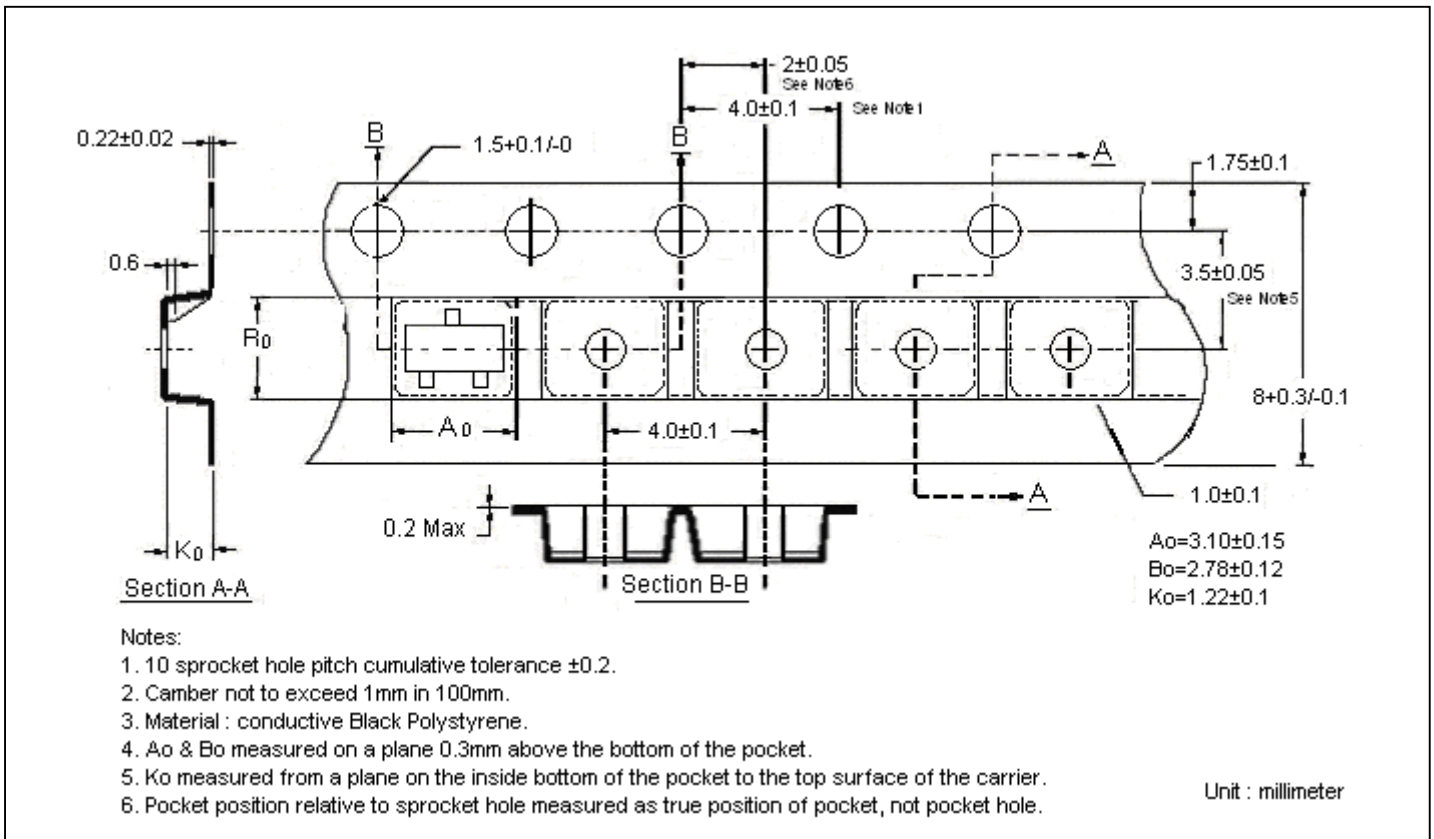
Transient Thermal Response Curves



**Reel Dimension**

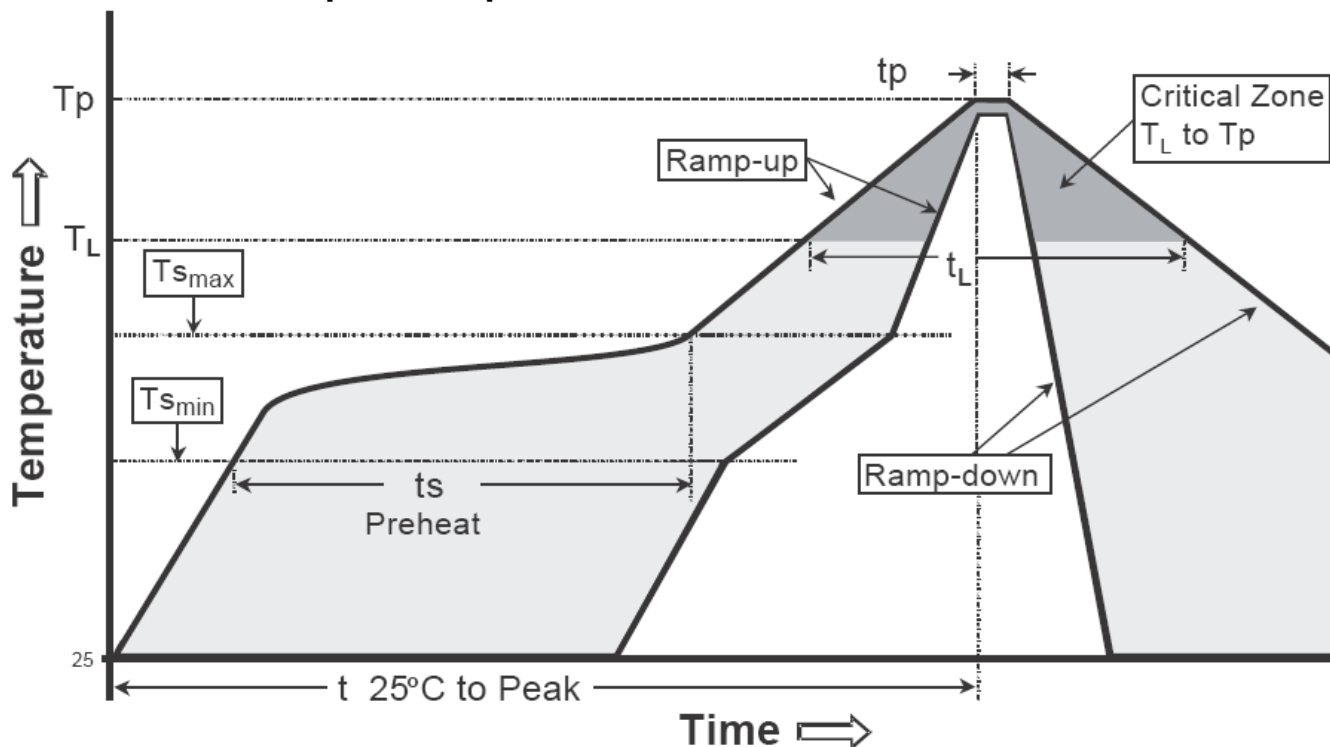


**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

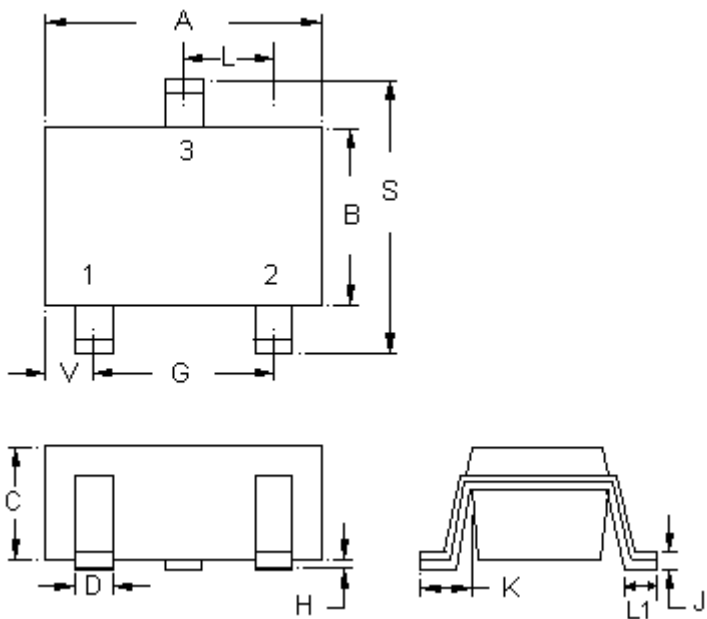
**Recommended temperature profile for IR reflow**


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

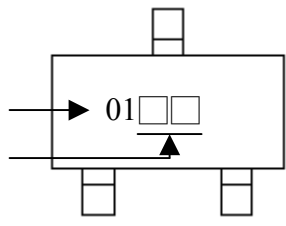


**SOT-23 Dimension**



The diagram shows four views of the SOT-23 package: a top view with dimensions A, L, B, S, 1, 2, 3, V, and G; a side view with dimensions C, D, H, and J; a perspective view with dimensions K, L1, and L2; and a bottom view with dimension J.

**Marking:**



Device Code → 01 □ □  
 Date Code ▲

3-Lead SOT-23 Plastic Surface Mounted Package  
 CYStek Package Code: N3

Style: Pin 1.Gate 2.Source 3.Drain

**Date Code Rule :**  
 First code : Year code, the last digit of Christian year  
 Second code : Month code, 1→Jan, 2→Feb, 3→Mar, ..., 9→Sep, A→Oct, B→Nov, C→Dec

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0032	0.0079	0.08	0.20
B	0.0472	0.0669	1.20	1.70	K	0.0118	0.0266	0.30	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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