N-Channel Enhancement Mode Power MOSFET

MTN10N70EA

BV_{DSS} : 770V @Tj=150℃
$R_{DS(ON)}$: 0.92Ω
I_D : 9.5A

Description

The MTN10N70EA is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.
The SOT-82 package is universally preferred for all commercial-industrial applications

Features

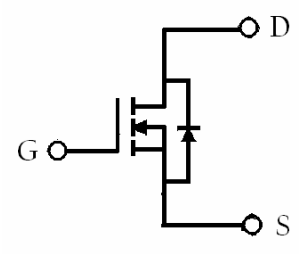
- BV_{DSS}=770V typically @ Tj=150℃
- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- RoHS compliant package

Applications

- Power Factor Correction
- LCD TV Power
- Full and Half Bridge Power

Symbol

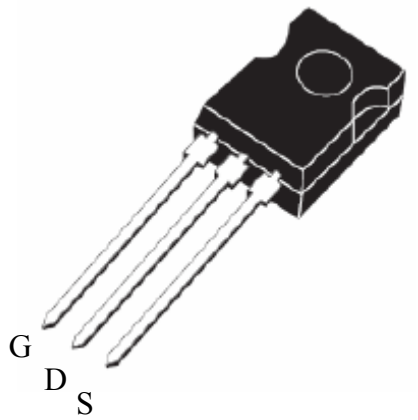
MTN10N70EA



G：Gate
D：Drain
S：Source

Outline

SOT-82



Absolute Maximum Ratings (T_C=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage (Note 1)	V_{DS}	700	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current	I_D	9.5*	A
Continuous Drain Current @T_C=100°C	I_D	5.7*	A
Pulsed Drain Current @ V_{GS}=10V (Note 2)	I_{DM}	38*	A
Single Pulse Avalanche Energy @ L=4.3mH, I_D=10 Amps, V_{DD}=50V	E_{AS}	237	mJ
Repetitive Avalanche Energy	E_{AR}	5	
Peak Diode Recovery dv/dt (Note 3)	dv/dt	3.0	V/ns
Maximum Temperature for Soldering @ Lead at 0.063 in(1.6mm) from case for 10 seconds	T_L	300	°C
Maximum Temperature for Soldering @ Package Body for 10 seconds	T_{PKG}	260	°C
Total Power Dissipation (T_C=25℃)	Pd	50	W
Linear Derating Factor		0.4	W/°C
Operating Junction and Storage Temperature	Tj, Tstg	-55~+150	°C

*Drain current limited by maximum junction temperature

Note : 1. TJ=+25℃ to +150℃.

2. Repetitive rating; pulse width limited by maximum junction temperature.

3. I_{SD}≤10A, dI/dt≤100A/μs, V_{DD}≤BV_{DSS}, T_J=+150℃.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j\text{-}c}$	2.5	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j\text{-}a}$	100	°C/W

Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	700	-	-	V	V_{GS}=0, I_D=250μA
$\Delta BV_{DSS}/\Delta Tj$	-	0.63	-	V/°C	Reference to 25°C, I_D=250μA
$V_{GS(th)}$	2.0	-	4.0	V	V_{DS} = V_{GS}, I_D=250μA
*G_{FS}	-	6.8	-	S	V_{DS} =15V, I_D=5A
I_{GSS}	-	-	±100	nA	V_{GS}=±30
I_{DSS}	-	-	10	μA	V_{DS} =650V, V_{GS} =0
I_{DSS}	-	-	250	μA	V_{DS} =520V, V_{GS} =0, Tj=125°C
*$R_{DS(ON)}$	-	0.87	0.92	Ω	V_{GS} =10V, I_D=6A
Dynamic					
*Qg	-	39	-	nC	I_D=9.5A, V_{DD}=300V, V_{GS}=10V
*Qgs	-	9.5	-		
*Qgd	-	17.6	-		
*$t_{d(ON)}$	-	19	-	ns	V_{DD}=300V, I_D=9.5A, V_{GS}=10V, R_G=9.1Ω
*tr	-	16	-		
*$t_{d(OFF)}$	-	49	-		
*t_f	-	16	-		
Ciss	-	1882	-	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Coss	-	170	-		
Crss	-	20	-		
Source-Drain Diode					
*V_{SD}	-	-	1.5	V	I_S=9.5A, V_{GS}=0V
*I_S	-	-	9.5	A	V_D=V_G=0, V_S=1.3V
*I_{SM}	-	-	38		
*trr	-	345	530	ns	V_{GS}=0, I_F=9.5A, dI/dt=100A/μs
*Qrr	-	2.8	4.4	μC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

Device	Package	Shipping	Marking
MTN10N70EA	SOT-82 (RoHS compliant)	250 pcs/bag, 10 bags/box, 10 boxes / carton	10N70

Characteristic Curves

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

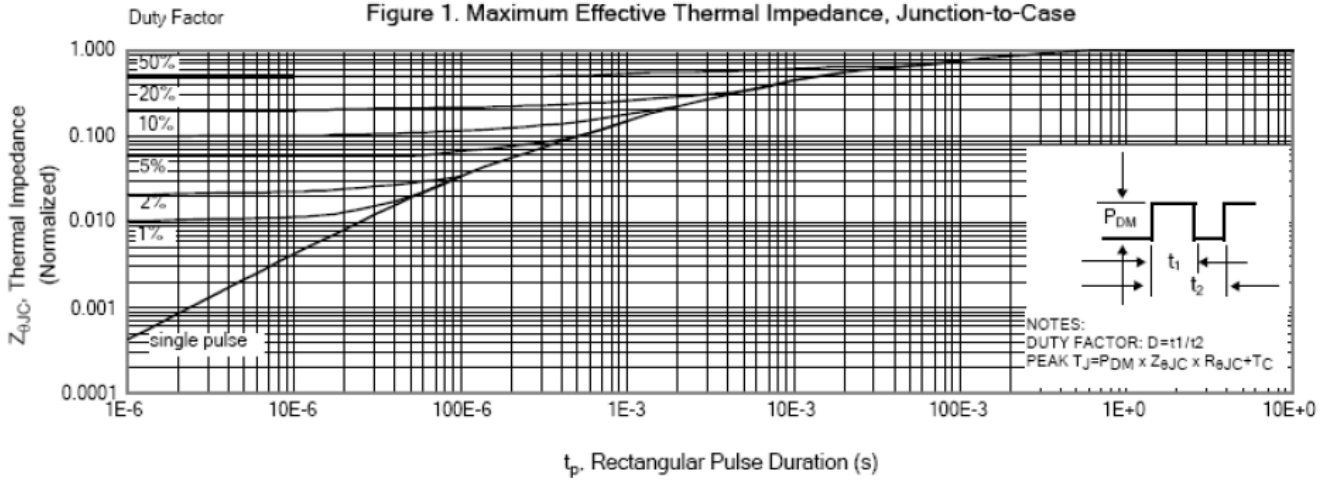


Figure 2. Maximum Power Dissipation vs Case Temperature

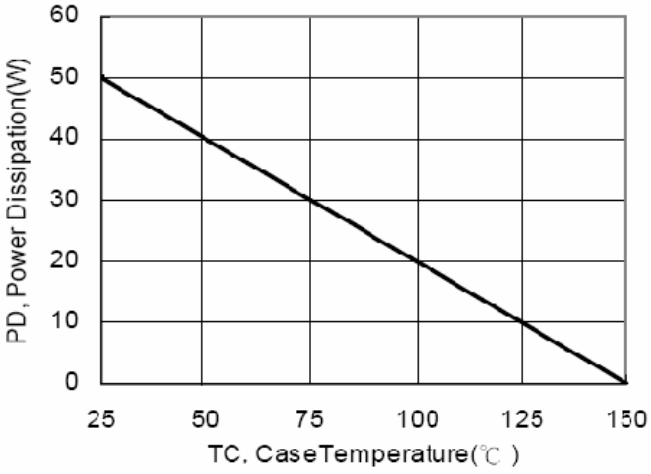


Figure 3. Maximum Continuous Drain Current vs Case Temperature

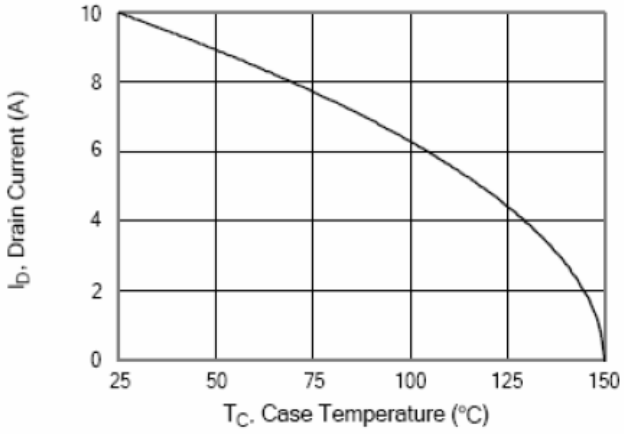


Figure 4. Typical Output Characteristics

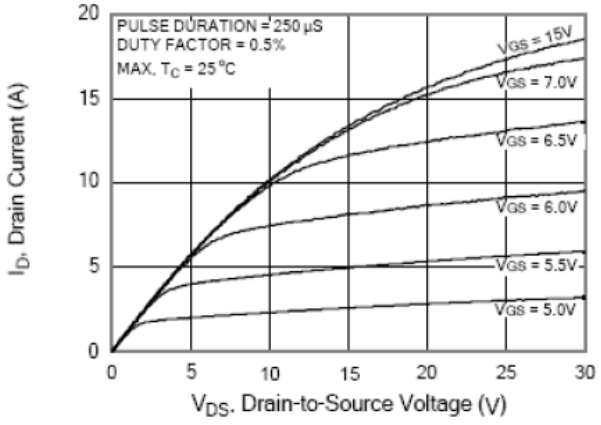
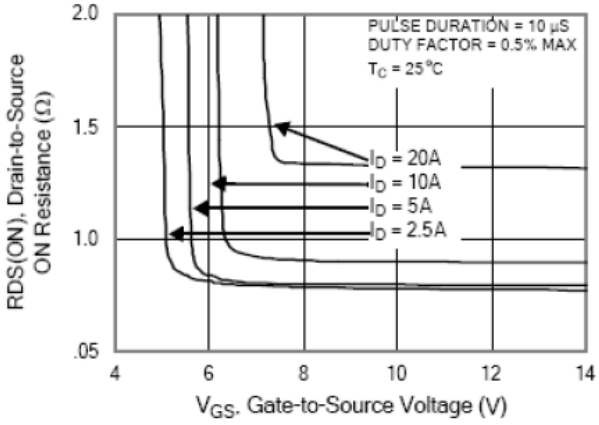


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current



Characteristic Curves(Cont.)

Figure 6. Maximum Peak Current Capability

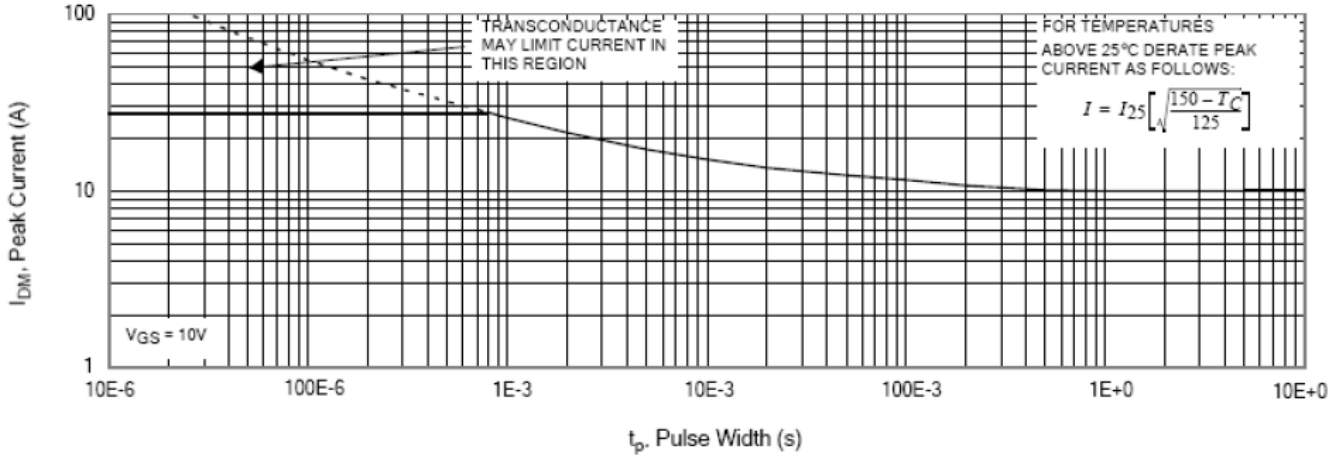


Figure 7. Typical Transfer Characteristics

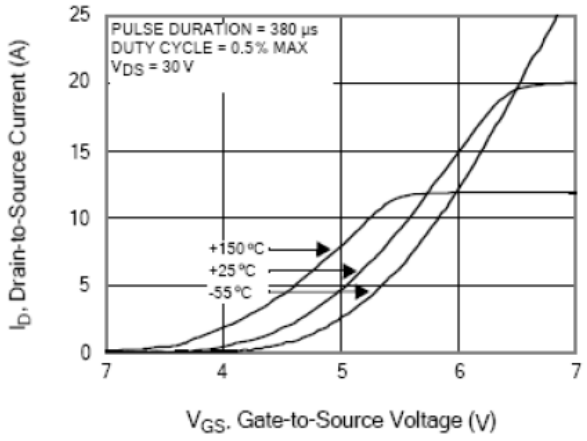


Figure 8. Unclamped Inductive Switching Capability

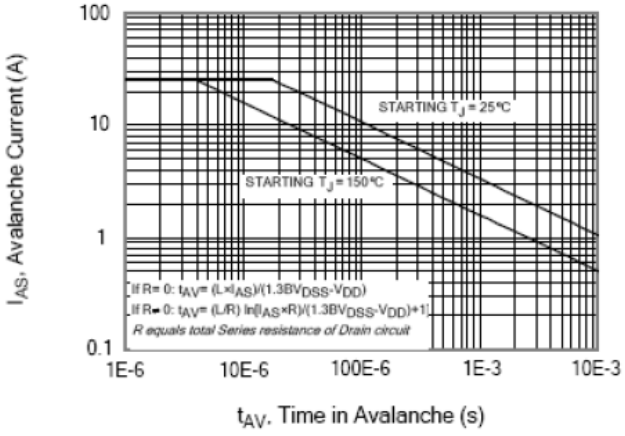


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

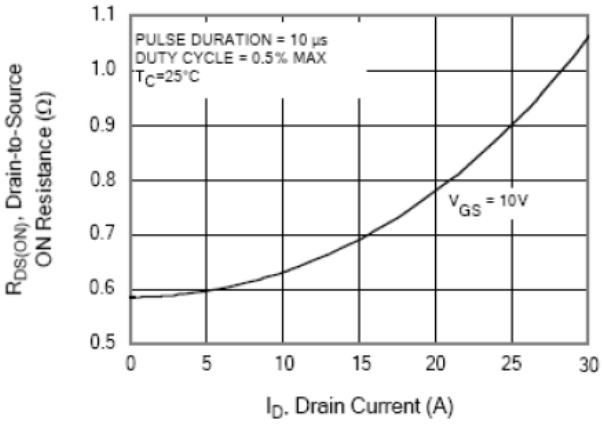
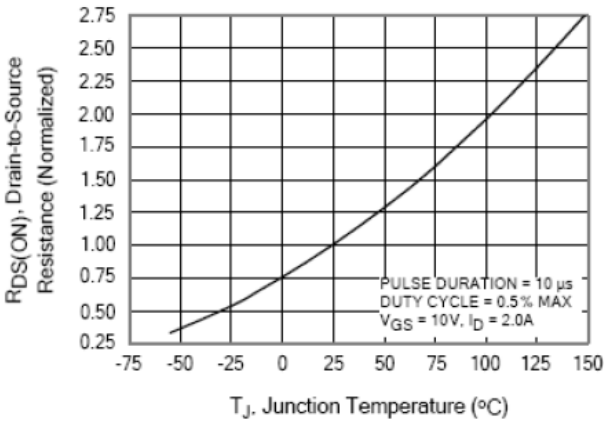


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature



Characteristic Curves(Cont.)

Figure 11. Typical Breakdown Voltage vs Junction Temperature

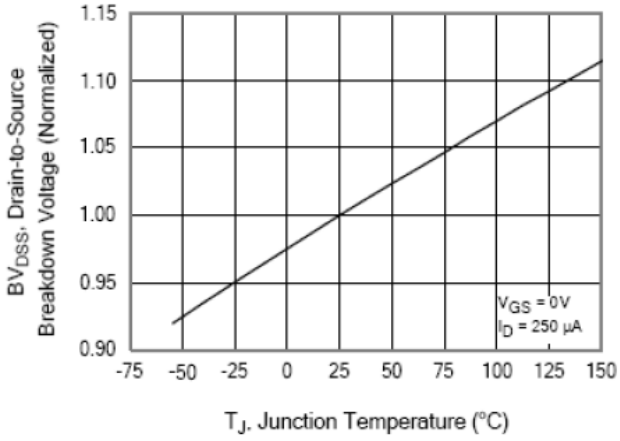


Figure 12. Typical Threshold Voltage vs Junction Temperature

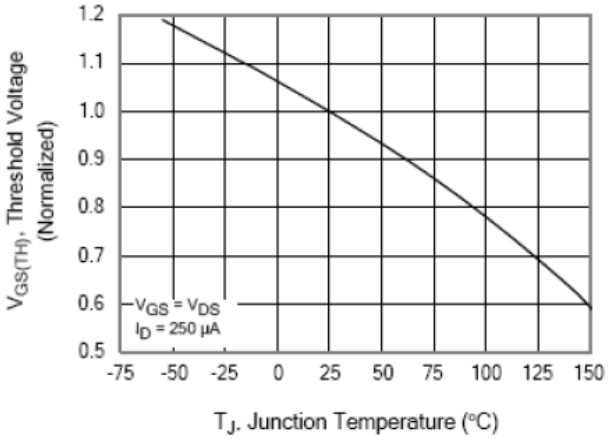


Figure 13. Maximum Forward Bias Safe Operating Area

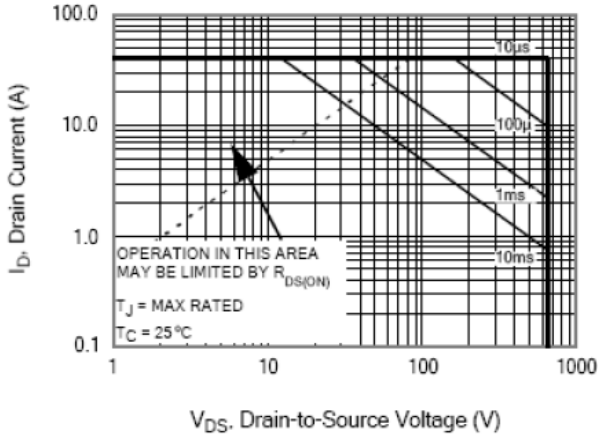


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

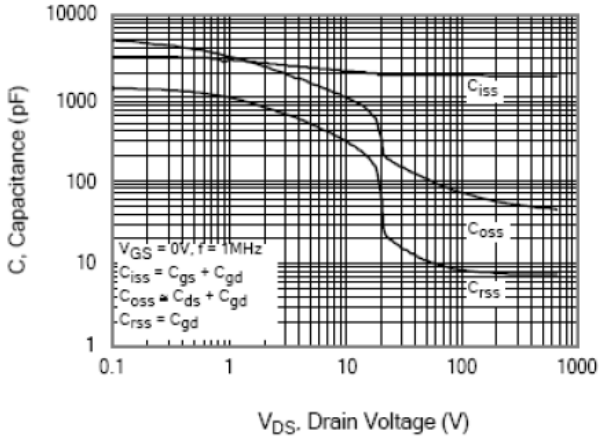


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

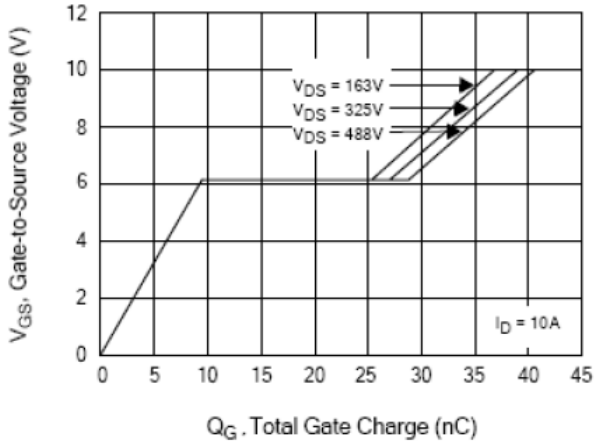
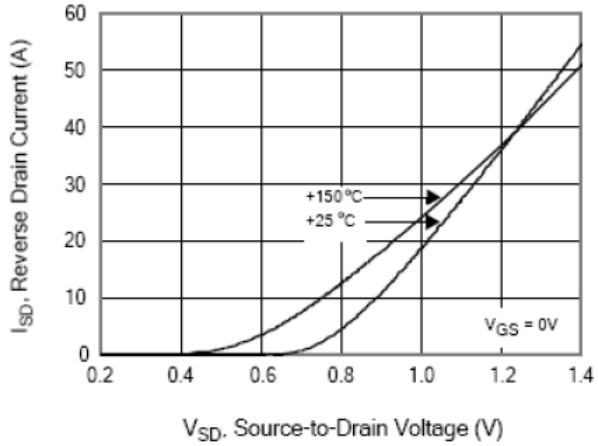


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuit and Waveforms

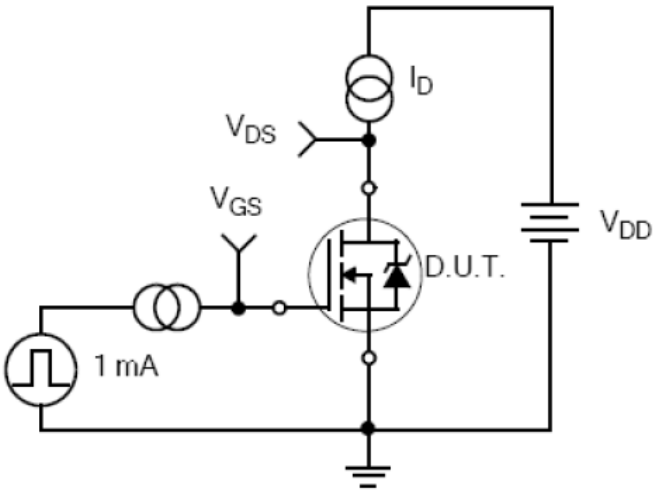


Figure 17. Gate Charge Test Circuit

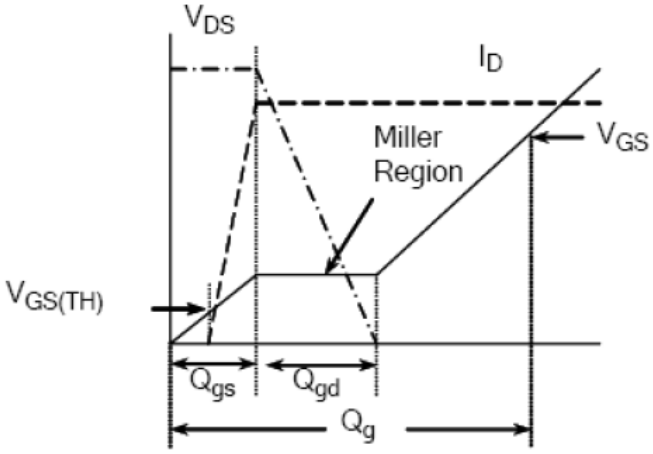


Figure 18. Gate Charge Waveform

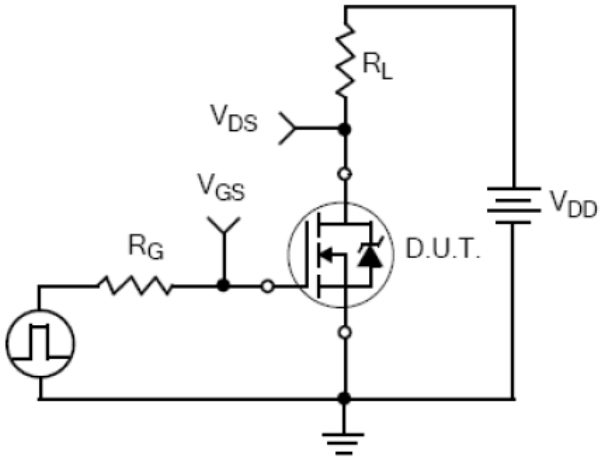


Figure 19. Resistive Switching Test Circuit

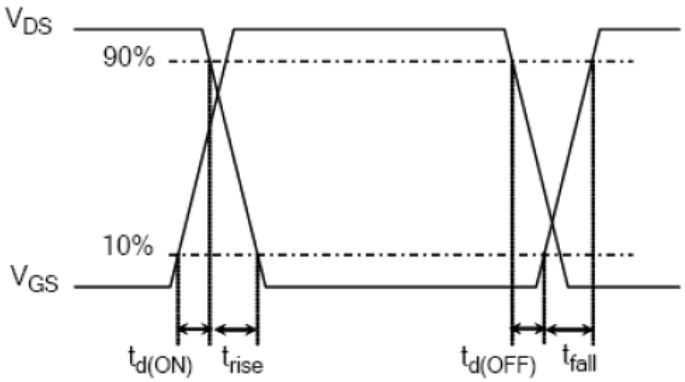


Figure 20. Resistive Switching Waveforms

Test Circuit and Waveforms(Cont.)

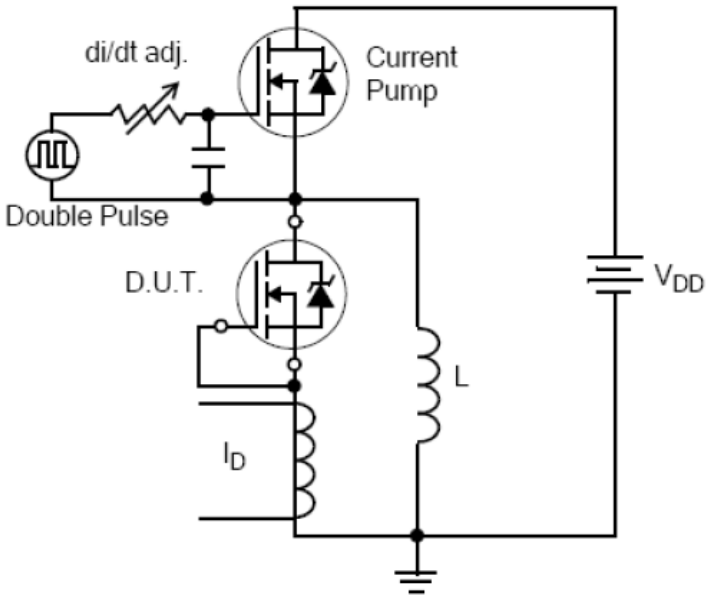


Figure 21. Diode Reverse Recovery Test Circuit

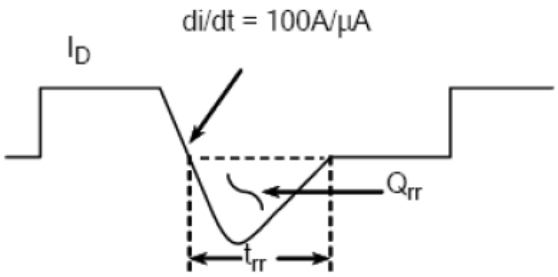


Figure 22. Diode Reverse Recovery Waveform

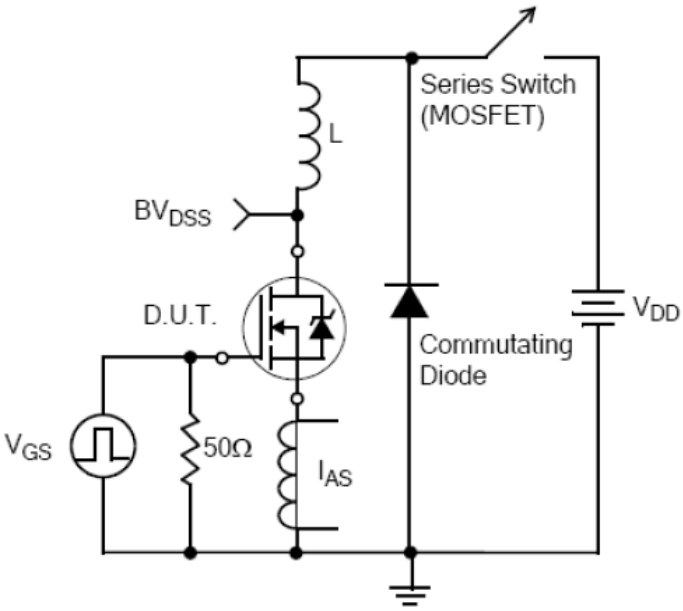
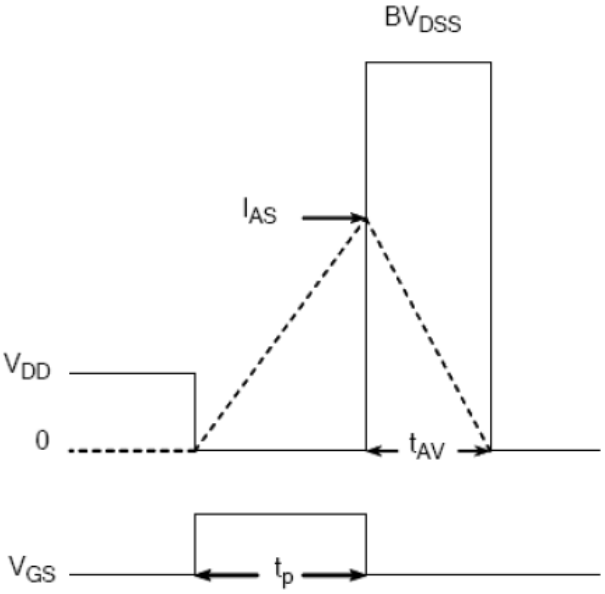


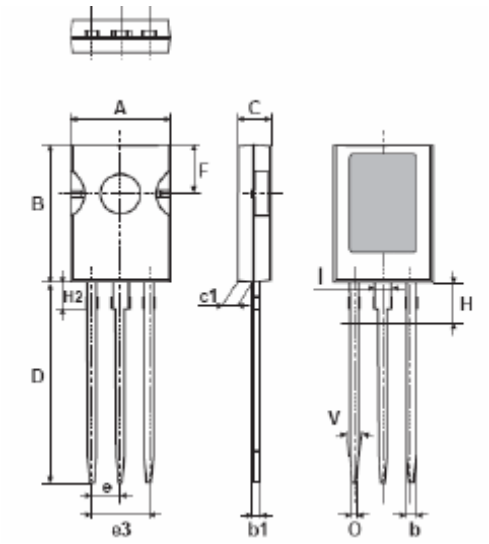
Figure 23. Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

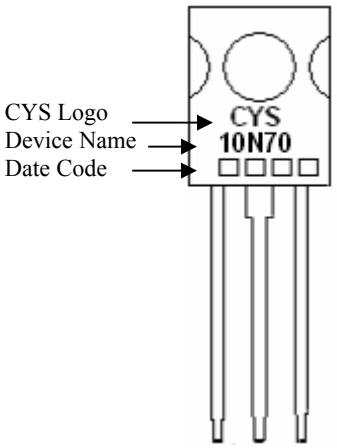
Figure 24. Unclamped Inductive Switching Waveforms

SOT- 82 Dimension



3-Lead SOT-82 Plastic Package
CYStek Package Code: EA

Marking:



Style: Pin 1.Gate 2.Drain 3.Source
4.Drain

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.291	0.307	7.4	7.8	e3	0.163	0.183	4.15	4.65
B	0.413	0.425	10.5	10.8	F	*0.149		*3.8	
b	0.028	0.035	0.7	0.9	H	*0.100		*2.54	
b1	0.019	0.029	0.49	0.75	H2	*0.084		*2.15	
C	0.094	0.106	2.4	2.7	I	*0.05		*1.27	
c1	0.039	0.051	1.0	1.3	O	*0.012		*0.3	
D	0.606	0.630	15.4	16.0	V	*10°		*10°	
e	*0.086		*2.2						

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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