N-Channel Enhancement Mode Power MOSFET

MTN10N65FPG

BV_{DSS} : 650V
$R_{DS(ON)}$: 0.82Ω
I_D : 10A

Description

The MTN10N65FPG is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.
The TO-220FP package is universally preferred for all commercial-industrial applications

Features

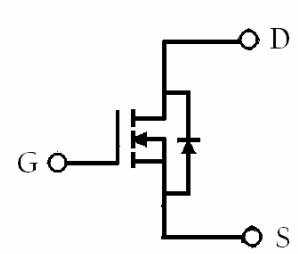
- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Insulating package, front/back side insulating voltage=2500V(AC)
- Pb-free lead plating and halogen-free package

Applications

- Power Factor Correction
- LCD TV Power
- Full and Half Bridge Power

Symbol

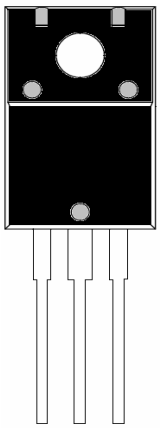
MTN10N65FPG



G：Gate
D：Drain
S：Source

Outline

TO-220FP



G D S

Absolute Maximum Ratings (T_C=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage (Note 1)	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current	I_D	10*	A
Continuous Drain Current @T_C=100°C	I_D	6	A
Pulsed Drain Current @ V_{GS}=10V (Note 2)	I_{DM}	40*	A
Single Pulse Avalanche Energy @ L=4.3mH, I_D=10 Amps, V_{DD}=50V	E_{AS}	237	mJ
Repetitive Avalanche Energy	E_{AR}	5	
Peak Diode Recovery dv/dt (Note 3)	dv/dt	3.0	V/ns
Maximum Temperature for Soldering @ Lead at 0.063 in(1.6mm) from case for 10 seconds	T_L	300	°C
Maximum Temperature for Soldering @ Package Body for 10 seconds	T_{PKG}	260	°C
Total Power Dissipation (T_C=25℃)	Pd	50	W
Linear Derating Factor		0.4	W/°C
Operating Junction and Storage Temperature	Tj, Tstg	-55~+150	°C

*Drain current limited by maximum junction temperature

Note : 1. TJ=+25℃ to +150℃.
2. Repetitive rating; pulse width limited by maximum junction temperature.
3. ISD≤10A, dI/dt≤100A/μs, VDD≤BVDSS, TJ=+150℃.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j\text{-}c}$	2.5	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j\text{-}a}$	100	°C/W

Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	650	-	-	V	V_{GS}=0, I_D=250μA
$\Delta BV_{DSS}/\Delta Tj$	-	0.6	-	V/°C	Reference to 25°C, I_D=250μA
$V_{GS(th)}$	2.0	-	4.0	V	V_{DS} = V_{GS}, I_D=250μA
*G_{FS}	-	6.8	-	S	V_{DS} =15V, I_D=5A
I_{GSS}	-	-	±100	nA	V_{GS}=±30
I_{DSS}	-	-	25	μA	V_{DS} =650V, V_{GS} =0
I_{DSS}	-	-	250	μA	V_{DS} =520V, V_{GS} =0, Tj=125°C
*$R_{DS(ON)}$	-	0.75	0.82	Ω	V_{GS} =10V, I_D=6A
Dynamic					
*Qg	-	53	-	nC	I_D=10A, V_{DD}=325V, V_{GS}=10V
*Qgs	-	10.7	-		
*Qgd	-	22.3	-		
*$t_{d(ON)}$	-	19	-	ns	V_{DD}=325V, I_D=10A, V_{GS}=10V, R_G=9.1Ω
*tr	-	16	-		
*$t_{d(OFF)}$	-	49	-		
*t_f	-	16	-		
Ciss	-	2516	-	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Coss	-	182.2	-		
Crss	-	71	-		
Source-Drain Diode					
*V_{SD}	-	-	1.5	V	I_S=10A, V_{GS}=0V
*I_S	-	-	10	A	V_D=V_G=0, V_S=1.3V
*I_{SM}	-	-	40		
*trr	-	352	528	ns	V_{GS}=0, I_F=10A, dI/dt=100A/μs
*Qrr	-	2.9	4.35	μC	

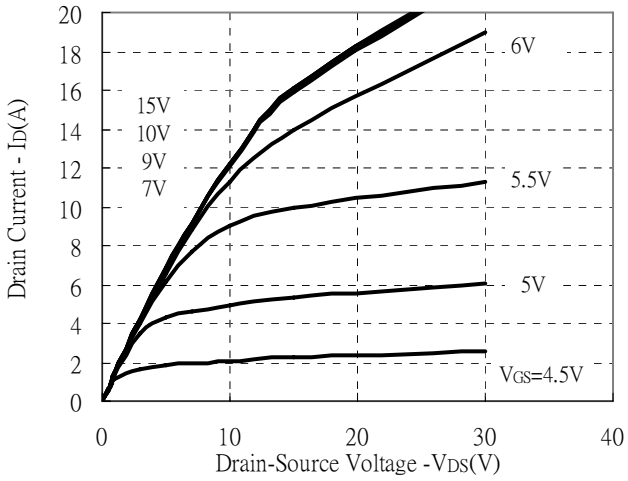
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

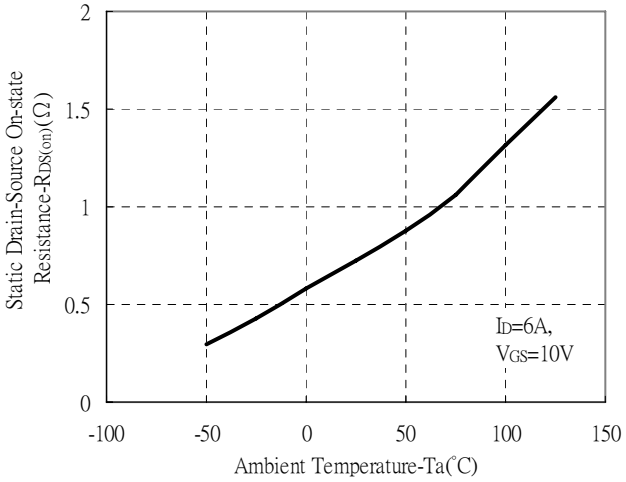
Device	Package	Shipping
MTN10N65FPG	TO-220FP (Pb-free lead plating and halogen-free package)	50 pcs/tube

Typical Characteristics

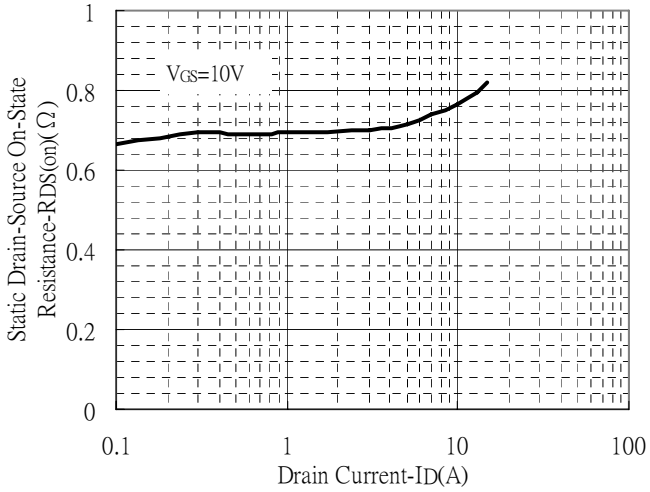
Typical Output Characteristics



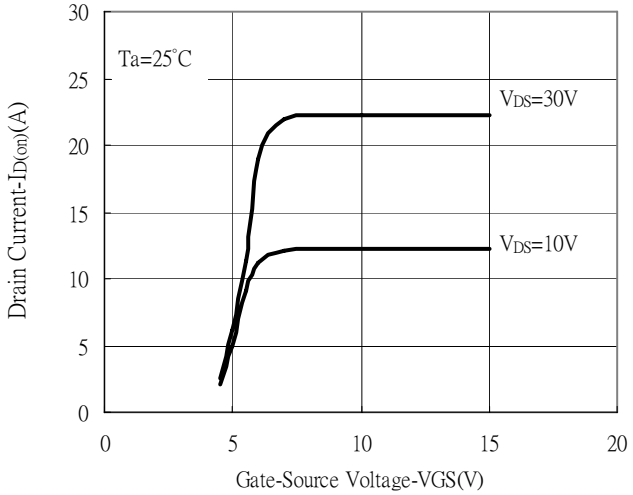
Static Drain-Source On-resistance vs Ambient Temperature



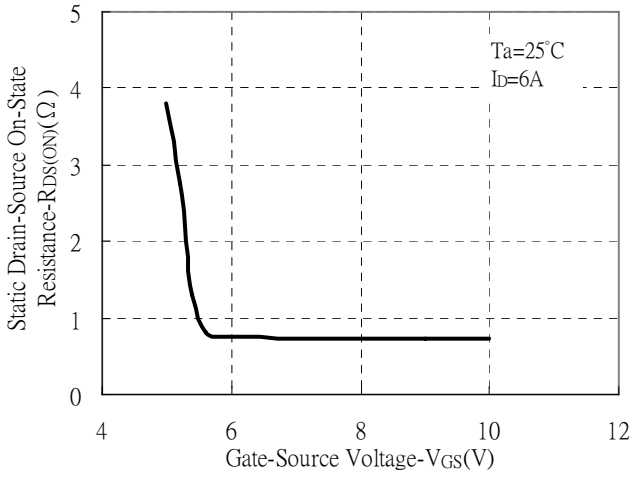
Static Drain-Source On-State resistance vs Drain Current



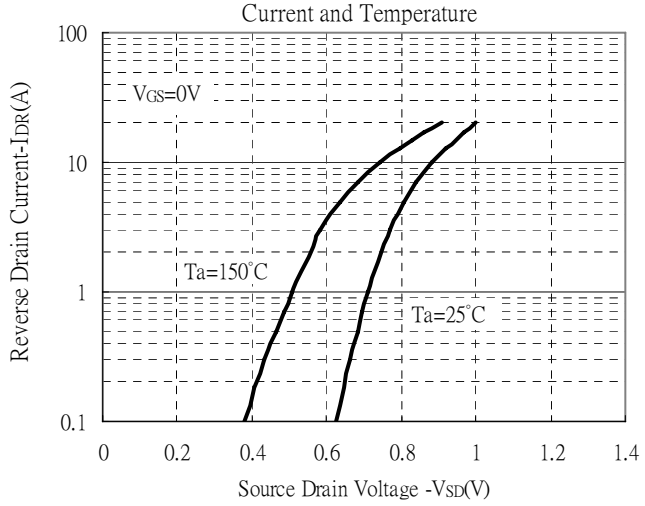
Drain Current vs Gate-Source Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

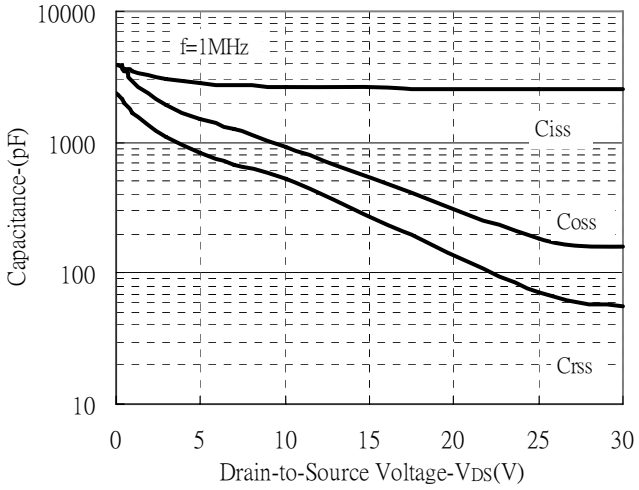


Body Diode Forward Voltage Variation vs Source Current and Temperature

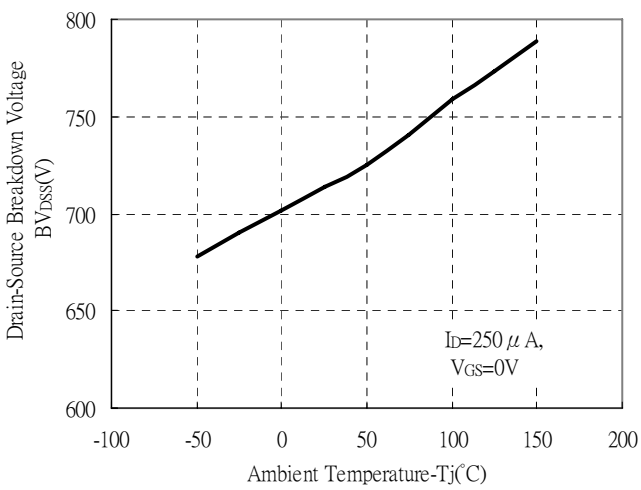


Characteristic Curves(Cont.)

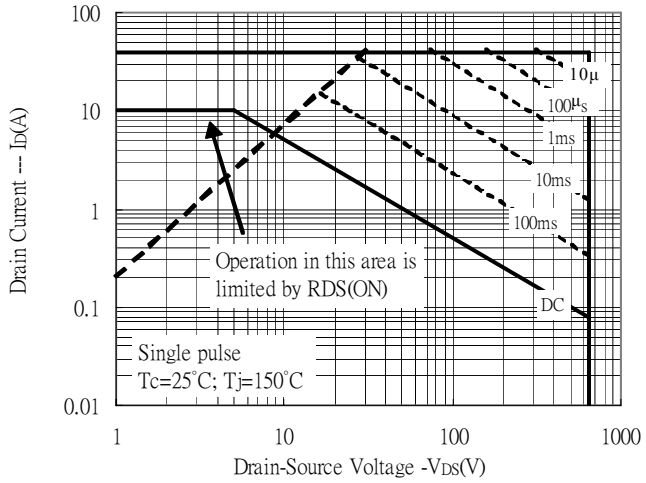
Capacitance vs Reverse Voltage



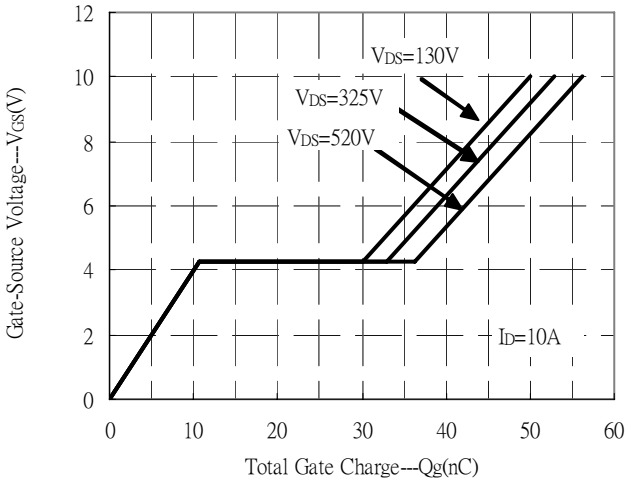
Brekdown Voltage vs Ambient Temperature



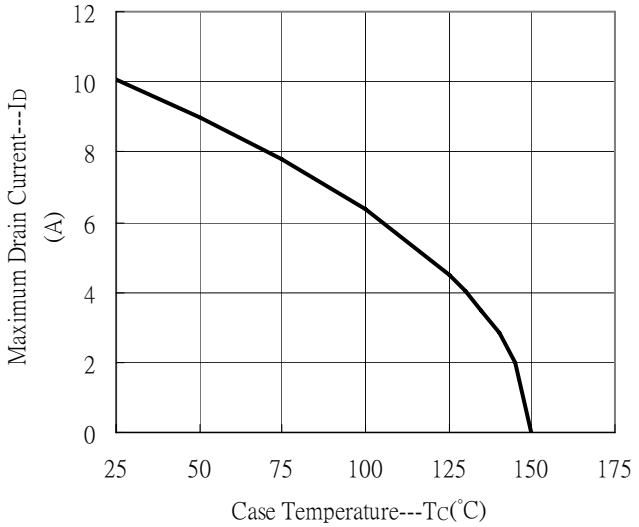
Maximum Safe Operating Area



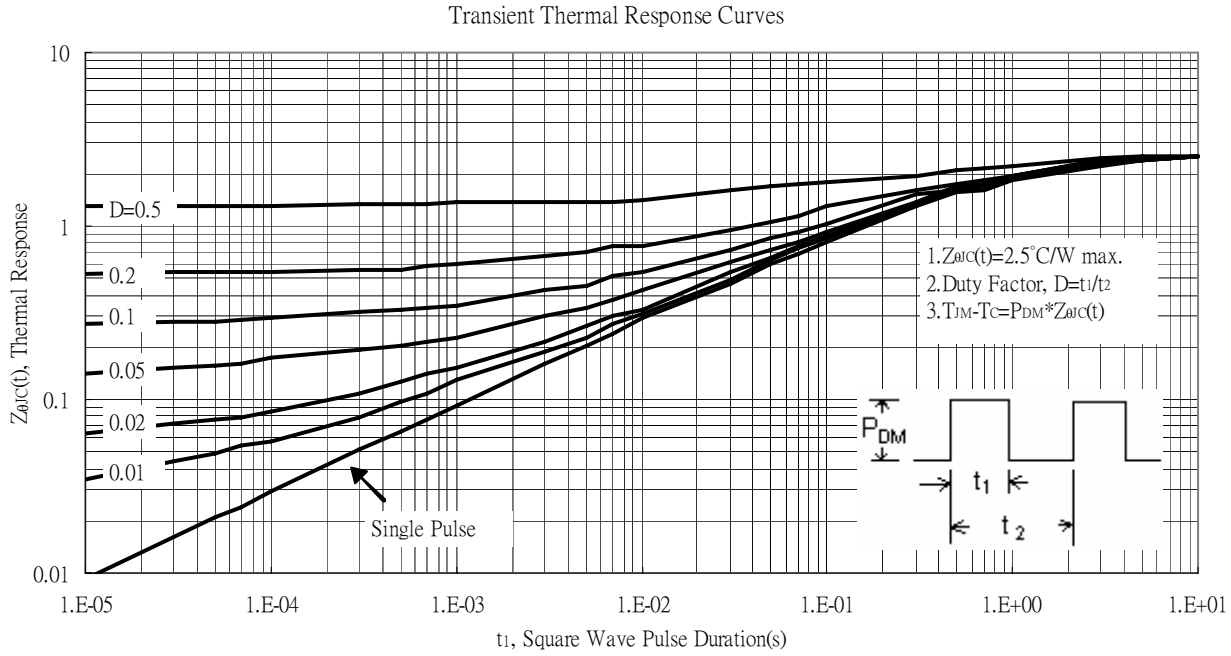
Gate Charge Characteristics



Maximum Drain Current vs Case Temperature



Typical Characteristics(Cont.)



Test Circuit and Waveforms

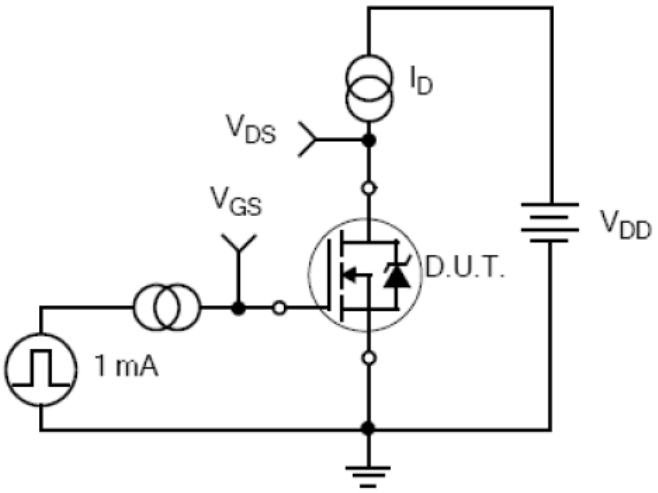


Figure 17. Gate Charge Test Circuit

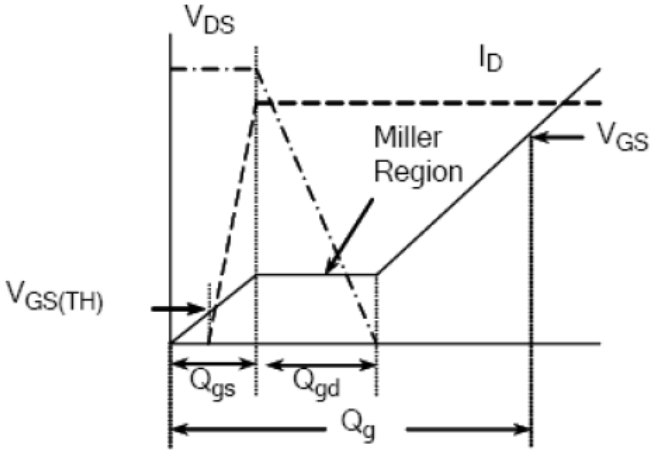


Figure 18. Gate Charge Waveform

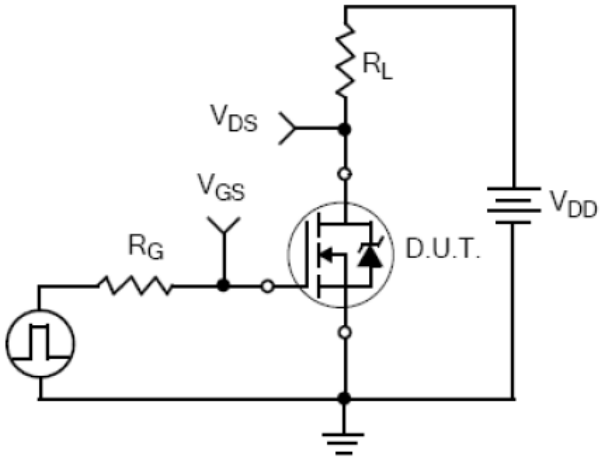


Figure 19. Resistive Switching Test Circuit

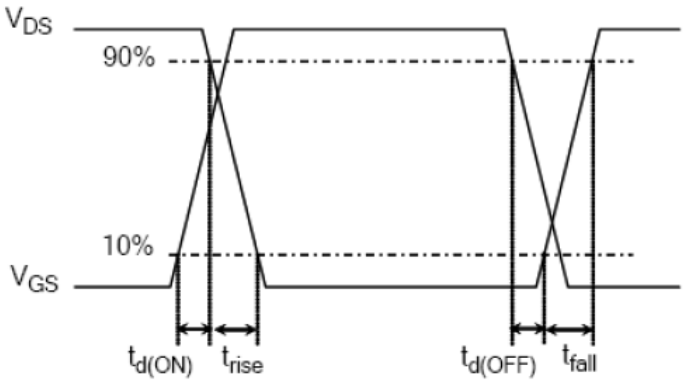


Figure 20. Resistive Switching Waveforms

Test Circuit and Waveforms(Cont.)

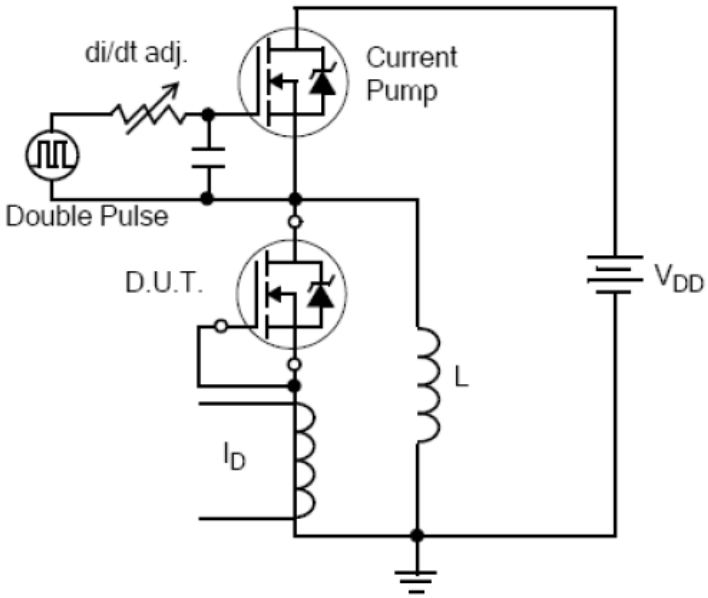


Figure 21. Diode Reverse Recovery Test Circuit

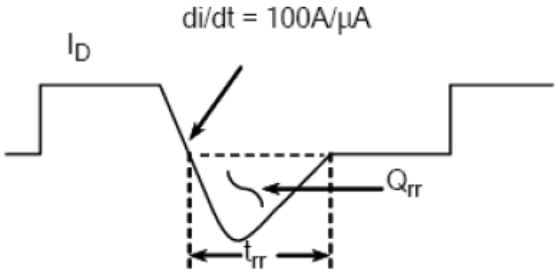


Figure 22. Diode Reverse Recovery Waveform

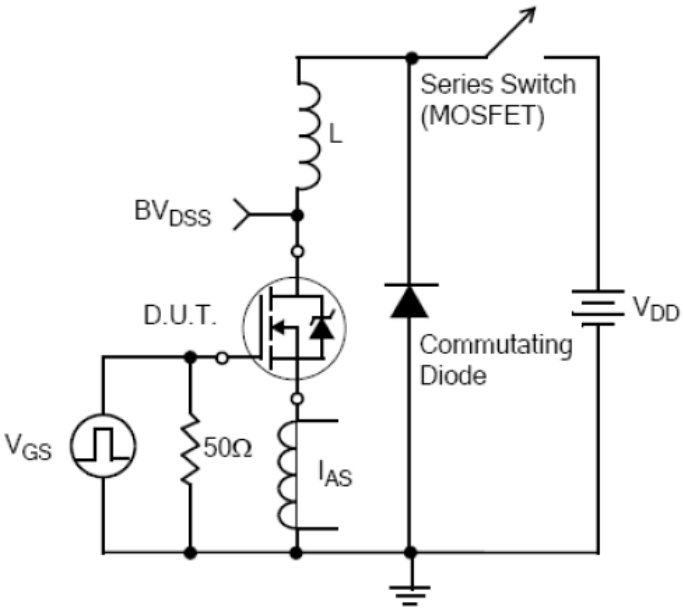
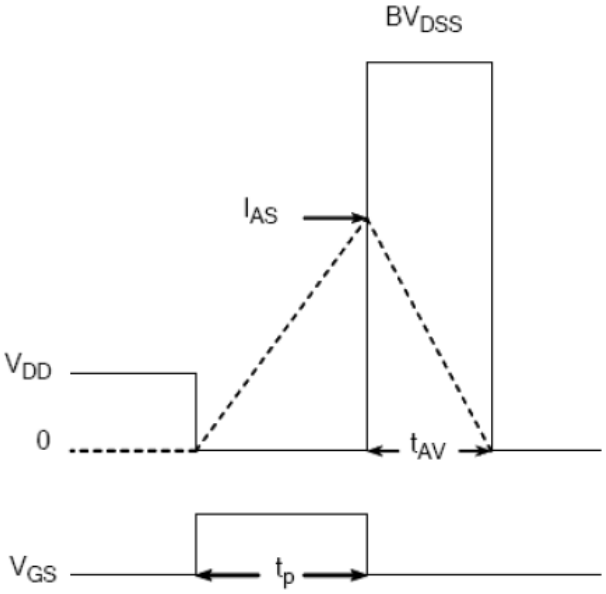


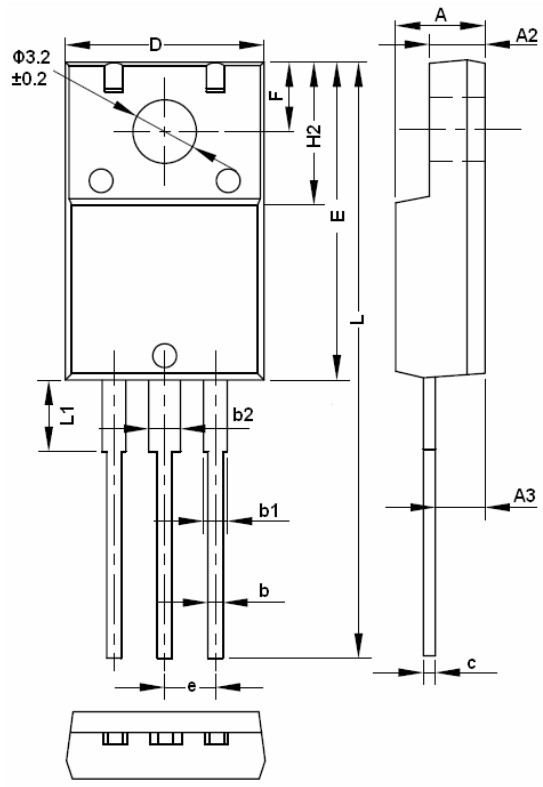
Figure 23. Unclamped Inductive Switching Test Circuit

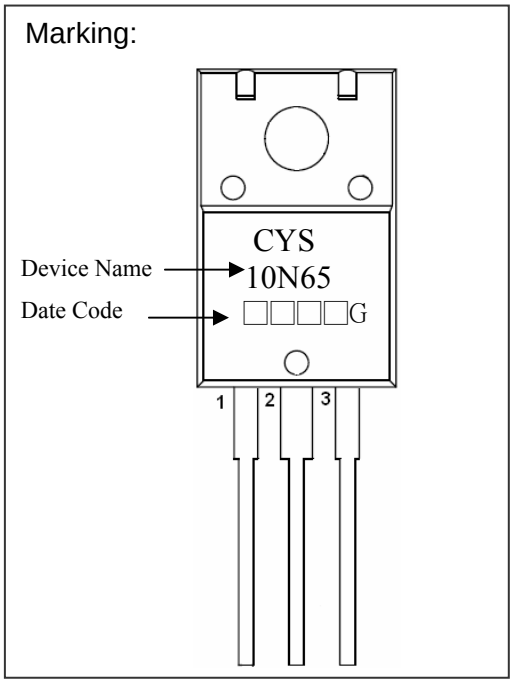


$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure 24. Unclamped Inductive Switching Waveforms

TO-220FP Dimension





Style: Pin 1.Gate 2.Drain 3.Source

3-Lead TO-220FP Plastic Package
CYStek Package Code: FP

*Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	4.20	4.80	0.1654	0.1890	D	9.70	10.30	0.3819	0.4055
A2	2.50	3.10	0.0984	0.1220	E	15.70	16.30	0.6181	0.6417
A3	2.20	2.80	0.0866	0.1102	e	2.35	2.75	0.0925	0.1083
b	0.74	0.78	0.0291	0.0307	F	3.20	3.80	0.1260	0.1496
b1	0.90	1.50	0.0354	0.0591	H2	6.90	7.50	0.2717	0.2953
b2	1.30	1.90	0.0512	0.0748	L	29.20	30.80	1.1496	1.2126
c	0.30	0.90	0.0118	0.0354	L1	3.40	3.80	0.1339	0.1496

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.