



N-Channel Enhancement Mode Power MOSFET MTN4N65FP

BV_{DSS} : 650V
R_{DS(ON)} : 3Ω (typ.)
I_D : 4A

Description

The MTN4N65FP is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-220FP package is universally preferred for all commercial-industrial applications

Features

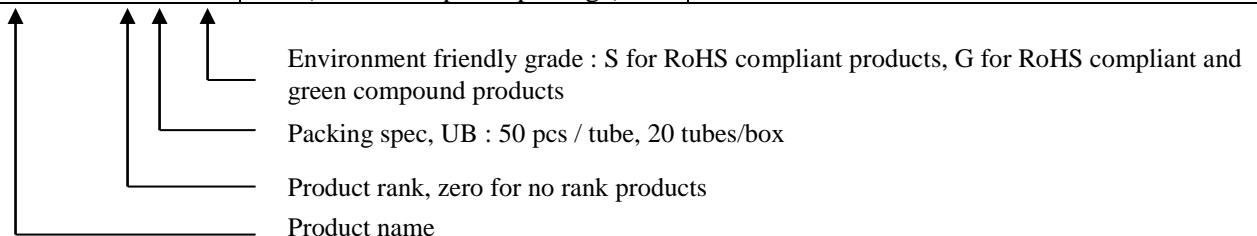
- Low On Resistance
- Simple Drive Requirement
- Fast Switching Characteristic
- Insulating package, front/back side insulating voltage=2500V(AC)
- RoHS compliant package

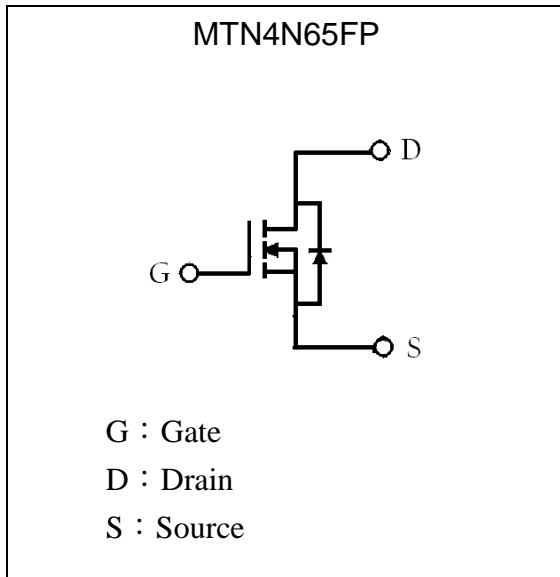
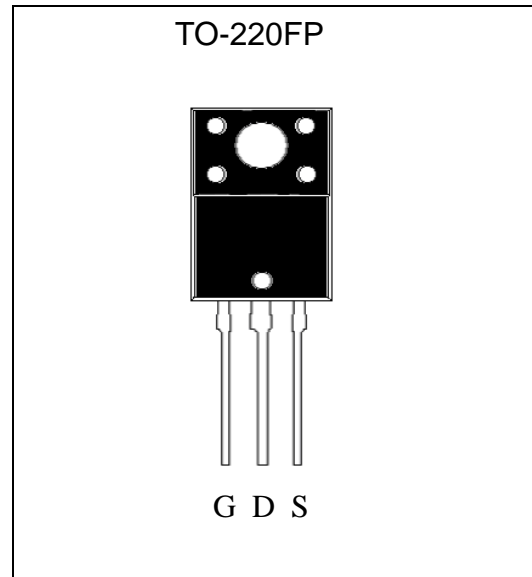
Applications

- Adapter
- Switching Mode Power Supply

Ordering Information

Device	Package	Shipping
MTN4N65FP-0-UB-S	TO-220FP (RoHS compliant package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton



Symbol

Outline

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	4*	A
Continuous Drain Current @ $T_C=100^\circ\text{C}$	I_D	2.4*	A
Pulsed Drain Current @ $V_{GS}=10\text{V}$ (Note 1)	I_{DM}	16*	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	69	mJ
Avalanche Current (Note 1)	I_{AR}	4	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	3.4	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Maximum Temperature for Soldering @ Lead at 0.125 in(0.318mm) from case for 10 seconds	T_L	300	$^\circ\text{C}$
Total Power Dissipation ($T_C=25^\circ\text{C}$)	P_D	34	W
Linear Derating Factor		0.27	W/ $^\circ\text{C}$
Operating Junction and Storage Temperature	T_j, T_{stg}	-55~+150	$^\circ\text{C}$

*Drain current limited by maximum junction temperature

Note : 1.Repetitive rating; pulse width limited by maximum junction temperature.

2. $I_{AS}=4\text{A}$, $V_{DD}=50\text{V}$, $L=8\text{mH}$, $R_G=25\ \Omega$, starting $T_J=+25^\circ\text{C}$.

3. $I_{SD}\leq 4\text{A}$, $dI/dt\leq 100\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, starting $T_J=+25^\circ\text{C}$.



Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	3.68	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	62.5	°C/W

Characteristics (Tj=25°C, unless otherwise specified)

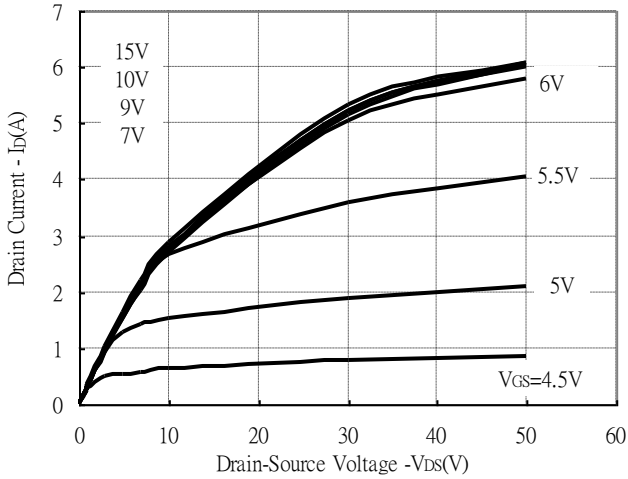
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	650	-	-	V	$V_{GS}=0, I_D=250\mu A, T_j=25^\circ C$
$\Delta BV_{DSS}/\Delta T_j$	-	0.6	-	V/°C	Reference to 25°C, $I_D=250\mu A$
$V_{GS(th)}$	2.0	-	4.0	V	$V_{DS} = V_{GS}, I_D=250\mu A$
* G_{FS}	-	2.3	-	S	$V_{DS} = 15V, I_D=2A$
I_{GSS}	-	-	±100	nA	$V_{GS}=\pm 30$
I_{DSS}	-	-	1	μA	$V_{DS} = 650V, V_{GS} = 0$
	-	-	10	μA	$V_{DS} = 520V, V_{GS} = 0, T_C=125^\circ C$
* $R_{DS(ON)}$	-	3.0	3.5	Ω	$V_{GS} = 10V, I_D=2A$
Dynamic					
* Q_g	-	11	-	nC	$I_D=4A, V_{DD}=520V, V_{GS}=10V$
* Q_{gs}	-	2.6	-		
* Q_{gd}	-	4.6	-		
* $t_{d(ON)}$	-	15	-	ns	$V_{DD}=325V, I_D=4A, V_{GS}=10V, R_G=25\Omega$
* t_r	-	33	-		
* $t_{d(OFF)}$	-	30	-		
* t_f	-	37	-		
C_{iss}	-	568	-	pF	$V_{GS}=0V, V_{DS}=25V, f=1MHz$
C_{oss}	-	51	-		
C_{rSS}	-	9.6	-		
Source-Drain Diode					
* V_{SD}	-	-	1.5	V	$I_S=4A, V_{GS}=0V$
* I_S	-	-	4	A	
* I_{SM}	-	-	16		
* t_{rr}	-	280	-	ns	$V_{GS}=0, I_F=4A, dI/dt=100A/\mu s$
* Q_{rr}	-	2	-	μC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%

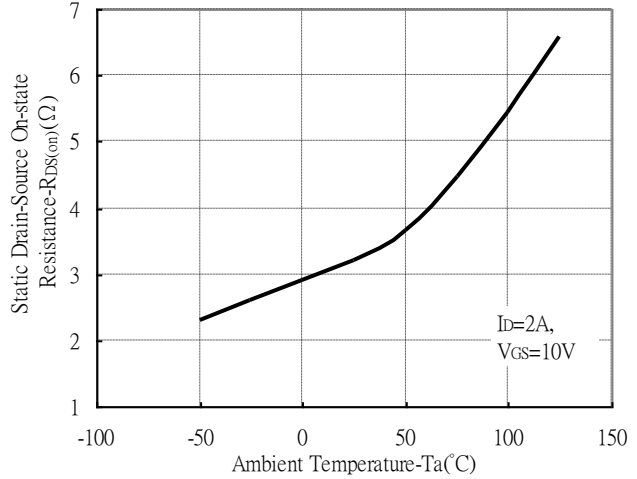


Typical Characteristics

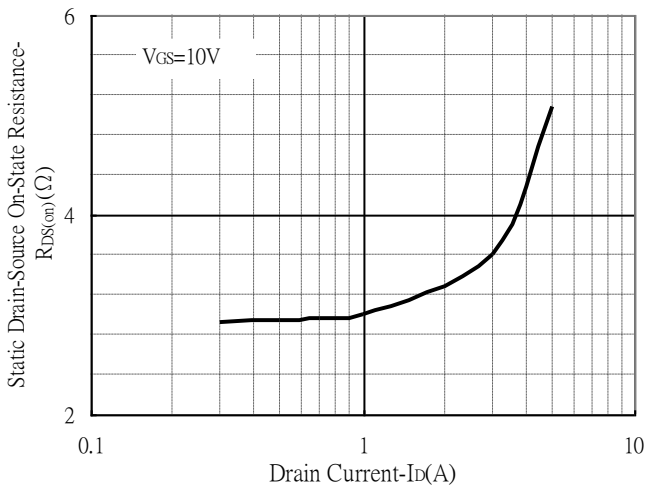
Typical Output Characteristics



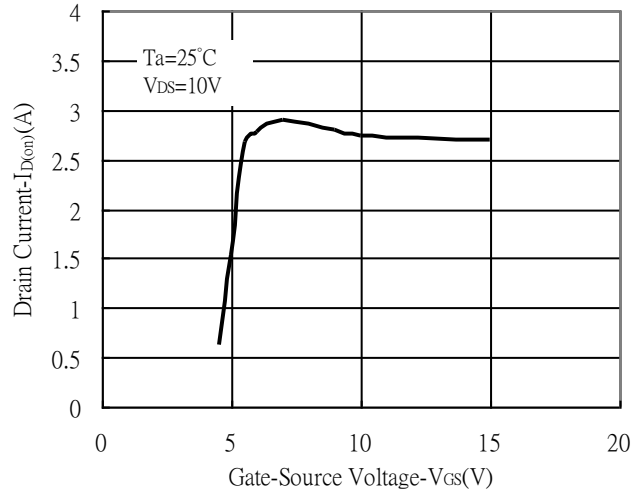
Static Drain-Source On-resistance vs Ambient Temperature



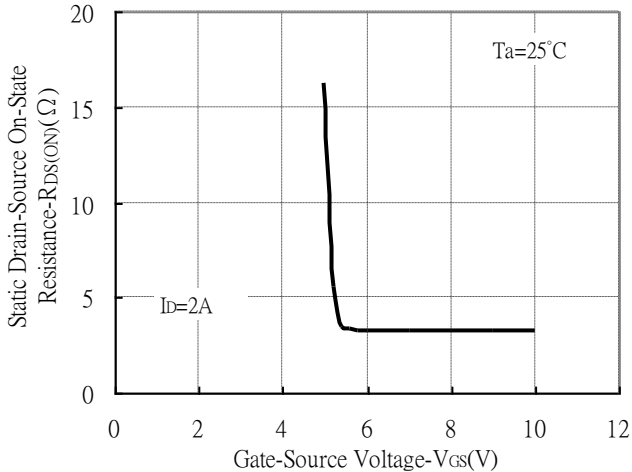
Static Drain-Source On-State resistance vs Drain Current



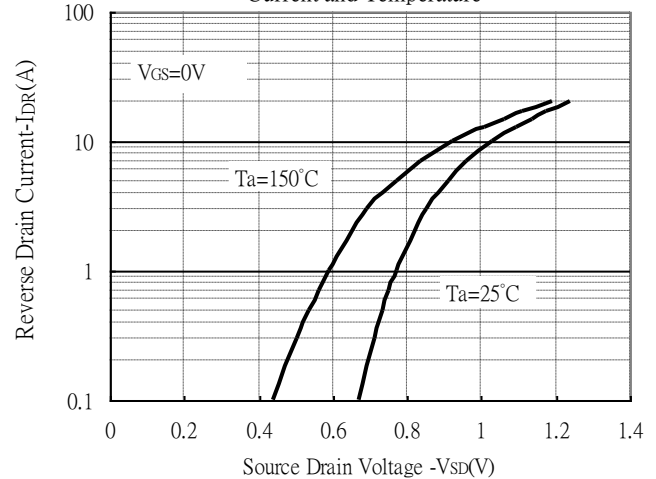
Drain Current vs Gate-Source Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

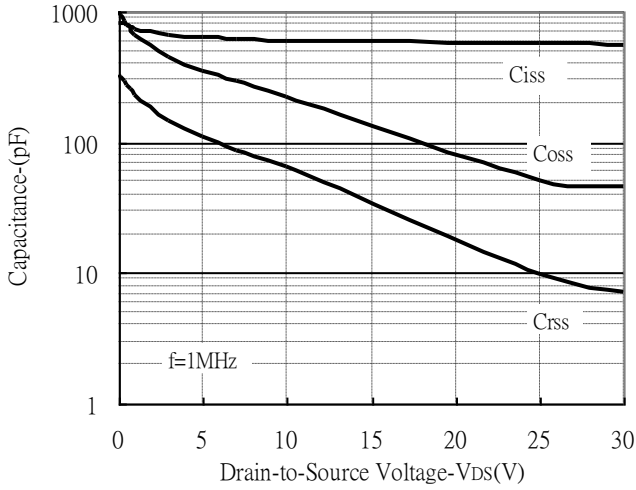


Body Diode Forward Voltage Variation with Source Current and Temperature

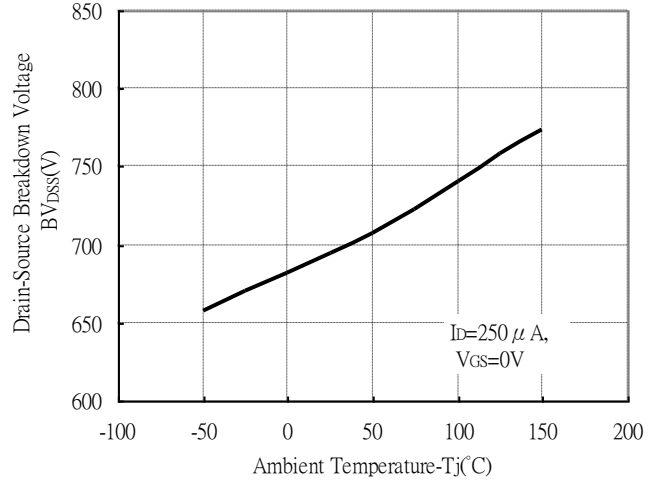


Typical Characteristics(Cont.)

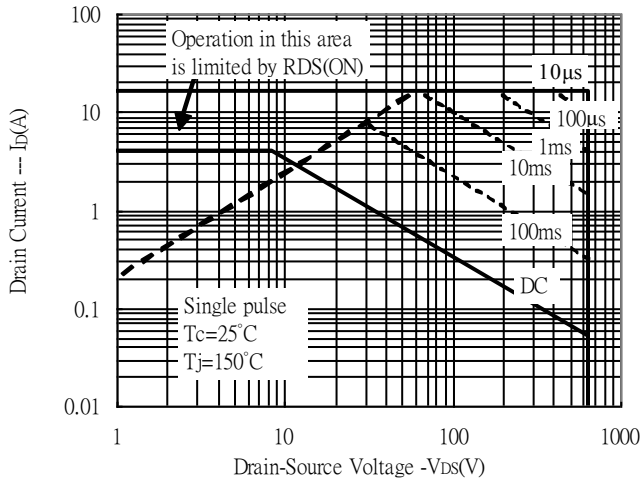
Capacitance vs Reverse Voltage



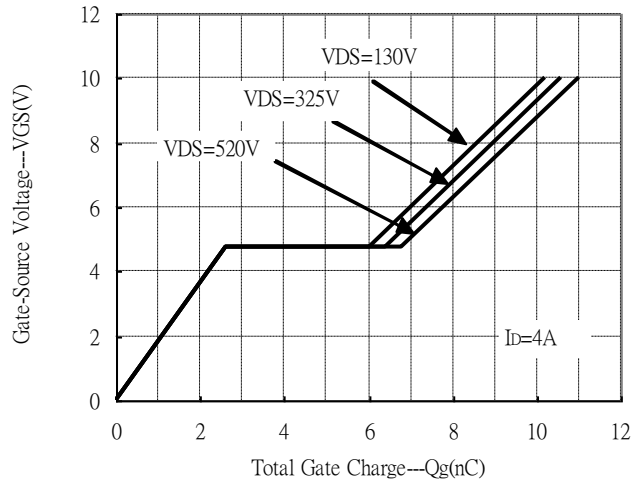
Brekdown Voltage vs Ambient Temperature



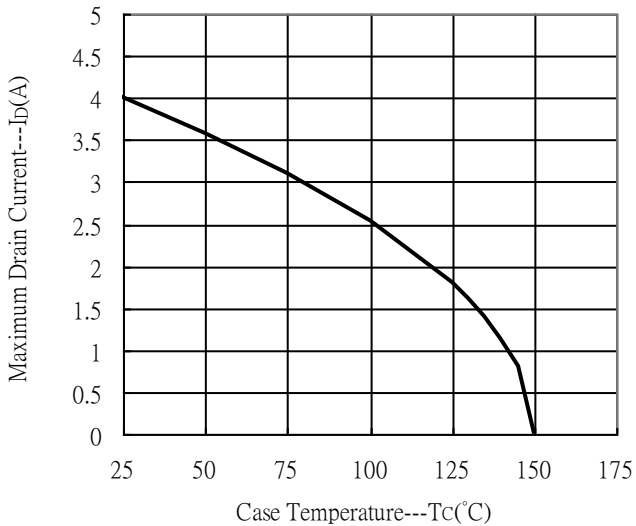
Maximum Safe Operating Area



Gate Charge Characteristics

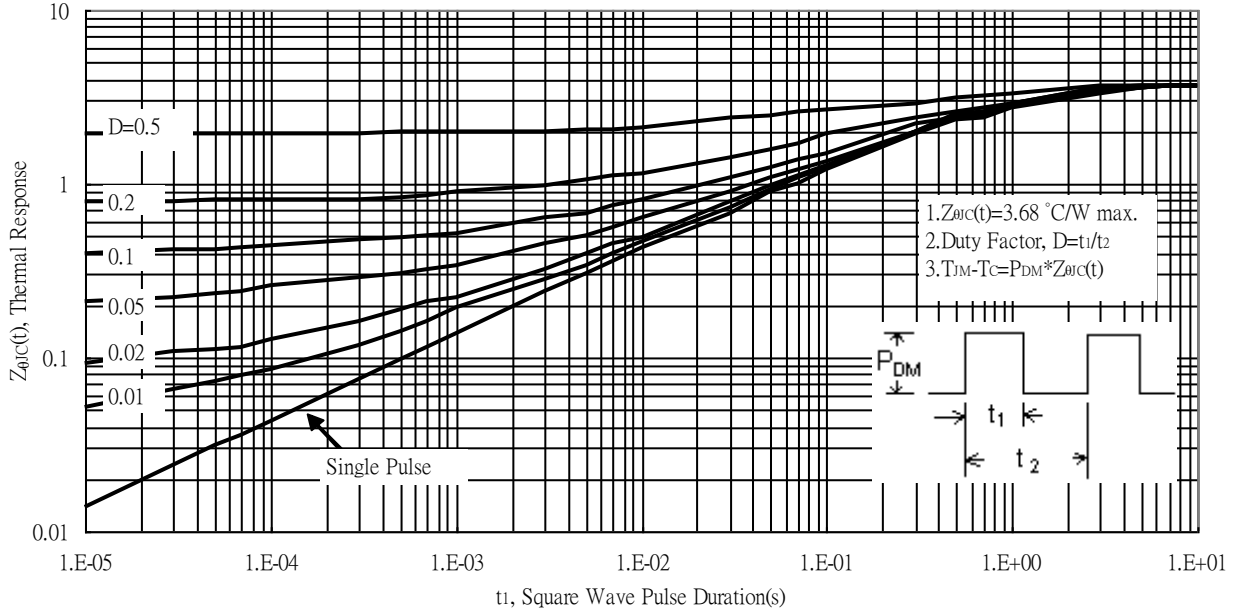


Maximum Drain Current vs Case Temperature

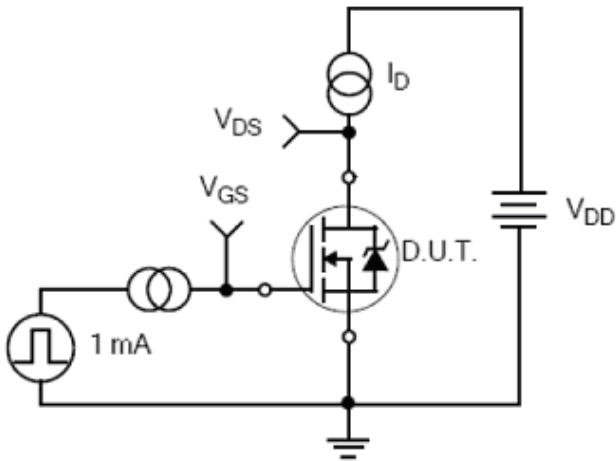


Typical Characteristics(Cont.)

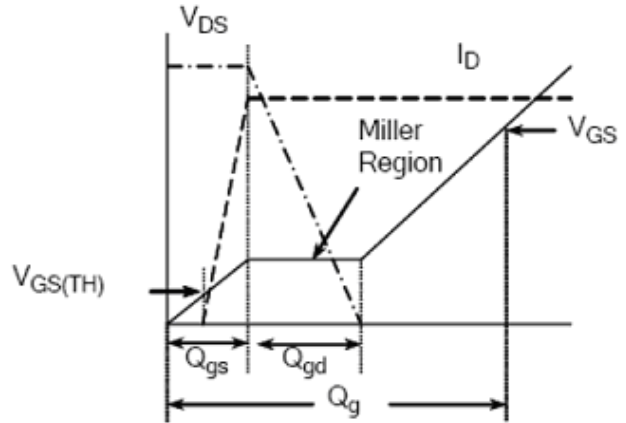
Transient Thermal Response Curves



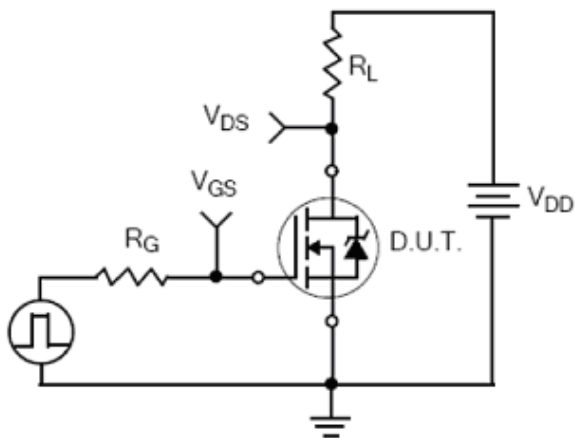
Test Circuit and Waveforms



Gate Charge Test Circuit



Gate Charge Waveform

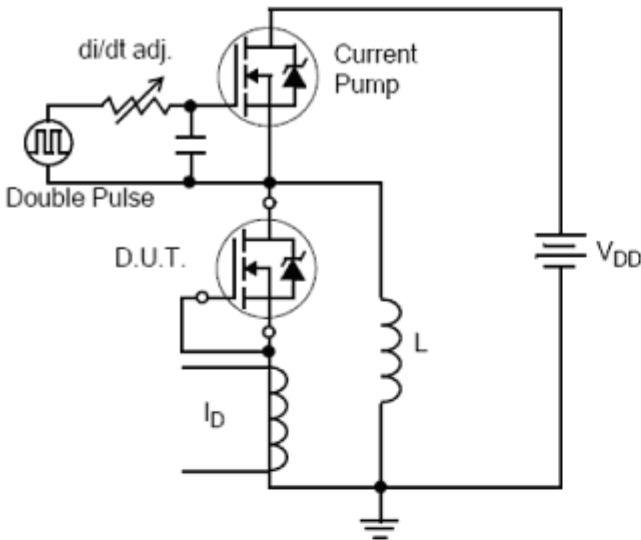


Resistive Switching Test Circuit

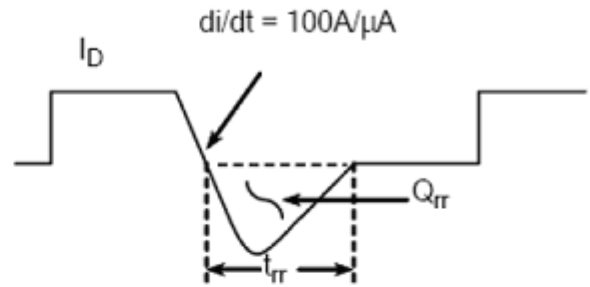


Resistive Switching Waveforms

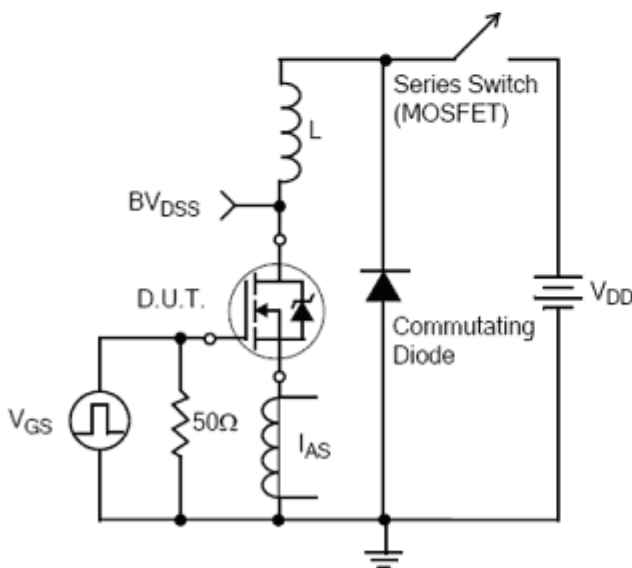
Test Circuit and Waveforms(Cont.)



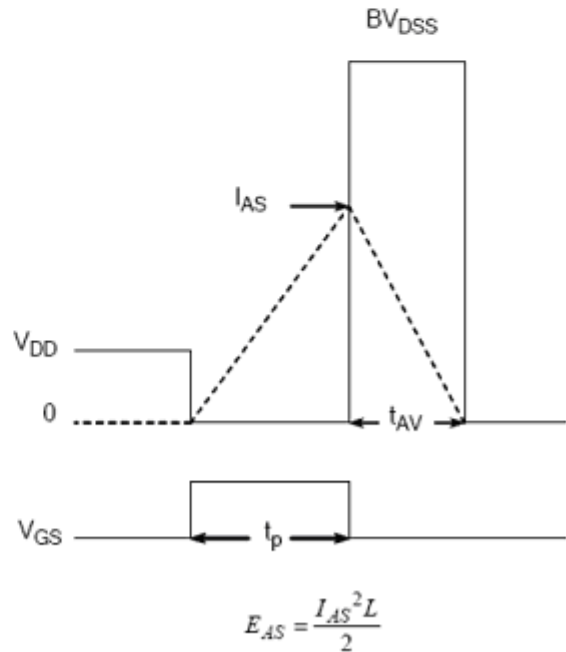
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

TO-220FP Dimension

3-Lead TO-220FP Plastic Package
 CYStek Package Code: FP

Marking:
 Device Name → CYS 4N65
 Date Code → □□□□

Style: Pin 1.Gate 2.Drain 3.Source

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.171	0.183	4.35	4.65	G	0.246	0.258	6.25	6.55
A1	0.051 REF		1.300 REF		H	0.138 REF		3.50 REF	
A2	0.112	0.124	2.85	3.15	H1	0.055 REF		1.40 REF	
A3	0.102	0.110	2.60	2.80	H2	0.256	0.272	6.50	6.90
b	0.020	0.030	0.50	0.75	J	0.031 REF		0.80 REF	
b1	0.031	0.041	0.80	1.05	K	0.020		0.50 REF	
b2	0.047 REF		1.20 REF		L	1.102	1.118	28.00	28.40
c	0.020	0.030	0.500	0.750	L1	0.043	0.051	1.10	1.30
D	0.396	0.404	10.06	10.26	L2	0.036	0.043	0.92	1.08
E	0.583	0.598	14.80	15.20	M	0.067 REF		1.70 REF	
e	0.100 *		2.54*		N	0.012 REF		0.30 REF	
F	0.106 REF		2.70 REF						

- Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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