

N-Channel Logic Level Enhancement Mode MOSFET

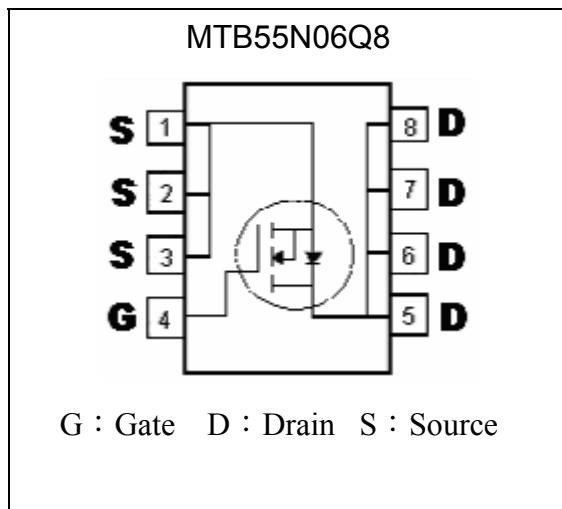
MTB55N06Q8

BV_{DSS}	60V
I_D	8A
RD_{SON}@V_{GS}=10V, I_D=6A	35mΩ (typ)
RD_{SON}@V_{GS}=5V, I_D=5A	38mΩ (typ)

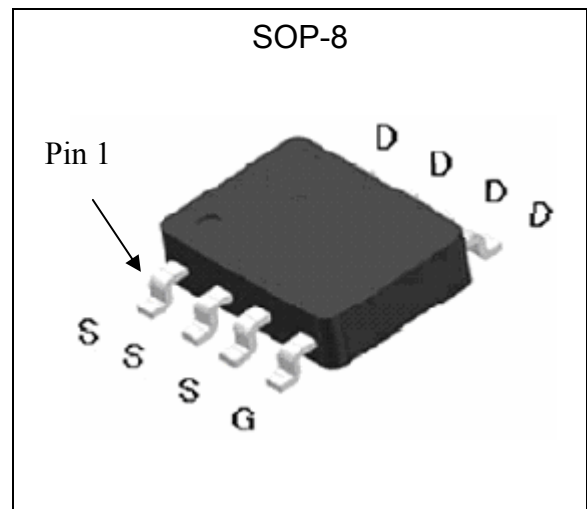
Features

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Dynamic dv/dt rating
- Repetitive Avalanche Rated
- UIS 100% tested
- Pb-free Lead Plating and Halogen-free Package

Symbol

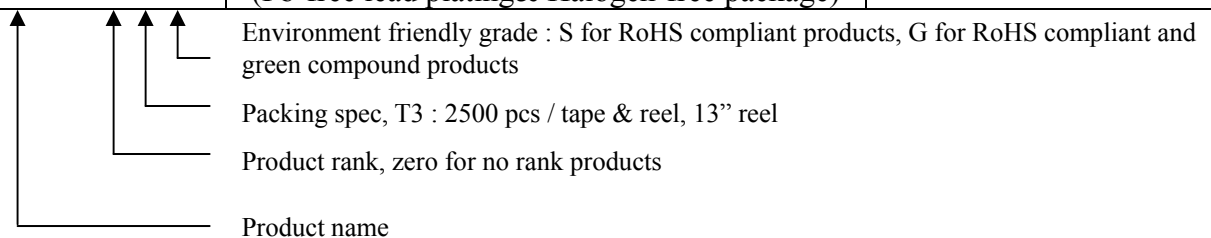


Outline



Ordering Information

Device	Package	Shipping
MTB55N06Q8-0-T3-G	SOP-8 (Pb-free lead plating & Halogen-free package)	2500 pcs / Tape & Reel





Absolute Maximum Ratings (Tc=25°C, unless otherwise noted)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	±20		
Continuous Drain Current @ T _C =25°C, V _{GS} =10V	I _D	8	A	
Continuous Drain Current @ T _C =100°C, V _{GS} =10V		5		
Continuous Drain Current @ T _A =25°C, V _{GS} =10V		6.3		
Continuous Drain Current @ T _A =100°C, V _{GS} =10V		4		
Pulsed Drain Current	I _{DM}	30 *1		
Avalanche Current	I _{AS}	6		
Avalanche Energy @ L=0.1mH, I _D =6A, R _G =25 Ω	E _{AS}	1.8	mJ	
Repetitive Avalanche Energy @ L=0.05mH	E _{AR}	0.9 *2		
Total Power Dissipation	P _D	T _A =25°C	3.1 *3	W
		T _A =100°C	1.2	
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55~+150	°C	

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	25	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	40 *3	°C/W

- Note : 1. Pulse width limited by maximum junction temperature.
 2. Duty cycle ≤ 1%.
 3. Surface mounted on 1 in² copper pad of FR-4 board, t ≤ 10s; 125°C/W when mounted on minimum copper pad.

Characteristics (Tc=25°C, unless otherwise specified)

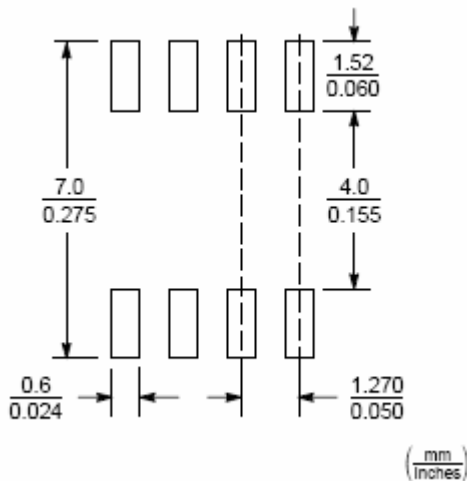
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	60	-	-	V	V _{GS} =0, I _D =250μA
V _{GS(th)}	1.0	1.7	3.0	V	V _{DS} = V _{GS} , I _D =250μA
G _{FS} *1	-	11	-	S	V _{DS} = 5V, I _D =6A
I _{GSS}	-	-	±100	nA	V _{GS} =±20
I _{DSS}	-	-	1	μA	V _{DS} = 48V, V _{GS} = 0
	-	-	25		V _{DS} = 40V, V _{GS} = 0, T _J =125°C
R _{DS(ON)} *1	-	35	45	mΩ	V _{GS} = 10V, I _D =6A
	-	38	50	mΩ	V _{GS} = 5V, I _D =5A
Dynamic					
C _{iss}	-	1160	-	pF	V _{GS} =0V, V _{DS} =30V, f=1MHz
C _{oss}	-	44	-		
C _{rss}	-	33	-		

Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Qg *1, 2	-	14	-	nC	V _{DS} =30V, V _{GS} =10V, I _D =6A
Qgs *1, 2	-	3.7	-		
Qgd *1, 2	-	4.9	-		
t _{d(ON)} *1, 2	-	12	-	ns	V _{DS} =30V, I _D =1A, V _{GS} =10V, R _{GS} =6Ω
t _r *1, 2	-	6	-		
t _{d(OFF)} *1, 2	-	34	-		
t _f *1, 2	-	12	-		
Source-Drain Diode					
I _S *1	-	-	2.3	A	
I _{SM} *3	-	-	9.2		
V _{SD} *1	-	0.77	1.2	V	I _F =I _S , V _{GS} =0V

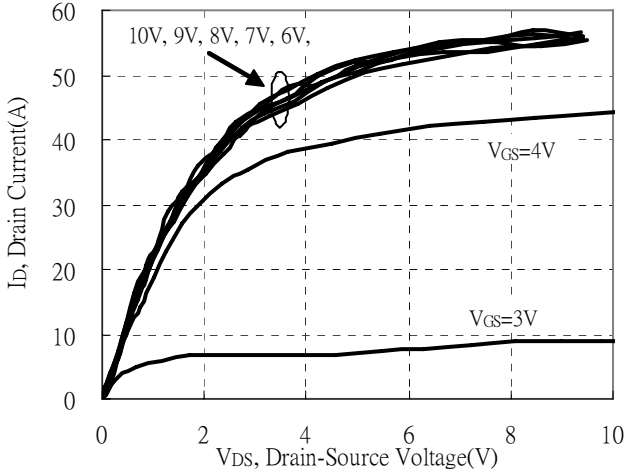
Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

Recommended Soldering Footprint

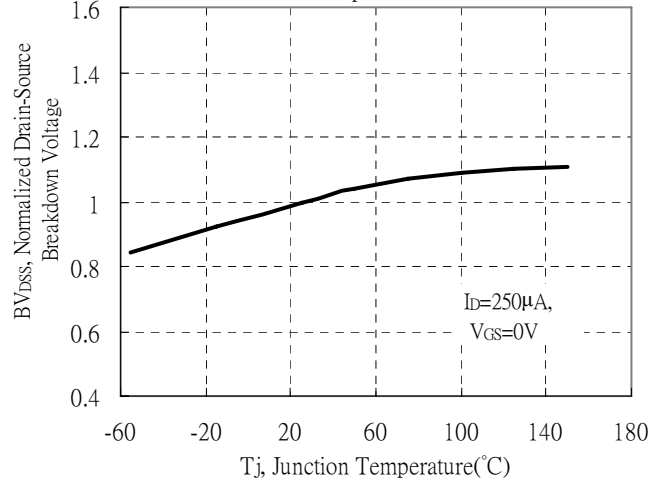


Typical Characteristics

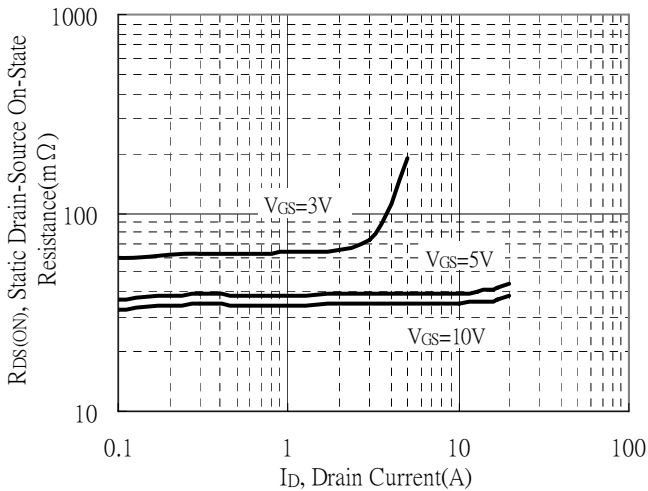
Typical Output Characteristics



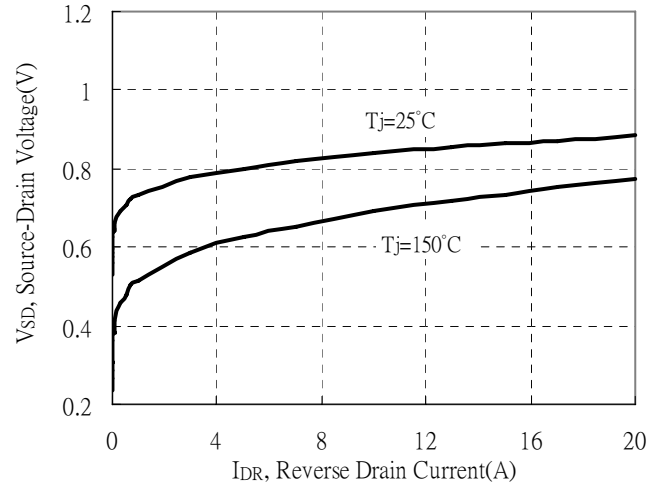
Normalized Brekdown Voltage vs Ambient Temperature



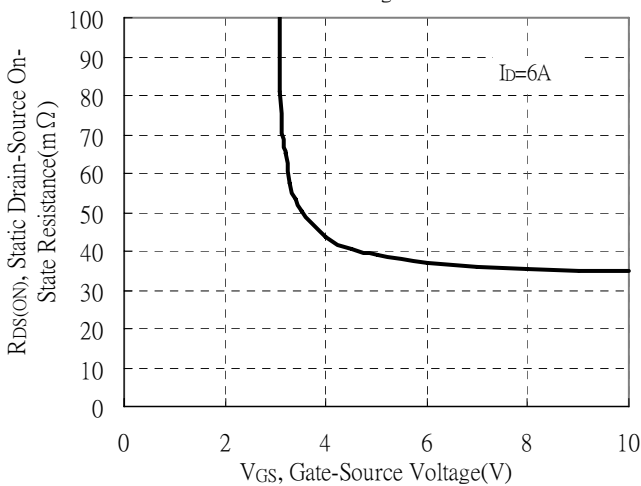
Static Drain-Source On-State resistance vs Drain Current



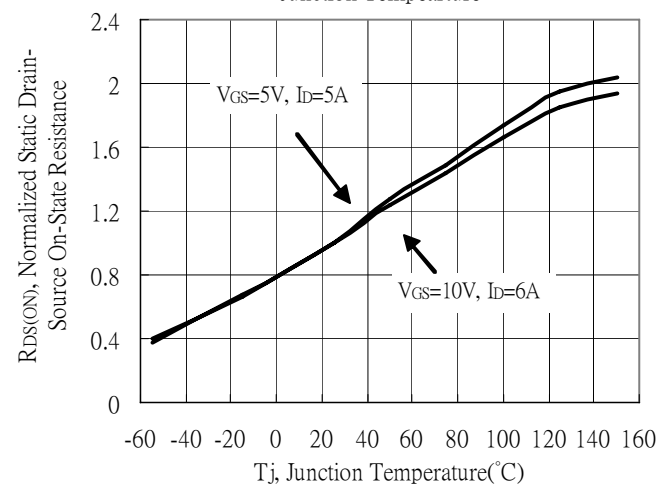
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

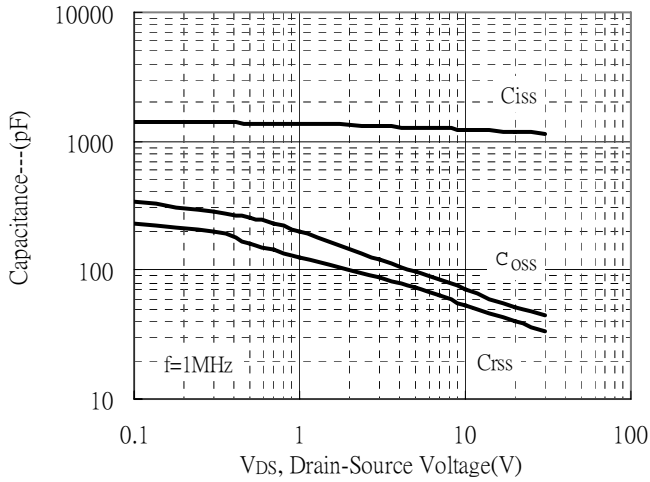


Normalized Drain-Source On-State Resistance vs Junction Temperature

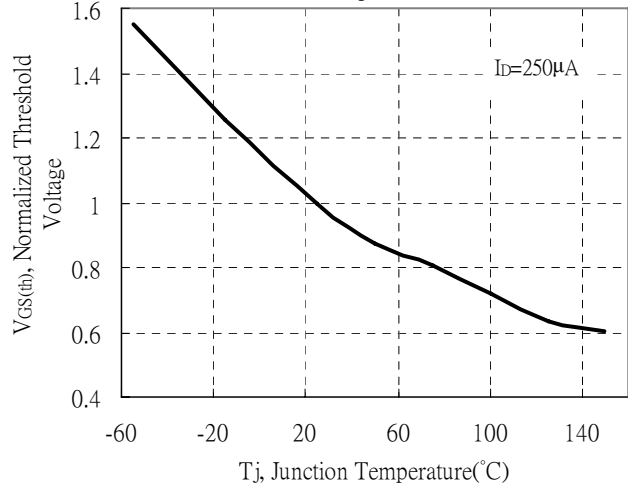


Typical Characteristics(Cont.)

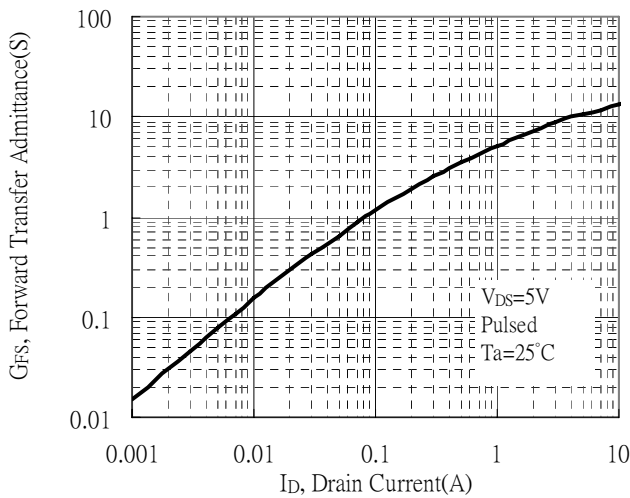
Capacitance vs Drain-to-Source Voltage



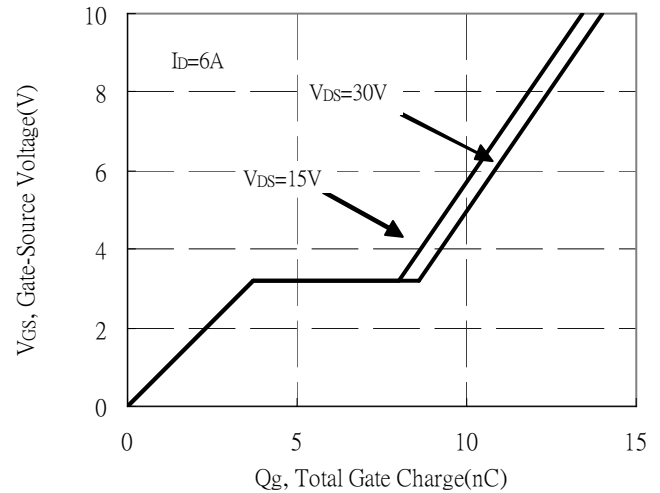
Normalized Threshold Voltage vs Junction Temperature



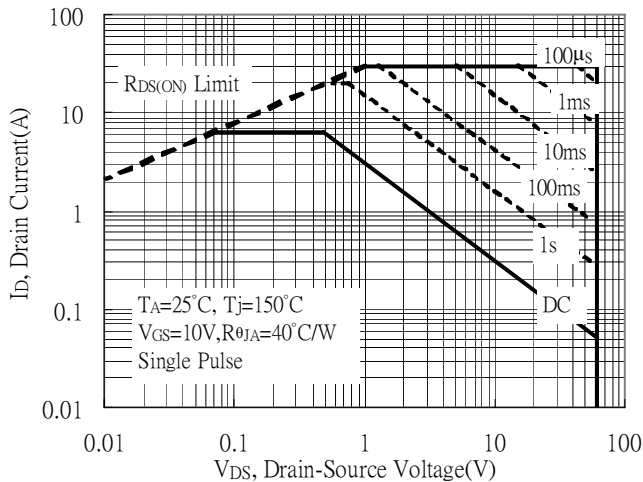
Forward Transfer Admittance vs Drain Current



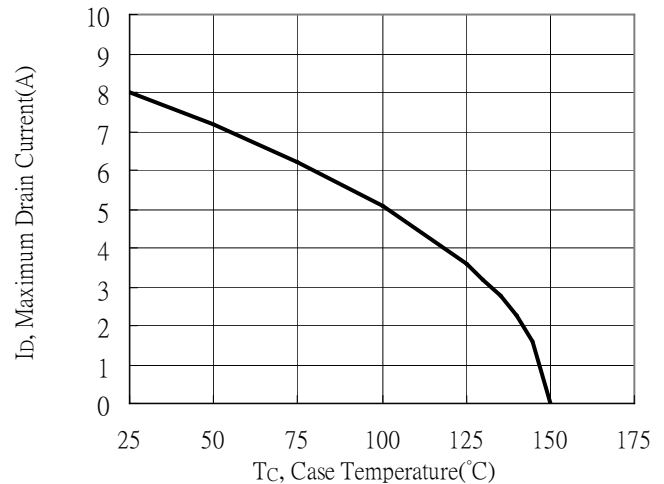
Gate Charge Characteristics



Maximum Safe Operating Area



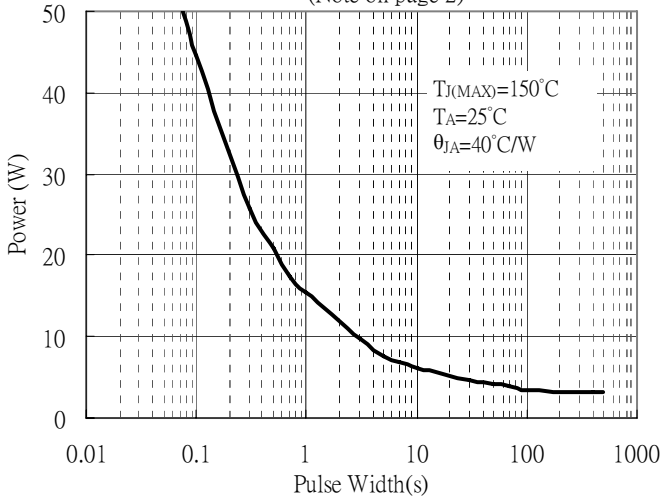
Maximum Drain Current vs Case Temperature



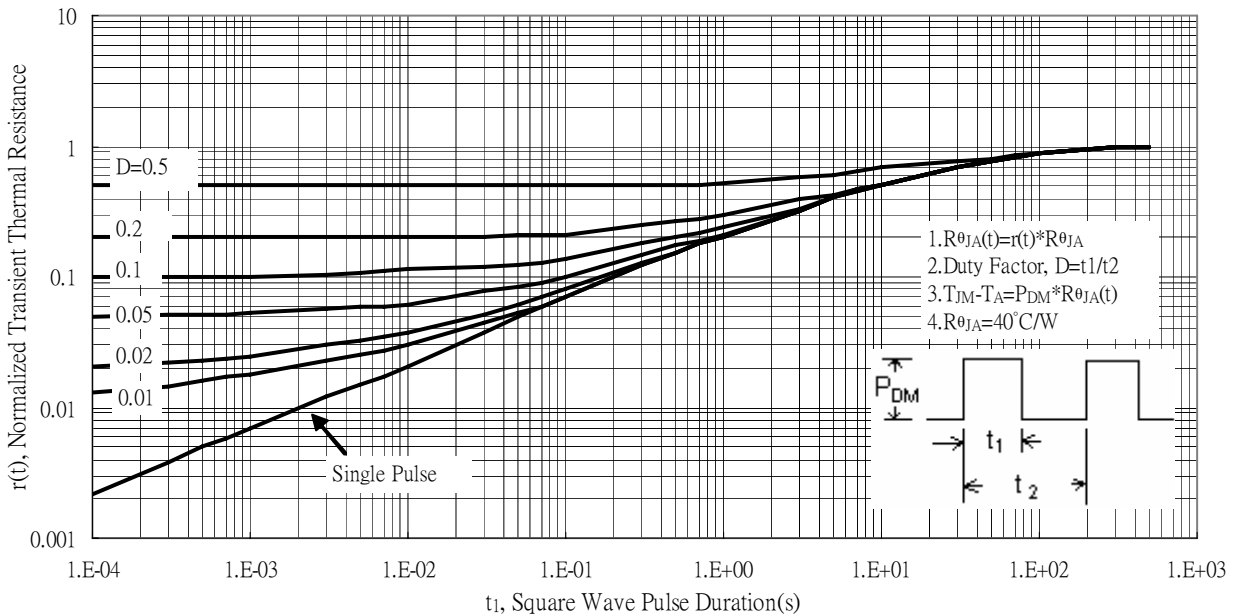


Typical Characteristics(Cont.)

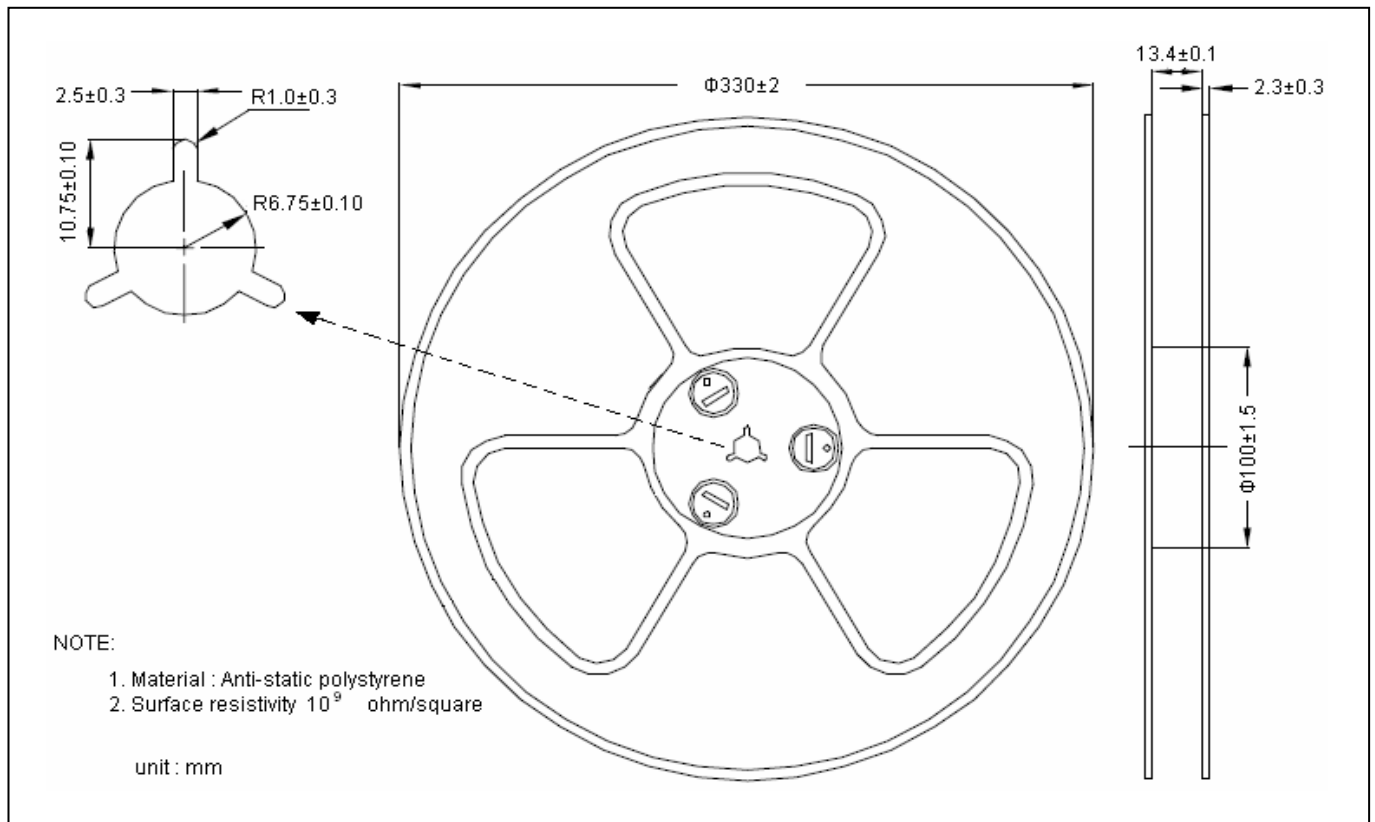
Single Pulse Power Rating, Junction to Ambient
(Note on page 2)



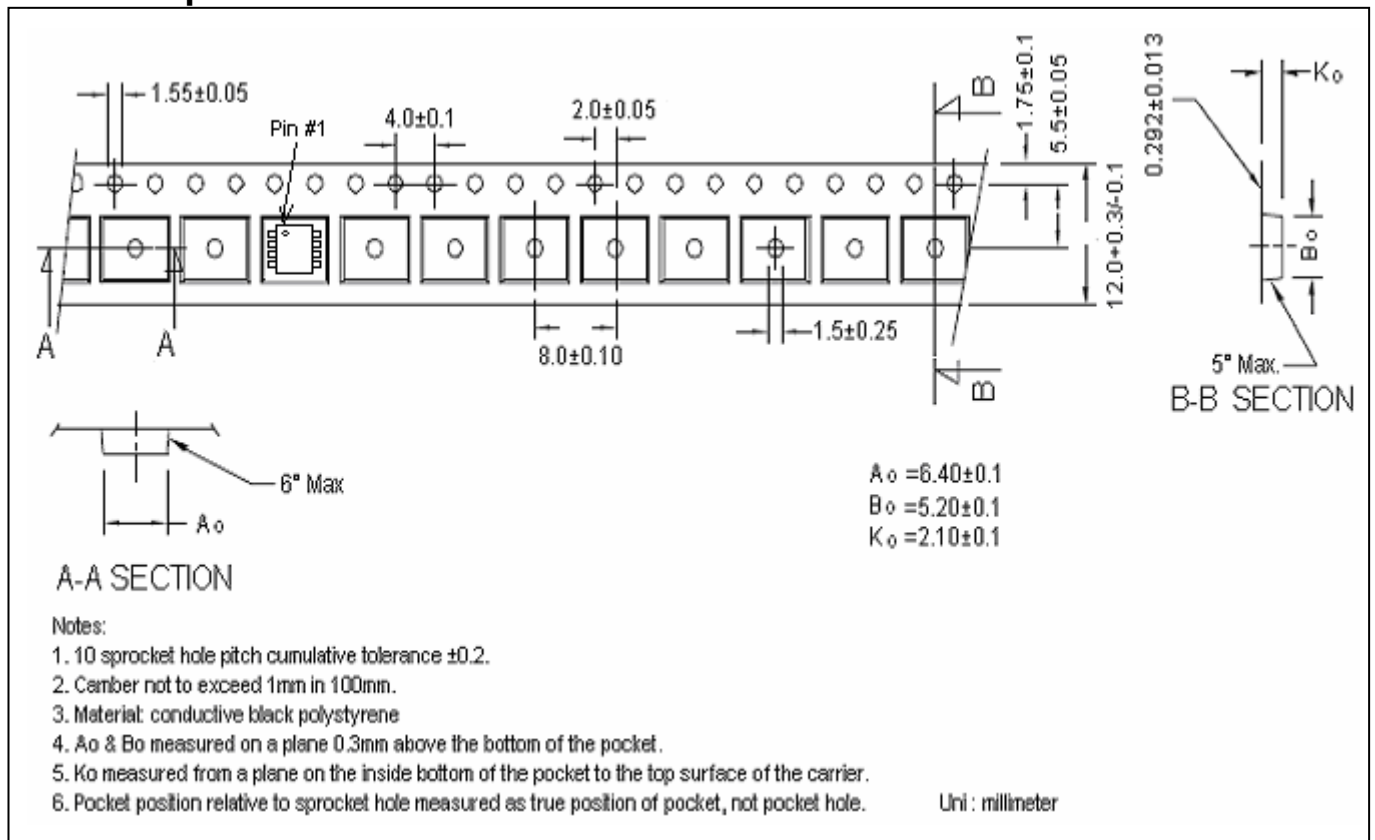
Transient Thermal Response Curves



Reel Dimension



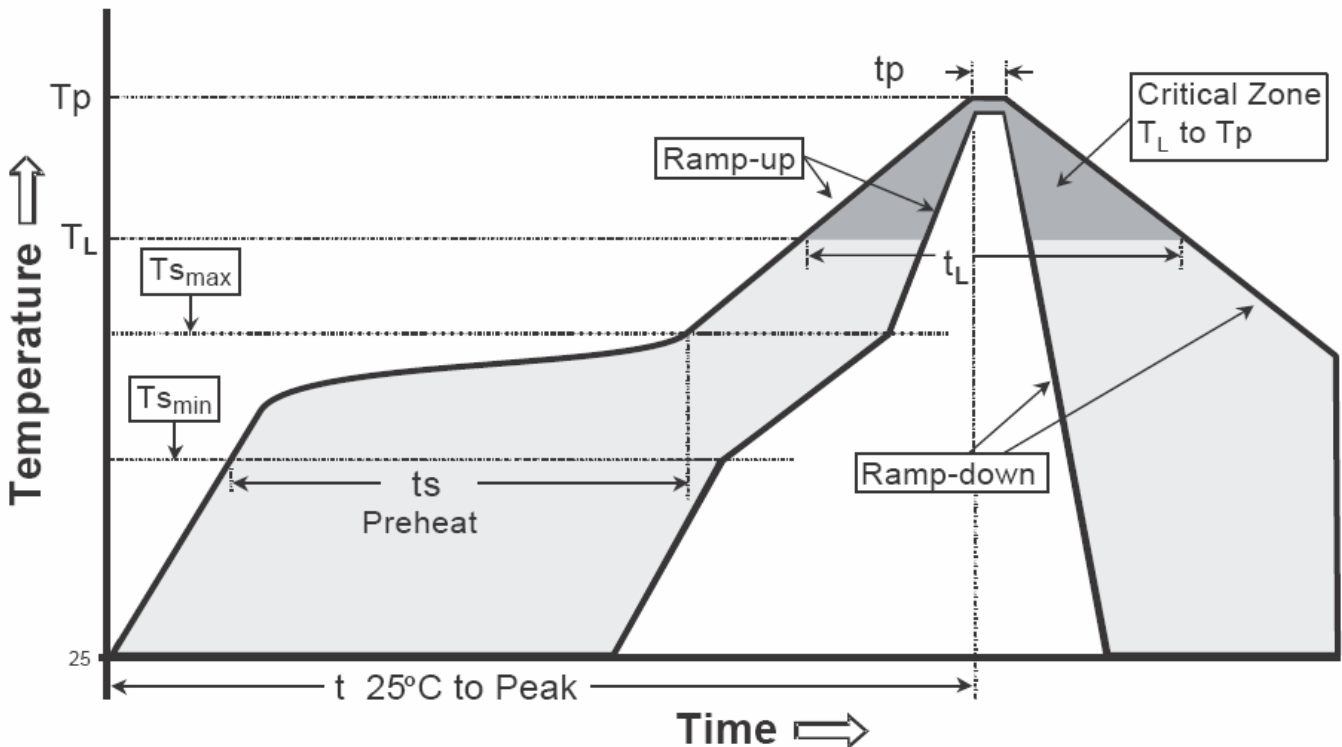
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

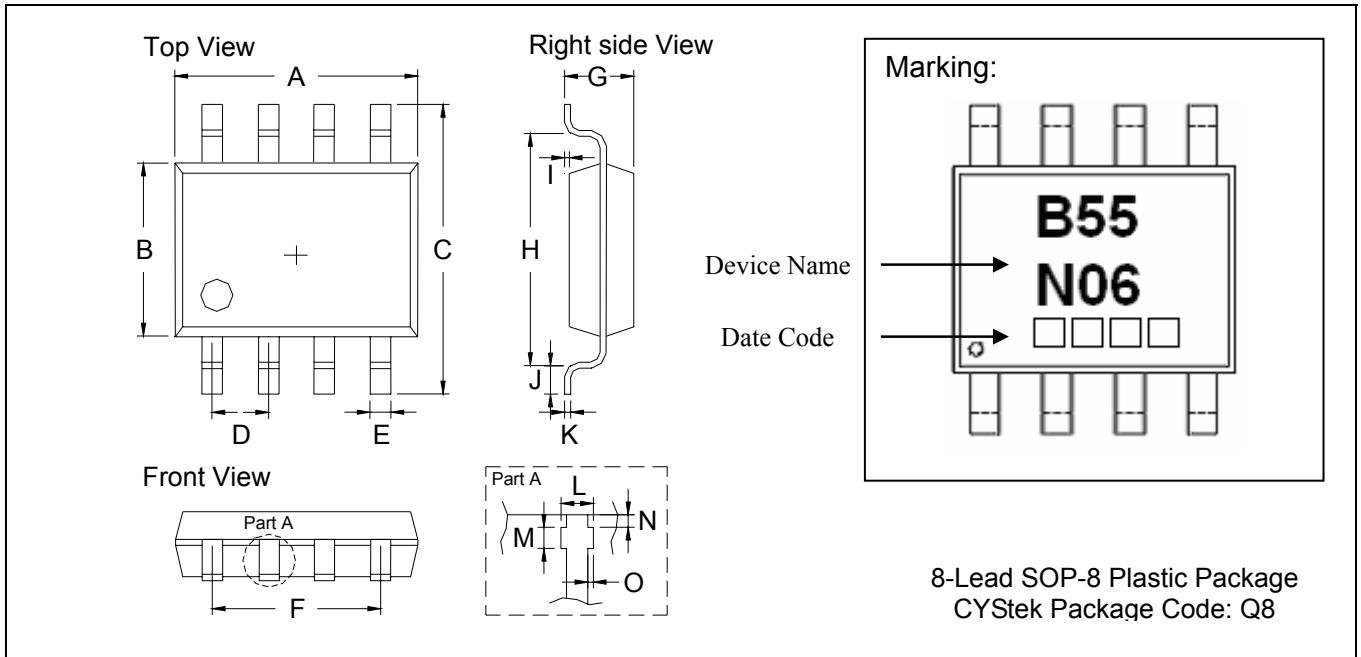
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOP-8 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1850	0.2007	4.70	5.10	I	0.0031	0.0110	0.08	0.28
B	0.1457	0.1614	3.70	4.10	J	0.0157	0.0323	0.40	0.83
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0102	0.19	0.26
D	0.0500*		1.27*		L	0.0145	0.0204	0.37	0.52
E	0.0130	0.0201	0.33	0.51	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0472	0.0638	1.20	1.62	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.