

# N-Channel Logic Level Enhancement Mode Power MOSFET

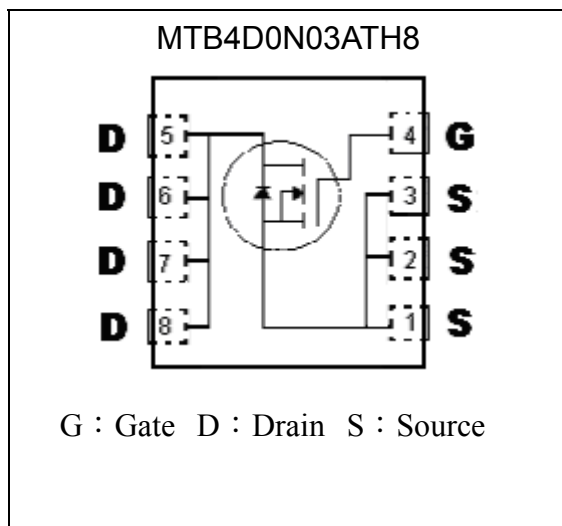
## MTB4D0N03ATH8

<b>BV<sub>DSS</sub></b>	<b>30V</b>
<b>I<sub>D</sub> @ V<sub>GS</sub>=10V</b>	<b>66A</b>
<b>R<sub>DS(ON)</sub>@ V<sub>GS</sub>=10V, I<sub>D</sub>=30A</b>	<b>5.3 mΩ (typ)</b>
<b>R<sub>DS(ON)</sub>@ V<sub>GS</sub>=4.5V, I<sub>D</sub>=20A</b>	<b>7.5 mΩ (typ)</b>

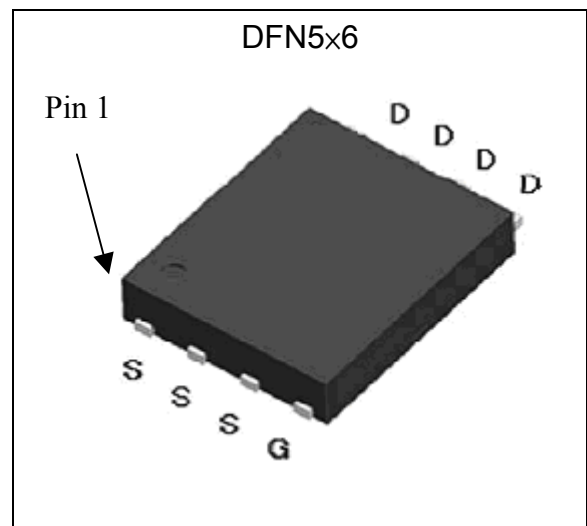
### Features

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Dynamic dv/dt rating
- Pb-free lead plating and Halogen-free package

### Symbol

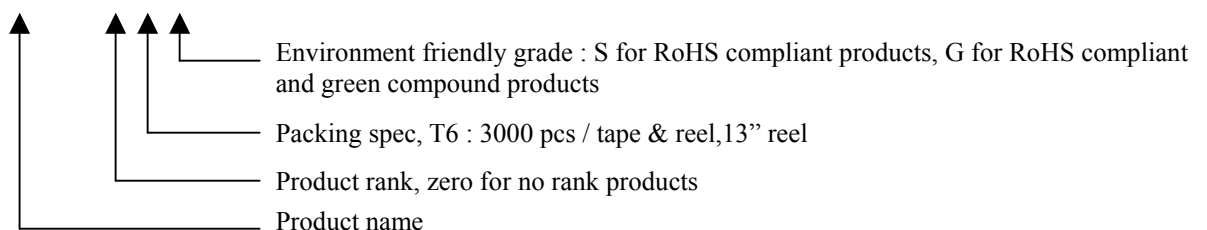


### Outline



### Ordering Information

Device	Package	Shipping
MTB4D0N03ATH8-0-T6-G	DFN 5 × 6 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30	V	
Gate-Source Voltage	V <sub>GS</sub>	±20		
Continuous Drain Current @ T <sub>c</sub> =25°C, V <sub>GS</sub> =10V	I <sub>D</sub>	66	A	
Continuous Drain Current @ T <sub>c</sub> =100°C, V <sub>GS</sub> =10V		42		
Pulsed Drain Current	I <sub>DM</sub>	160 *1		
Avalanche Current	I <sub>AS</sub>	43		
Avalanche Energy @ L=0.1mH, I <sub>D</sub> =43A, R <sub>G</sub> =25 Ω	E <sub>AS</sub>	92.5	mJ	
Repetitive Avalanche Energy @ L=0.05mH	E <sub>AR</sub>	5 *2		
Total Power Dissipation	P <sub>D</sub>	T <sub>c</sub> =25°C	50	W
		T <sub>c</sub> =100°C	20	
Operating Junction and Storage Temperature Range	T <sub>j</sub> , T <sub>stg</sub>	-55~+150	°C	

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R <sub>th,j-c</sub>	2.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R <sub>th,j-a</sub>	50 *3	°C/W

- Note : 1. Pulse width limited by maximum junction temperature  
 2. Duty cycle ≤ 1%  
 3. Surface mounted on 1 in<sup>2</sup> copper pad of FR-4 board, t ≤ 10s; 125°C/W when mounted on minimum copper pad.

**Characteristics (T<sub>c</sub>=25°C, unless otherwise specified)**

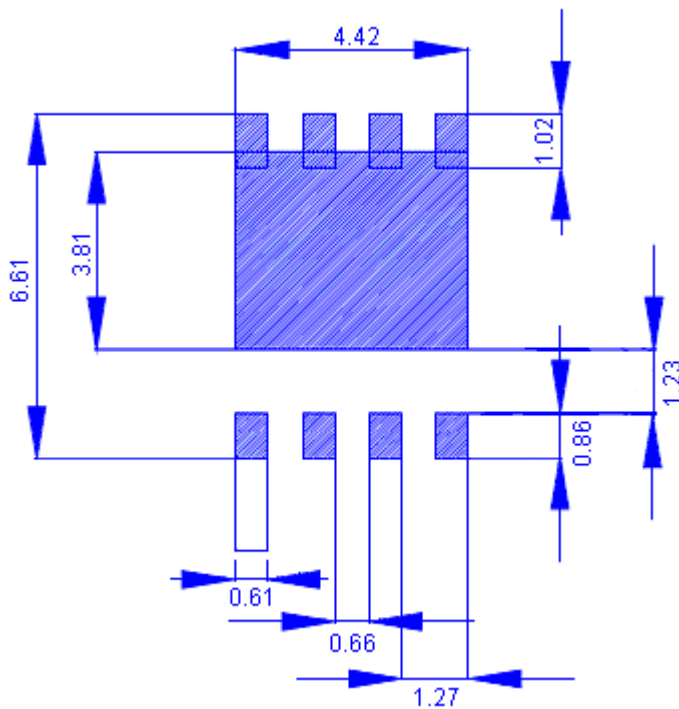
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	30	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
V <sub>GS(th)</sub>	1.0	1.8	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA
G <sub>FS</sub> *1	-	25	-	S	V <sub>DS</sub> =5V, I <sub>D</sub> =18A
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±20V
I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V
	-	-	25		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>j</sub> =125°C
R <sub>DS(ON)</sub> *1	-	5.3	7.0	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =30A
	-	7.5	10.0	mΩ	V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A
<b>Dynamic</b>					
C <sub>iss</sub>	-	1511	-	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz
C <sub>oss</sub>	-	299	-		
C <sub>rss</sub>	-	208	-		

**Characteristics (Tc=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Qg (VGS=10V) *1, 2	-	34	-	nC	VDS=15V, VGS=10V, ID=30A
Qg (VGS=4.5V) *1, 2	-	17	-		
Qgs *1, 2	-	6	-		
Qgd *1, 2	-	9.3	-		
td(ON) *1, 2	-	7	-	ns	VDS=15V, ID=24A, VGS=10V, RGS=2.7Ω
tr *1, 2	-	10	-		
td(OFF) *1, 2	-	22	-		
tf *1, 2	-	10	-		
Rg	-	4.3	-	Ω	VGS=15mV, VDS=0V, f=1MHz
<b>Source-Drain Diode</b>					
IS *1	-	-	66	A	
ISM *3	-	-	150		
VSD *1	-	0.81	1.2	V	IS=18A, VGS=0V
trr	-	14.5	-	ns	IF=18A, dIF/dt=100A/μs
Qrr	-	7.3	-	nC	

Note : \*1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%  
 \*2.Independent of operating temperature  
 \*3.Pulse width limited by maximum junction temperature.

**Recommended Soldering Footprint**

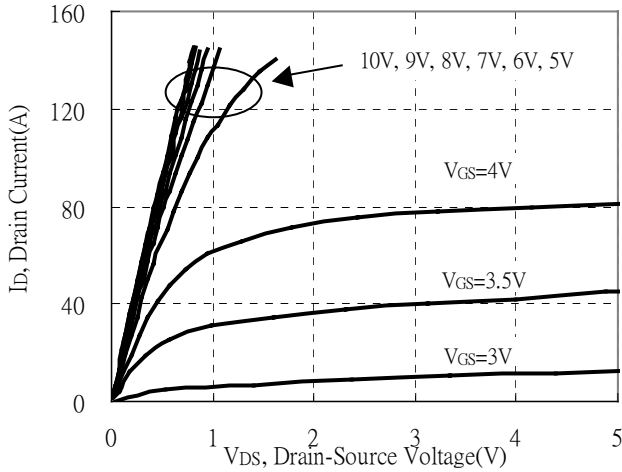


unit : mm

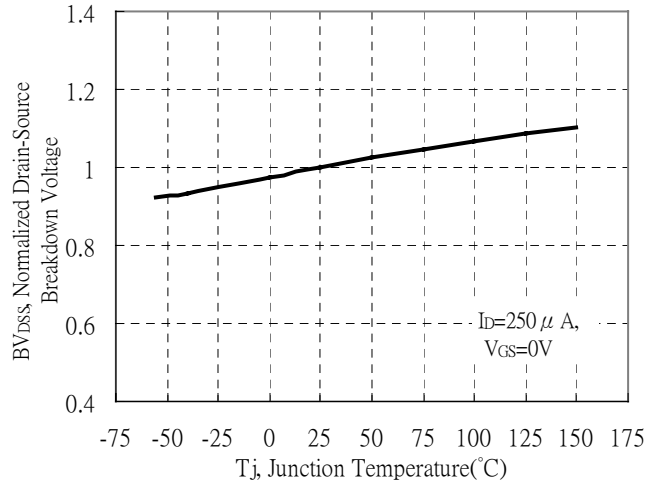


**Typical Characteristics**

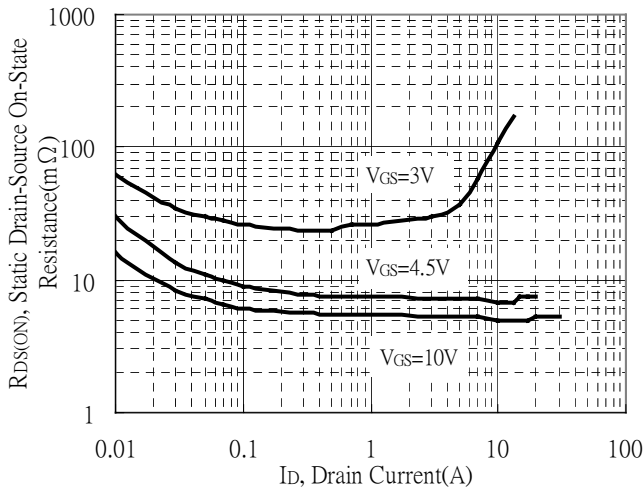
Typical Output Characteristics



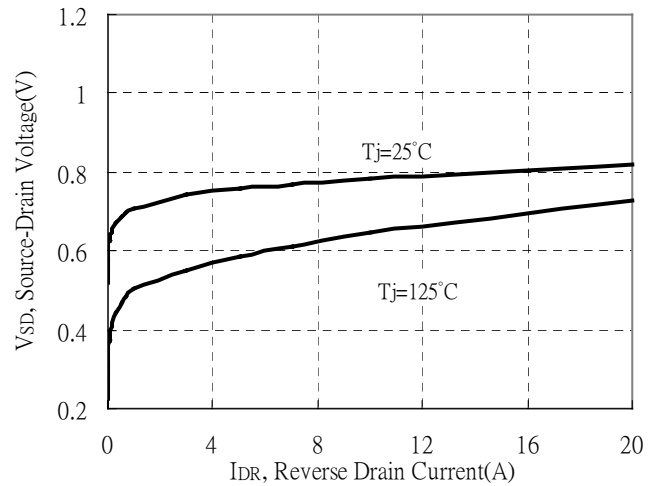
Brekdown Voltage vs Ambient Temperature



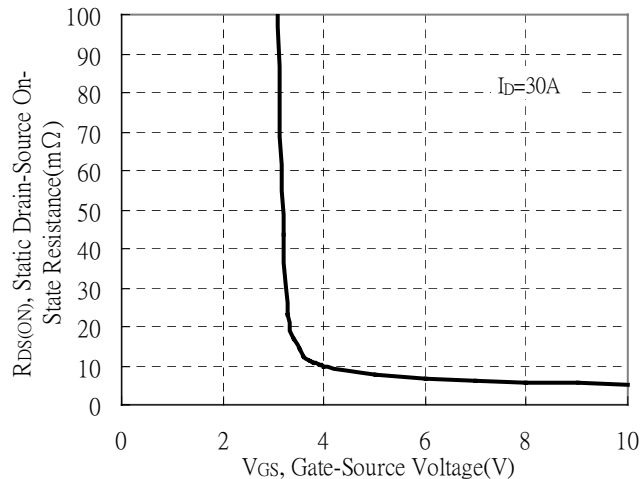
Static Drain-Source On-State resistance vs Drain Current



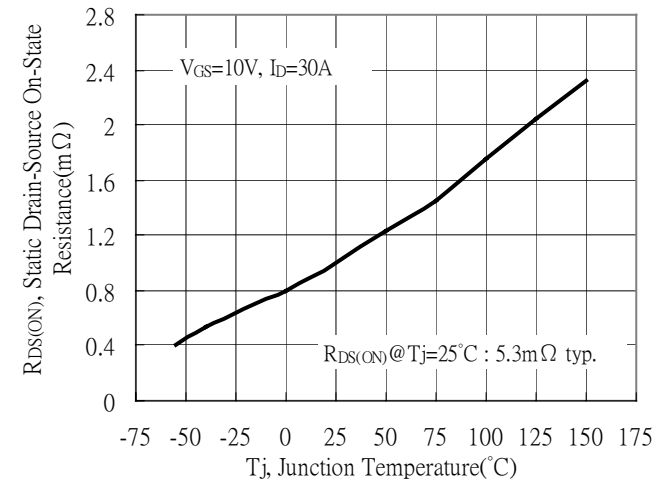
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



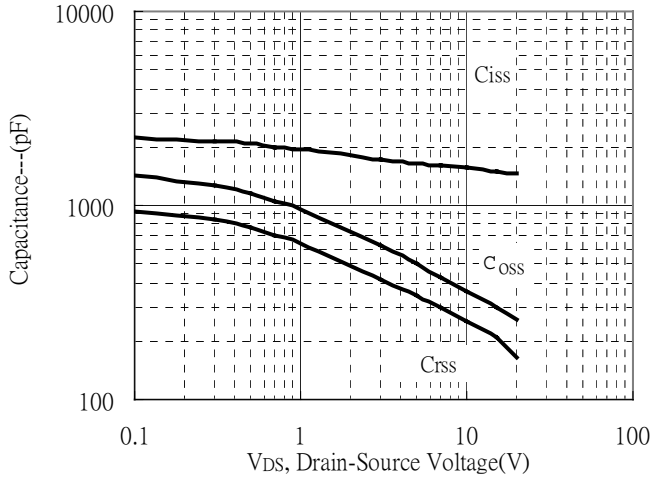
Drain-Source On-State Resistance vs Junction Temperature



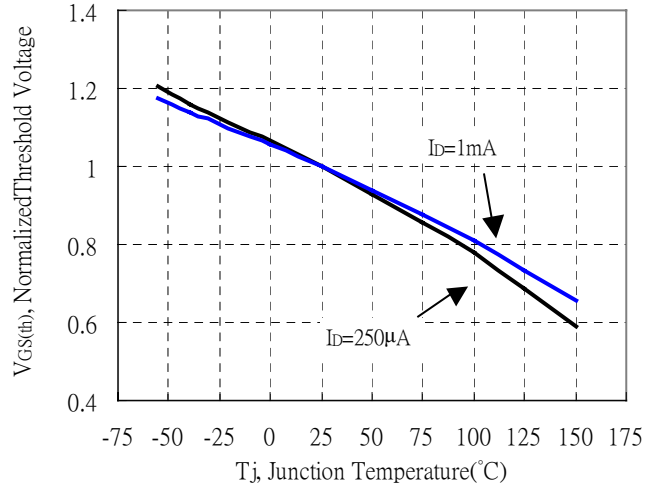


### Typical Characteristics(Cont.)

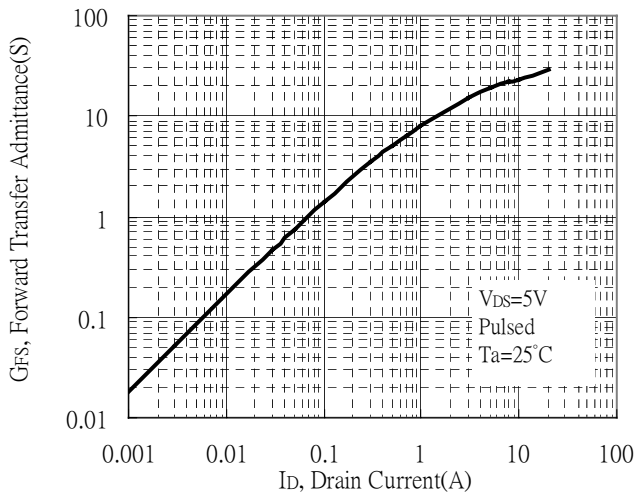
Capacitance vs Drain-to-Source Voltage



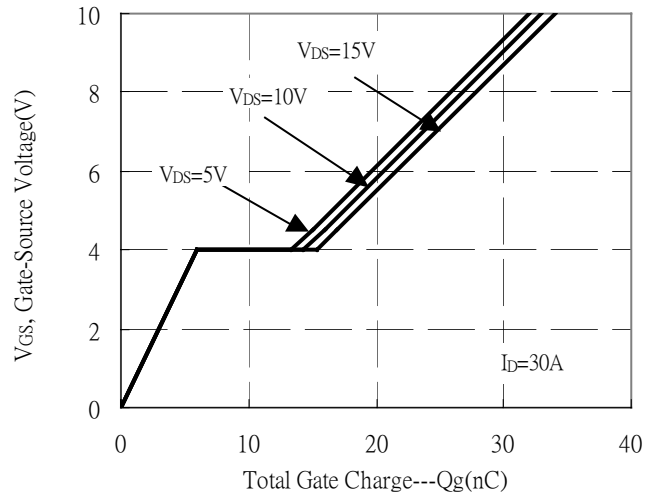
Threshold Voltage vs Junction Temperature



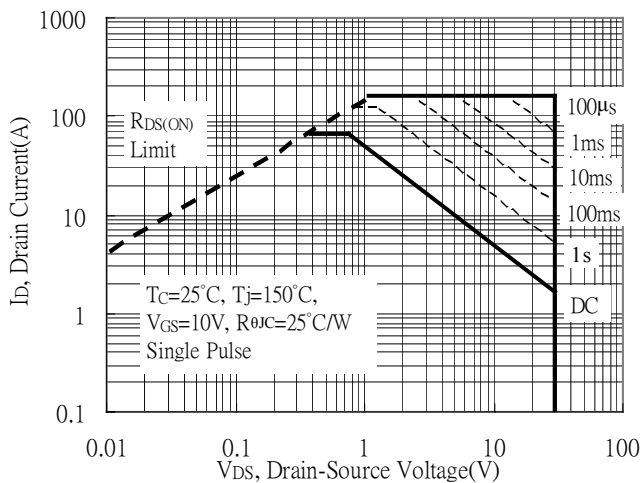
Forward Transfer Admittance vs Drain Current



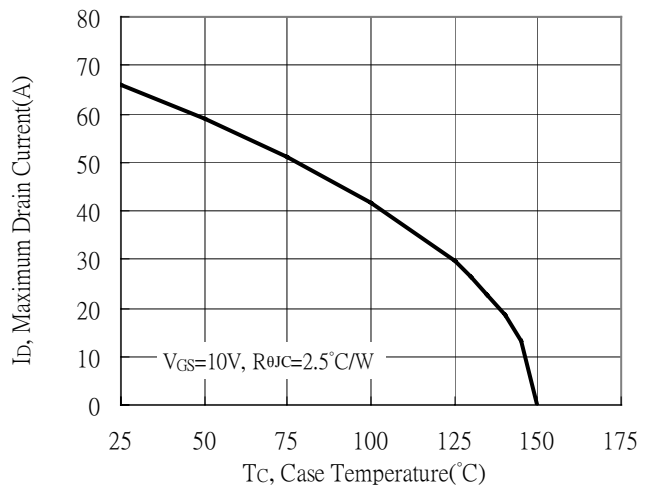
Gate Charge Characteristics



Maximum Safe Operating Area

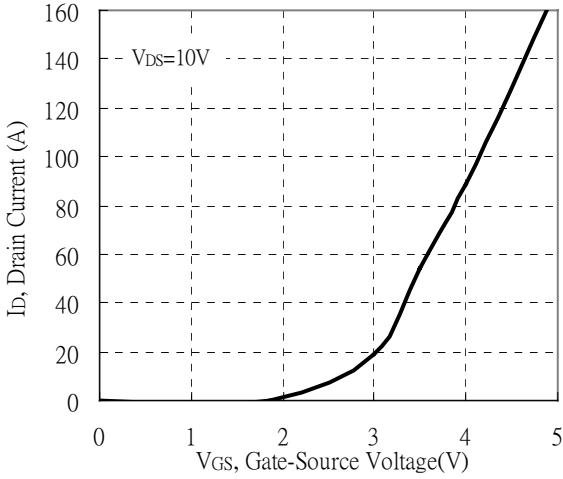


Maximum Drain Current vs Case Temperature

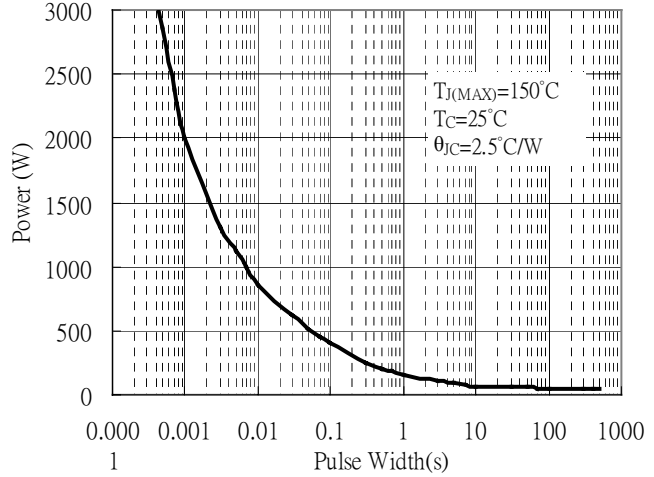


**Typical Characteristics(Cont.)**

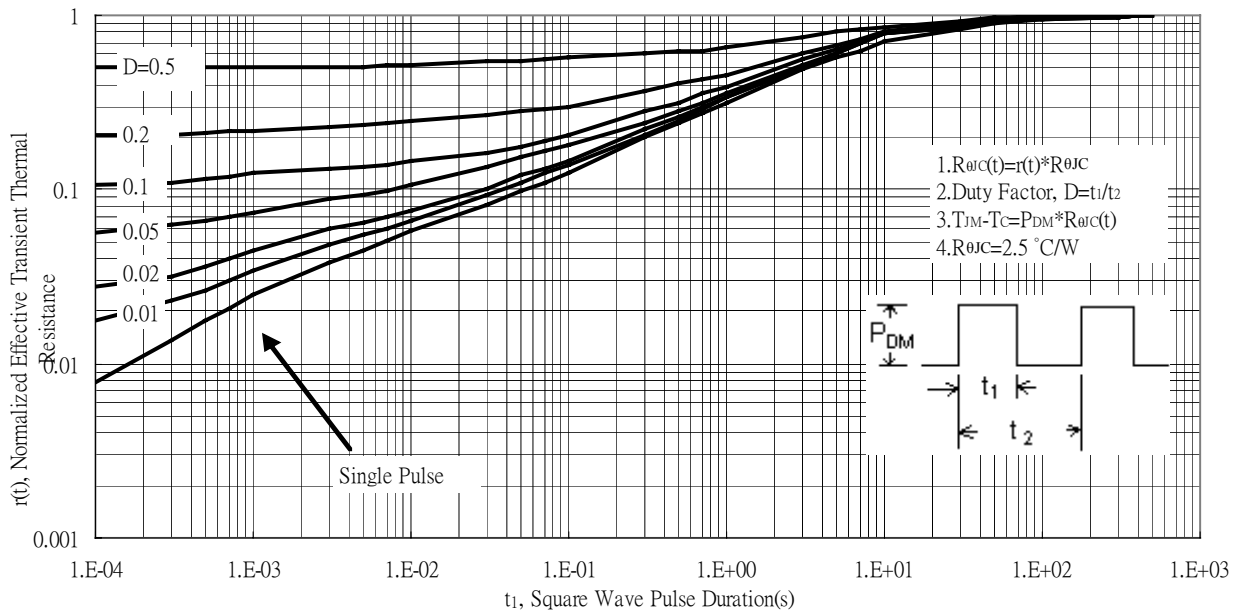
Typical Transfer Characteristics



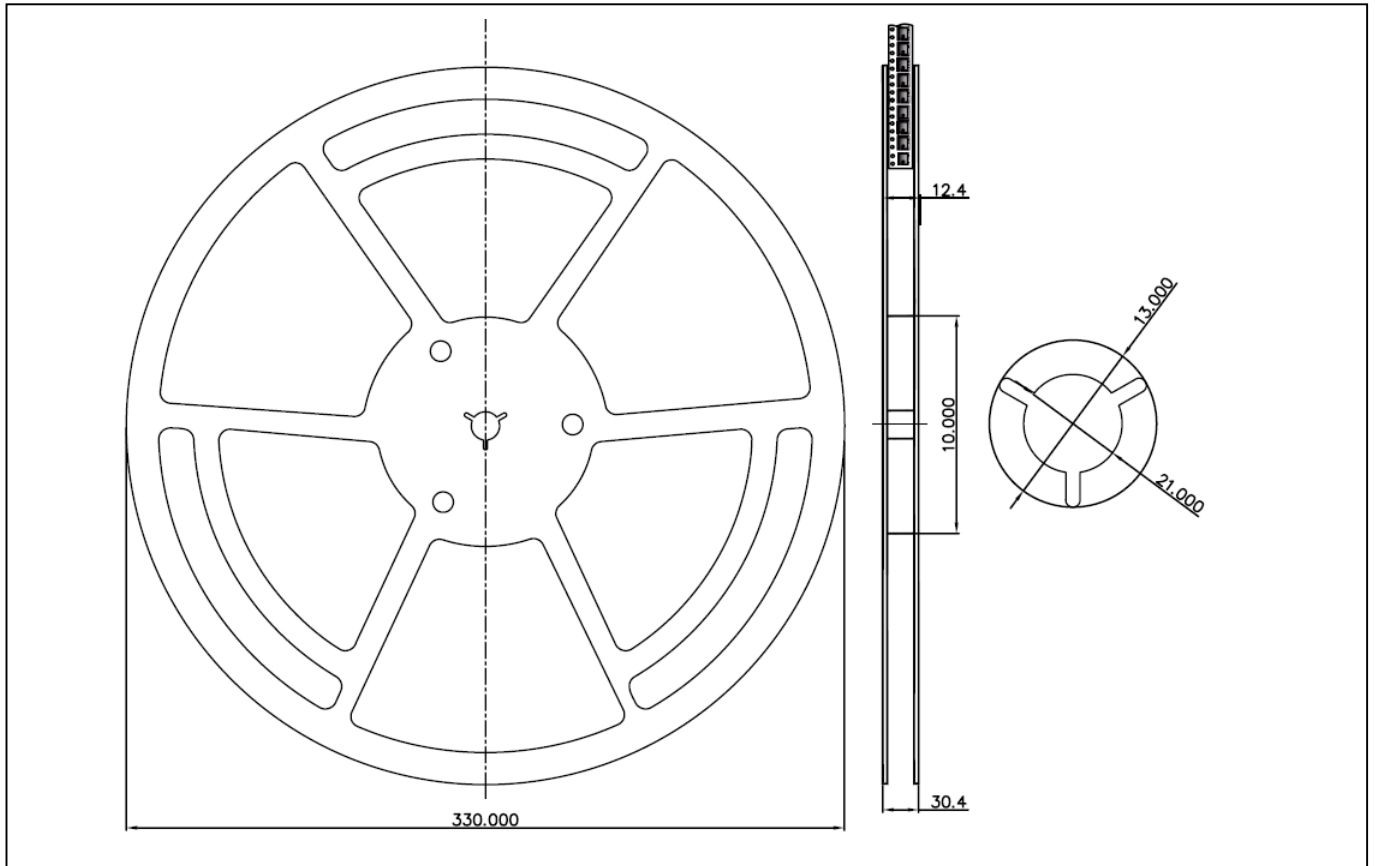
Single Pulse Maximum Power Dissipation



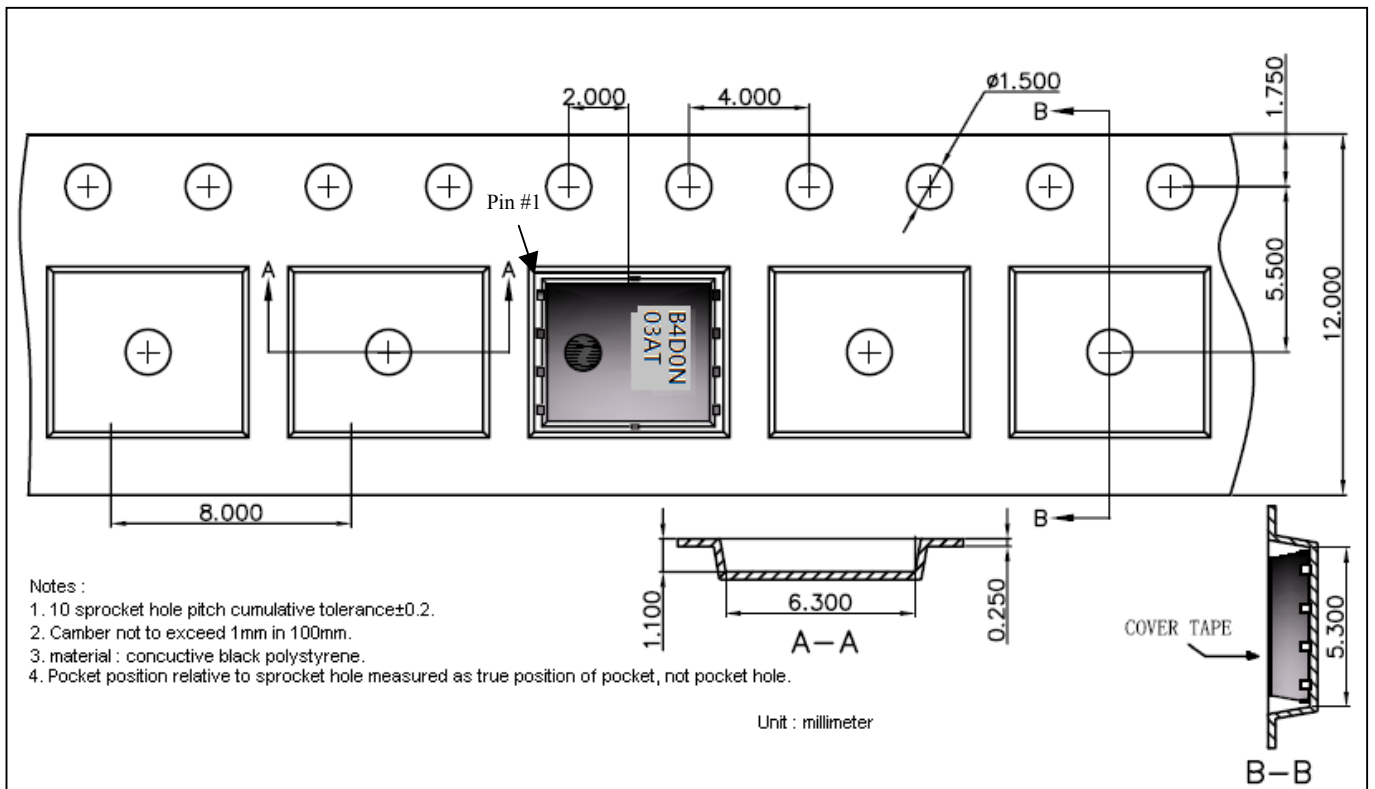
Transient Thermal Response Curves



**Reel Dimension**



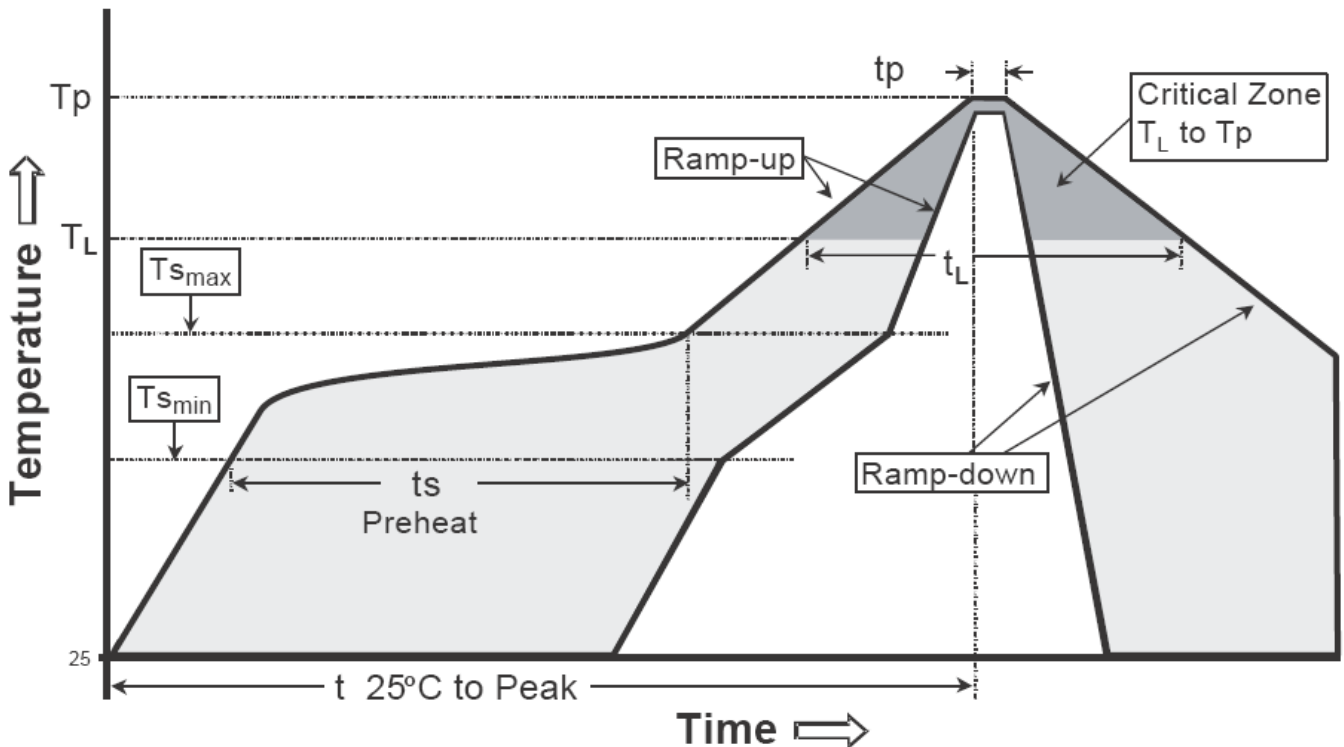
**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**

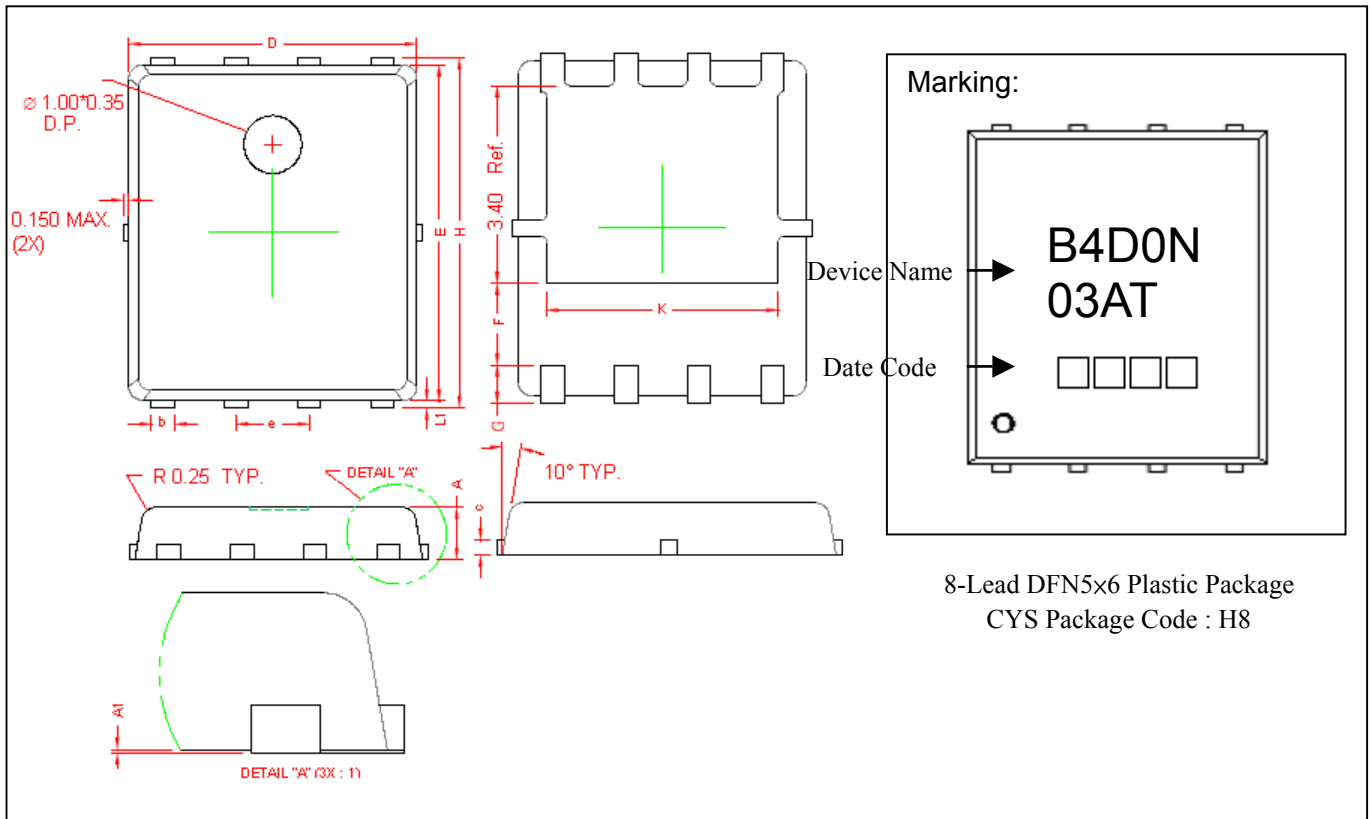


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>p</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t <sub>p</sub> )	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.



**DFN5x6 Dimension**



8-Lead DFN5x6 Plastic Package  
 CYS Package Code : H8

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.80	1.00	0.031	0.039	E	5.70	5.90	0.224	0.232
A1	0.00	0.05	0.000	0.002	e	1.27 BSC		0.050 BSC	
b	0.35	0.49	0.014	0.019	H	5.95	6.20	0.234	0.244
c	0.254 REF		0.010 REF		L1	0.10	0.18	0.004	0.007
D	4.90	5.10	0.193	0.201	G	0.60 REF		0.024 REF	
F	1.40 REF		0.055 REF		K	4.00 REF		0.157 REF	

**Notes:** 1. Controlling dimension: millimeters.  
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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