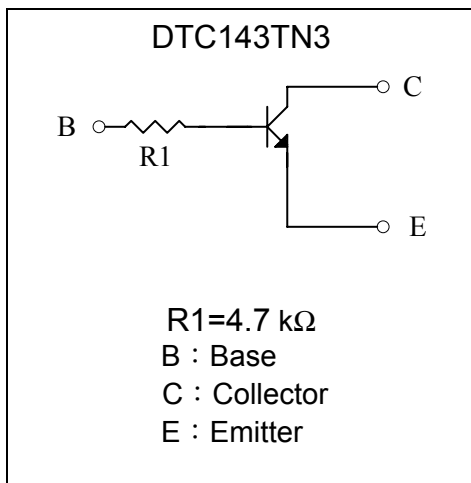
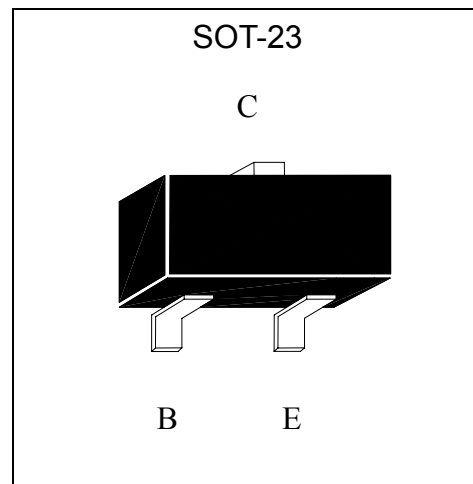


**NPN Digital Transistors (Built-in Resistors)**

# DTC143TN3

**Features**

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTA143TN3
- Pb-free lead plating and halogen-free package

**Equivalent Circuit**

**Outline**

**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	$V_{CBO}$	50	V
Collector-Emitter Voltage	$V_{CEO}$	50	V
Emitter-Base Voltage	$V_{EBO}$	5	V
Collector Current	$I_C$	100	mA
Power Dissipation	$P_d$	200	mW
Junction Temperature	$T_j$	150	°C
Storage Temperature	$T_{stg}$	-55~+150	°C



**Electrical Characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Collector-Base Breakdown Voltage	VCBO	50	-	-	V	IC=50μA
Collector-Emitter Breakdown Voltage	VCEO	50	-	-	V	IC=1mA
Emitter-Base Breakdown Voltage	VEBO	5	-	-	V	IE=50μA
Collector-Base Cutoff Current	ICBO	-	-	0.5	μA	VCB=50V
Emitter-Base Cutoff Current	IEBO	-	-	0.5	μA	VEB=4V
Collector-Emitter Saturation Voltage	VCE(sat)	-	-	0.3	V	IC=5mA, IB=0.25mA
DC Current Gain	hFE	100	-	600	-	VCE=5V, IC=1mA
Input Resistance	R	3.29	4.7	6.11	kΩ	-
Transition Frequency	fr	-	250	-	MHz	VCE=10V, IC=5mA, f=100MHz *

\* Transition frequency of the device

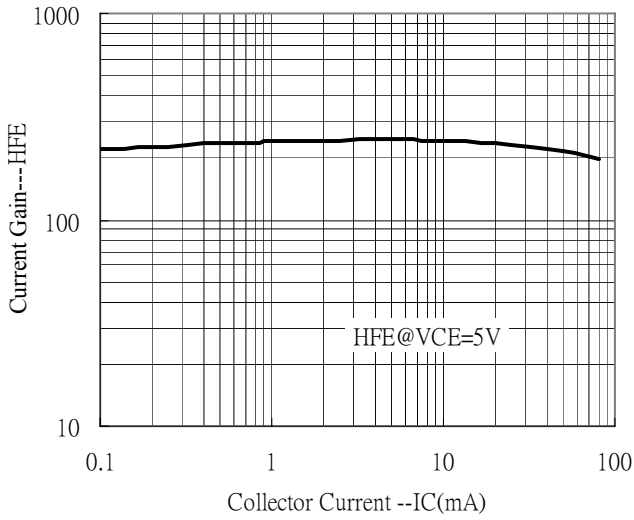
**Ordering Information**

Device	Package	Shipping	Marking
DTC143TN3	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel	8F

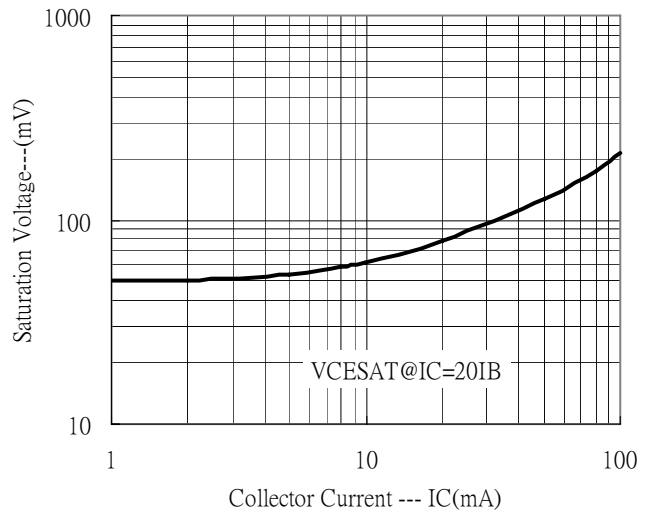


### Typical Characteristics

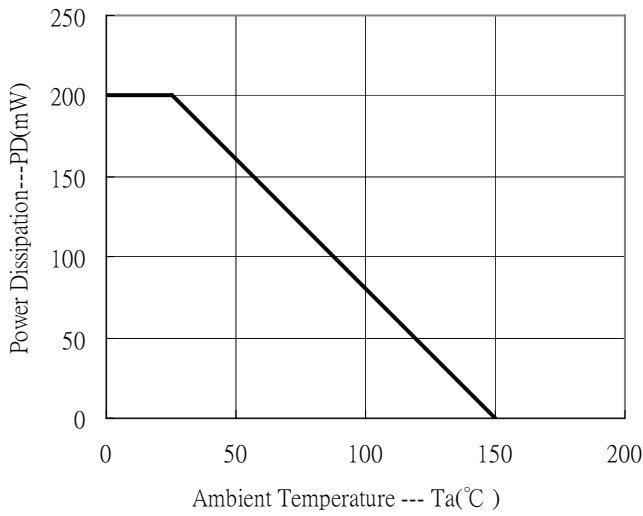
Current Gain vs Collector Current



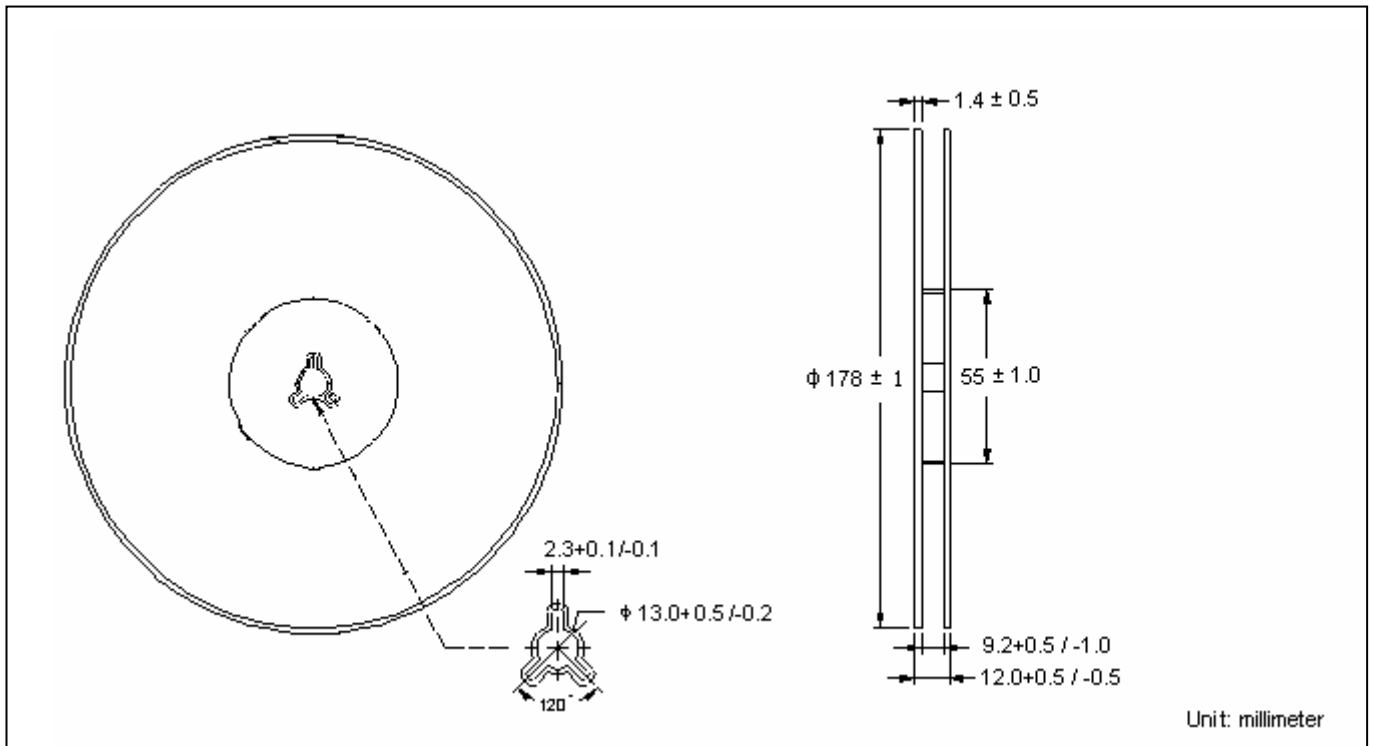
Saturation Voltage vs Collector Current



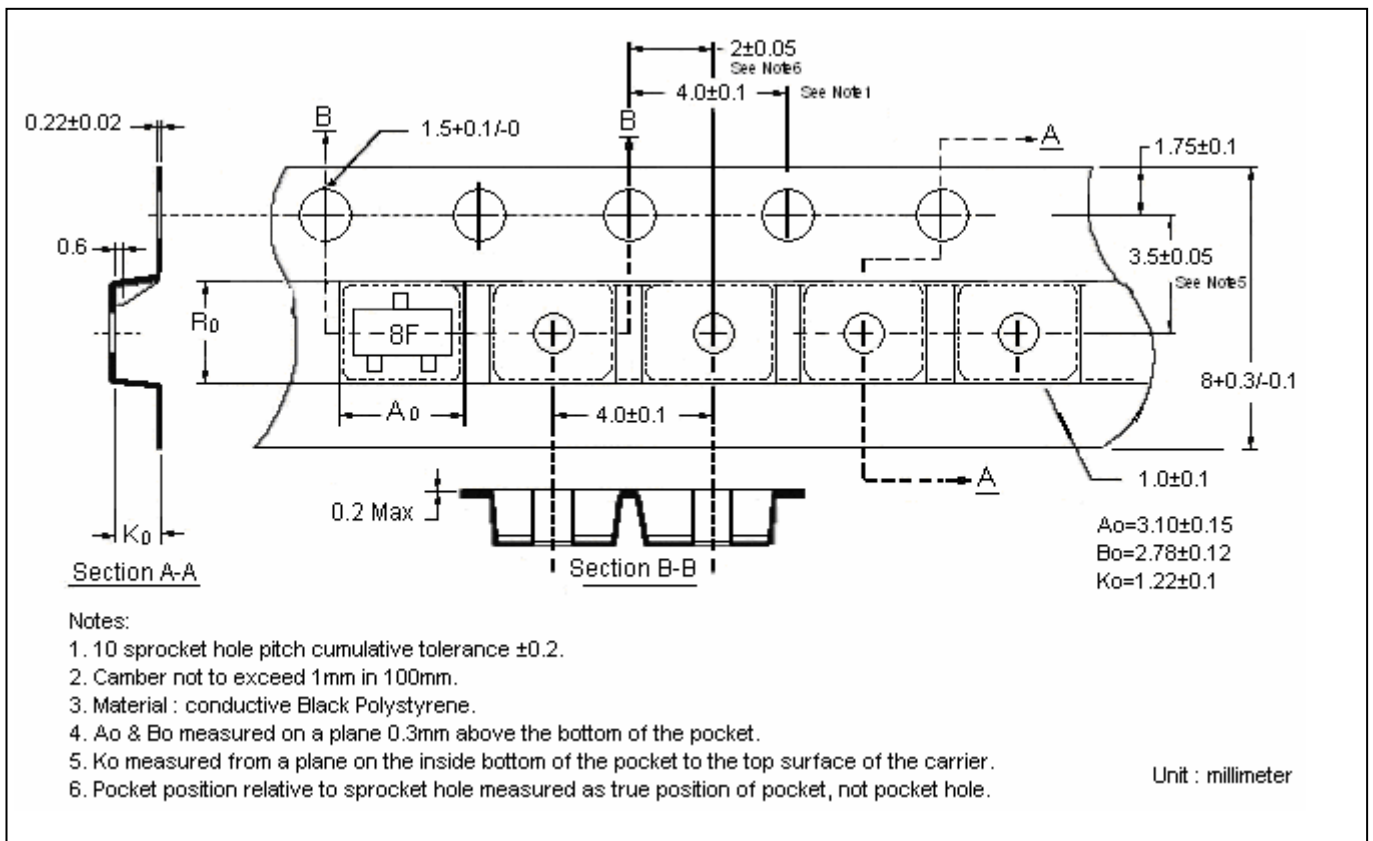
Power Derating Curve



### Reel Dimension



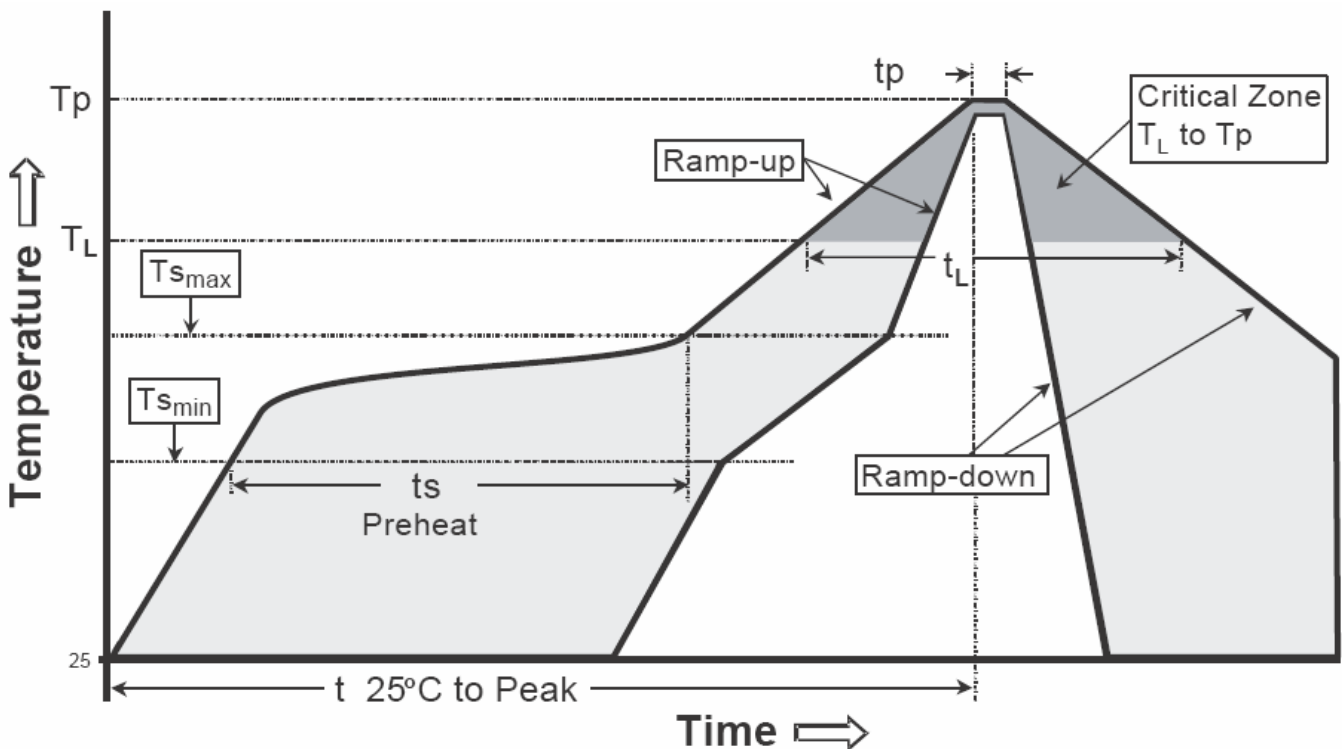
### Carrier Tape Dimension



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

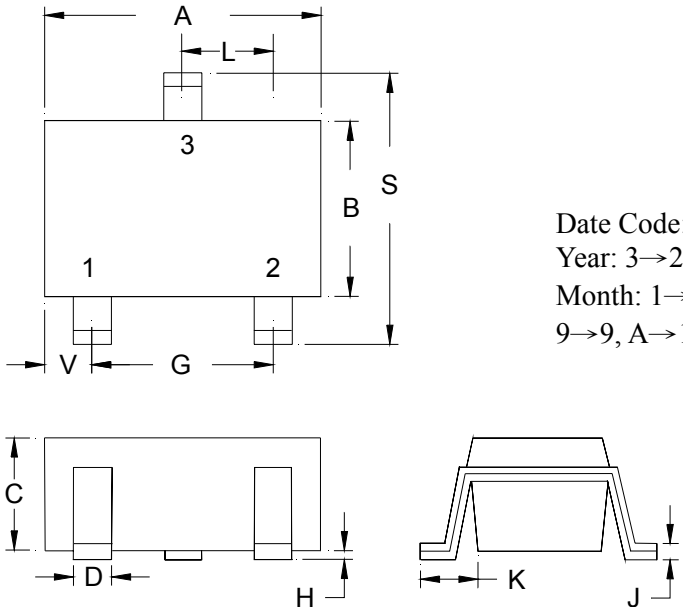
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

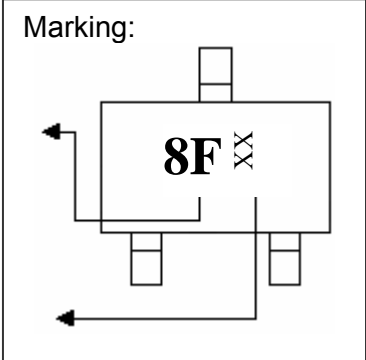
Note : All temperatures refer to topside of the package, measured on the package body surface.

**SOT-23 Dimension**



The diagram shows three views of the SOT-23 package: a top view with dimensions A, L, B, S, 1, 2, 3, V, and G; a side view with dimensions C, D, and H; and a perspective view with dimensions K and J. Lead 1 is the base, lead 2 is the emitter, and lead 3 is the collector.

**Marking:**



The marking diagram shows a rectangular package with three leads. The top lead is labeled '3', the bottom-left lead is labeled '1', and the bottom-right lead is labeled '2'. The marking '8F XX' is located in the center of the package. Arrows point to the leads from the text 'Style : Pin 1.Base 2.Emitter 3.Collector'.

**Product Code**

**Date Code: Year+Month**  
 Year: 3→2003, 4→2004  
 Month: 1→1, 2→2, . . .  
 9→9, A→10, B→11, C→12

**3-Lead SOT-23 Plastic Surface Mounted Package**  
 CYStek Package Code: N3

**Style : Pin 1.Base 2.Emitter 3.Collector**

\*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0034	0.0070	0.085	0.177
B	0.0472	0.0630	1.20	1.60	K	0.0128	0.0266	0.32	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1083	2.10	2.75
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0005	0.0040	0.013	0.10					

- Notes :** 1.Controlling dimension : millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material :**

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.