

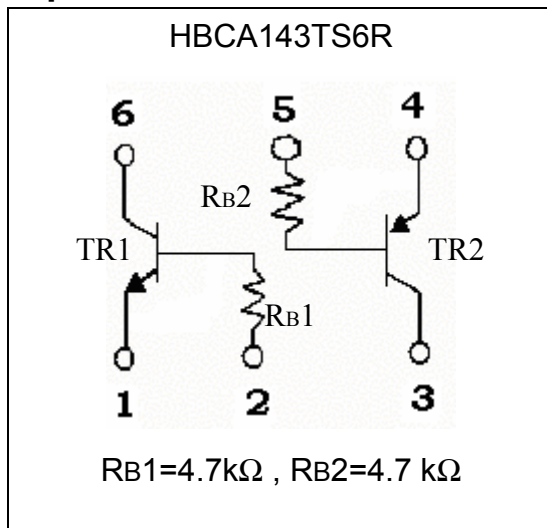
PNP and NPN Dual Digital Transistors

HBCA143TS6R

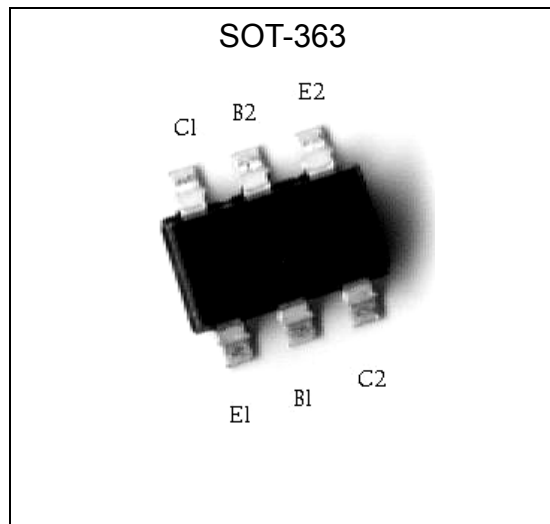
Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input for PNP transistor, and negative biasing of the input for NPN transistor. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- One DTA143T chip and one DTC143T chip in a SOT-363 package.
- Mounting by SOT-323 automatic mounting machines is possible.
- Mounting cost and area can be cut in half.
- Transistor elements are independent, eliminating interference.
- Pb-free lead plating and halogen-free package.

Equivalent Circuit



Outline



Ordering Information

Device	Package	Shipping	Marking
HBCA143TS6R-0-T1-G	SOT-363 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel	16



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Tr1(NPN)	Tr2(PNP)	
Collector-Base Voltage	V _{CBO}	50	-50	V
Collector-Emitter Voltage	V _{CEO}	50	-50	V
Emitter-Base Voltage	V _{EBO}	5	-5	V
Collector Current	I _C	100	-100	mA
Total Power Dissipation	P _d	200 (Note)		mW
Junction Temperature	T _j	150		°C
Storage Temperature	T _{stg}	-55~+150		°C

Note : 150mW per element must not be exceeded.

Characteristics (Ta=25°C)

•Tr1(NPN)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Collector-Base Breakdown Voltage	V _{CBO}	50	-	-	V	I _C =50μA
Collector-Emitter Breakdown Voltage	V _{CEO}	50	-	-	V	I _C =1mA
Emitter-Base Breakdown Voltage	V _{EBO}	5	-	-	V	I _E =50μA
Collector-Base Cutoff Current	I _{CBO}	-	-	0.5	μA	V _{CB} =50V
Emitter-Base Cutoff Current	I _{EBO}	-	-	0.5	μA	V _{EB} =4V
Collector-Emitter Saturation Voltage	V _{CE(sat)}	-	-	0.3	V	I _C =5mA, I _B =0.25mA
DC Current Gain	h _{FE}	100	-	600	-	V _{CE} =5V, I _C =1mA
Input Resistance	R	3.29	4.7	6.11	kΩ	-
Transition Frequency	f _T	-	250	-	MHz	V _{CE} =10V, I _E =5mA, f=100MHz*

* Transition frequency of the device

•Tr2(PNP)

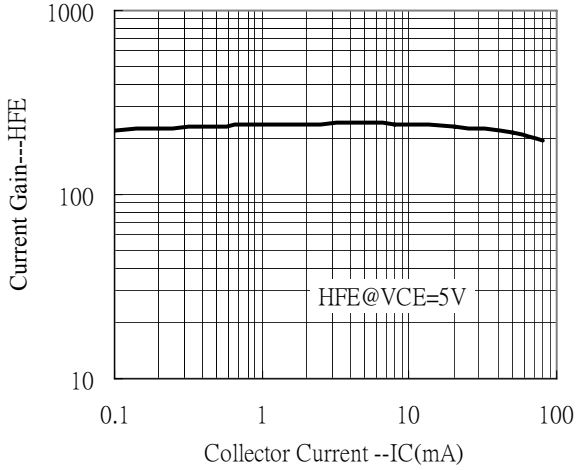
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Collector-Base Breakdown Voltage	BV _{CBO}	-50	-	-	V	I _C =-50μA
Collector-Emitter Breakdown Voltage	BV _{CEO}	-50	-	-	V	I _C =-1mA
Emitter-Base Breakdown Voltage	BV _{EBO}	-5	-	-	V	I _E =-50μA
Collector-Base Cutoff Current	I _{CBO}	-	-	-0.5	μA	V _{CB} =-50V
Emitter-Base Cutoff Current	I _{EBO}	-	-	-0.5	μA	V _{EB} =-4V
Collector-Emitter Saturation Voltage	V _{CE(sat)}	-	0.1	-0.3	V	I _C =-5mA, I _B =-0.25mA
DC Current Gain	h _{FE}	100	-	600	-	V _{CE} =-5V, I _C =-1mA
Input Resistance	R	3.29	4.7	6.11	kΩ	-
Transition Frequency	f _T	-	250	-	MHz	V _{CE} =-10V, I _C =-5mA, f=100MHz *

* Transition frequency of the device

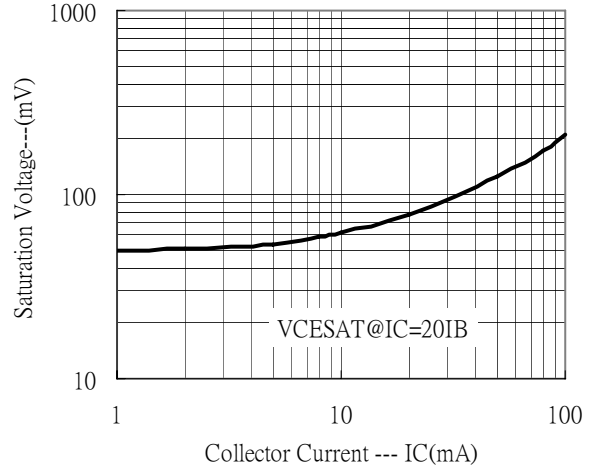
Typical Characteristics

•Tr1(NPN)

Current Gain vs Collector Current

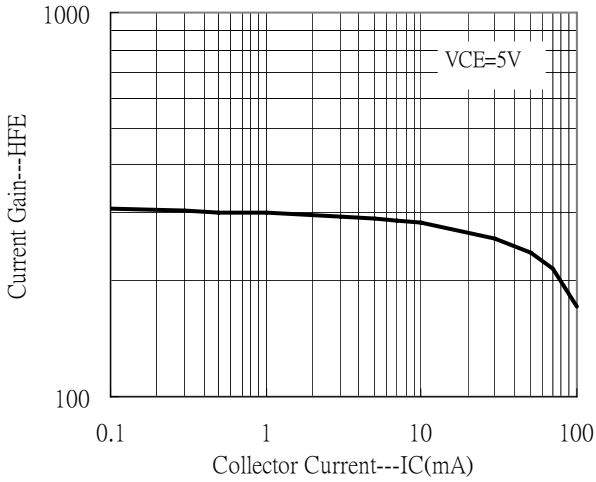


Saturation Voltage vs Collector Current

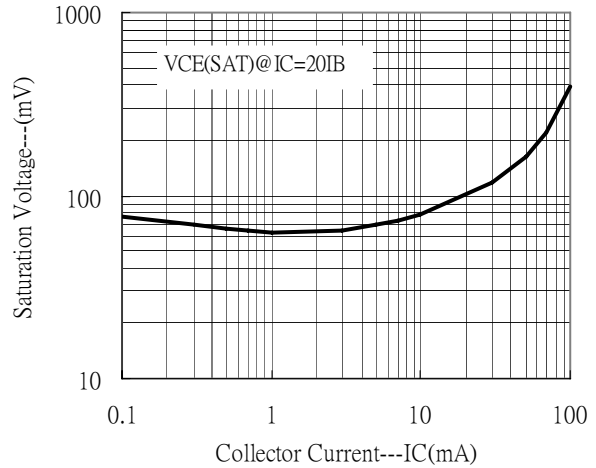


•Tr2(PNP)

Current Gain vs Collector Current

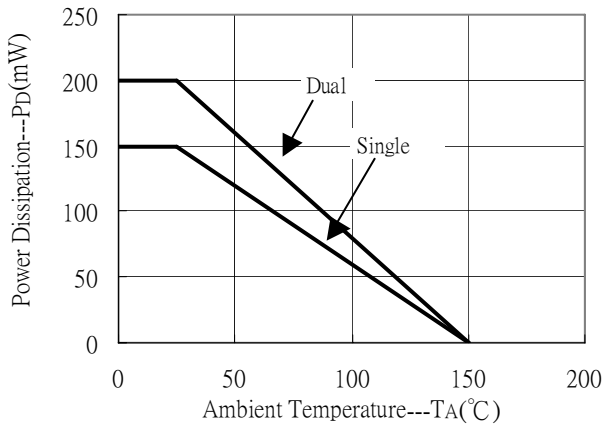


Saturation Voltage vs Collector Current

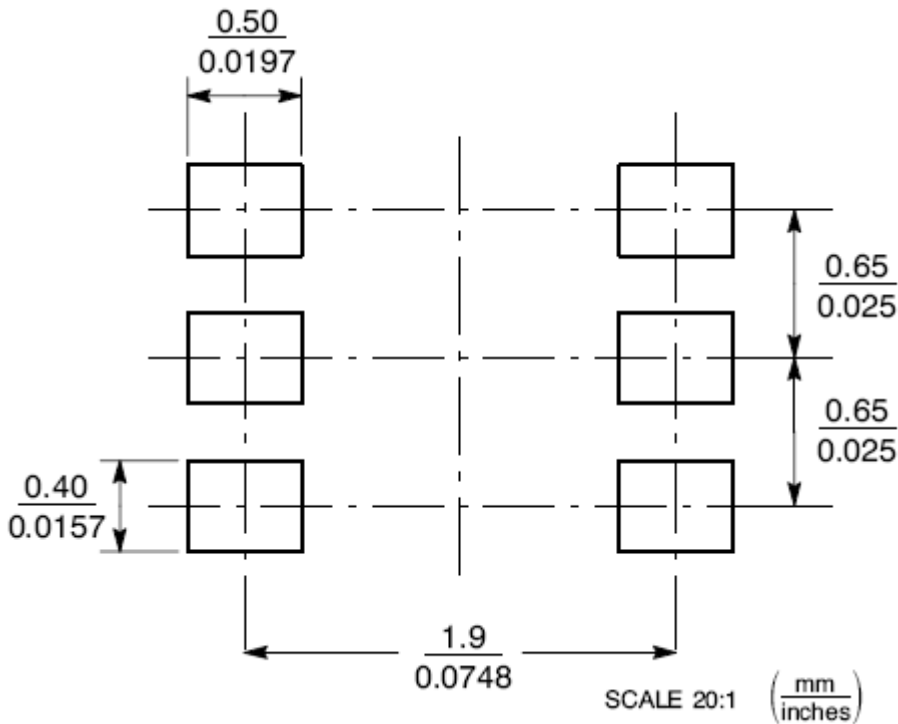


Typical Characteristics (Cont.)

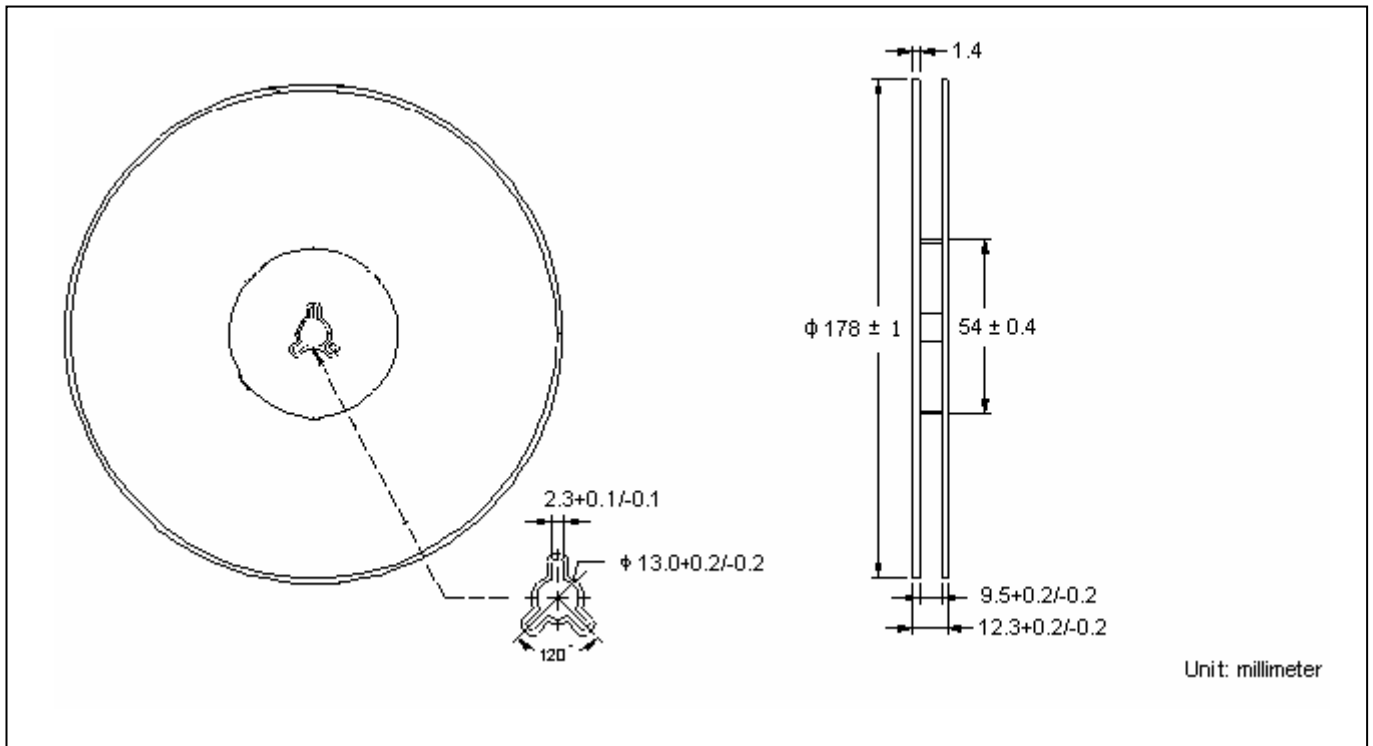
Power Derating Curves



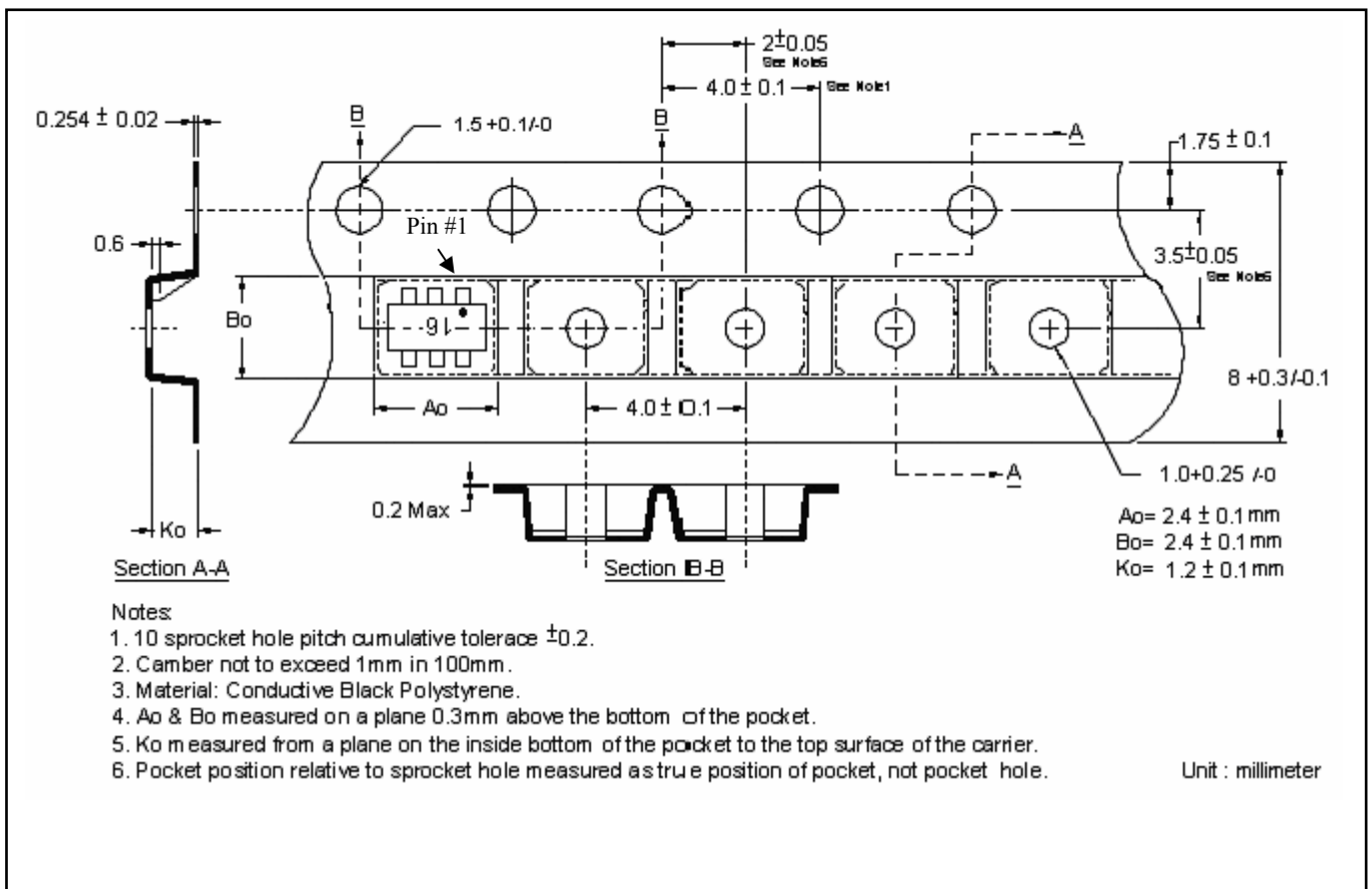
Recommended Soldering Footprint



Reel Dimension



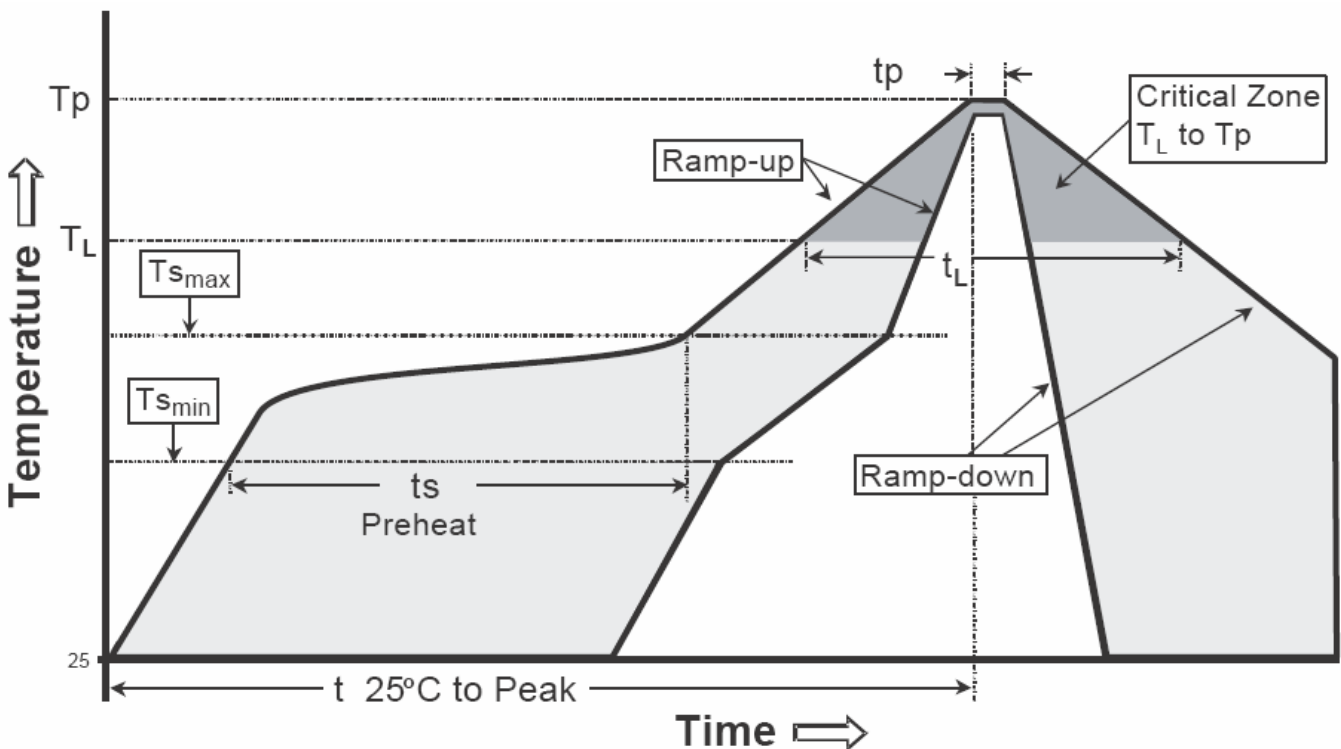
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

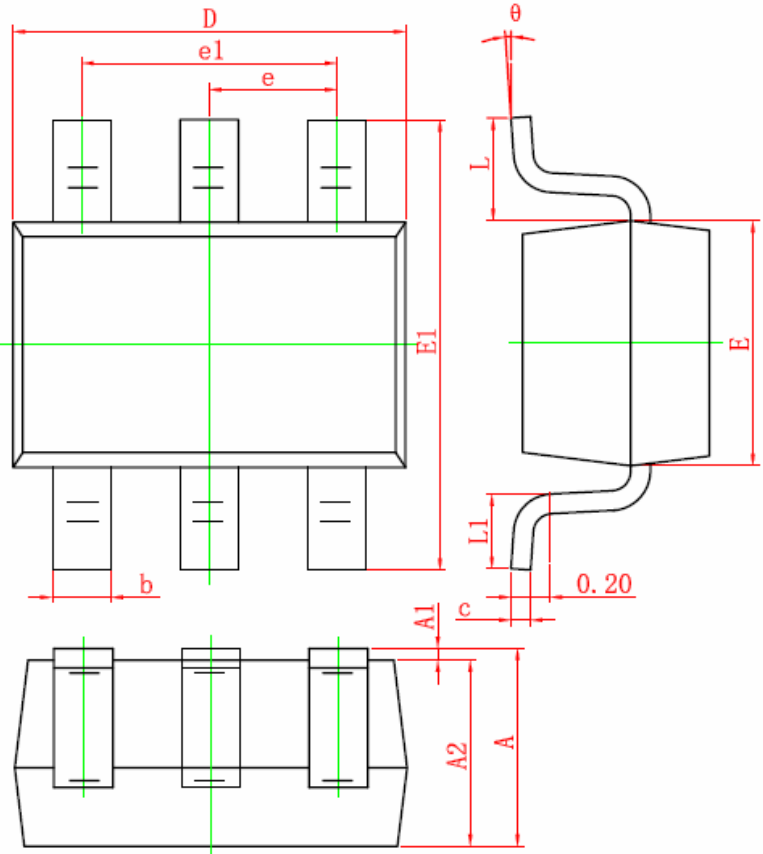
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

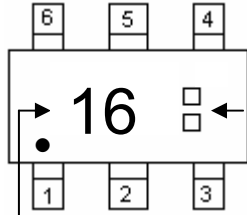
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-363 Dimension



The diagram shows three views of the SOT-363 package: a top view, a side view, and a bottom view. Dimensions are labeled with letters and numbers: D (total width), e1 (lead pitch), e (lead width), E1 (package height), b (lead width), A1 (lead height), c (lead thickness), A2 (package height), A (package height), L (lead length), L1 (lead length), and θ (lead angle). A specific lead thickness of 0.20 is indicated.

Marking:



Date Code:
 Year + Month
 Year : 6→2006,
 7→2007,..., etc
 Month : 1→Jan
 2→Feb, ..., 9→
 Sep, A→Oct, B
 →Nov, C→Dec

Device Code

6-Lead SOT-363 Plastic Surface Mounted Package
 CYStek Package Code: S6R

Style:
 Pin 1. Emitter1 (E1)
 Pin 2. Base1 (B1)
 Pin 3. Collector2 (C2)
 Pin 4. Emitter2 (E2)
 Pin 5. Base2 (B2)
 Pin 6. Collector1 (C1)

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	E1	2.150	2.450	0.085	0.096
A1	0.000	0.100	0.000	0.004	e	0.650	TYP	0.026	TYP
A2	0.900	1.000	0.035	0.039	e1	1.200	1.400	0.047	0.055
b	0.150	0.350	0.006	0.014	L	0.525	REF	0.021	REF
c	0.080	0.150	0.003	0.006	L1	0.260	0.460	0.010	0.018
D	2.000	2.200	0.079	0.087	θ	0°	8°	0°	8°
E	1.150	1.350	0.045	0.053					

Notes : 1. Controlling dimension : millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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