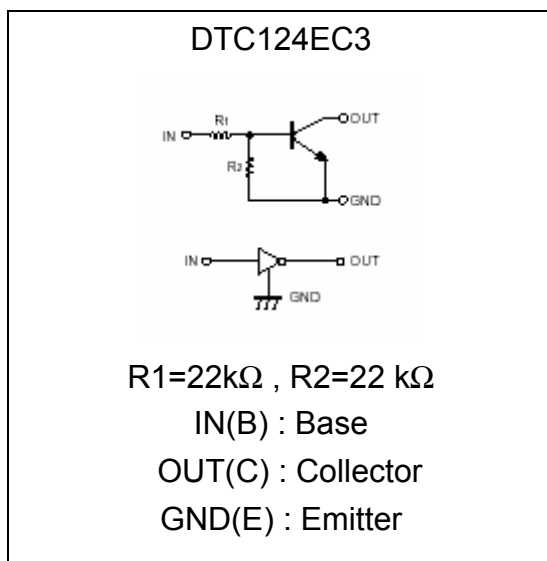
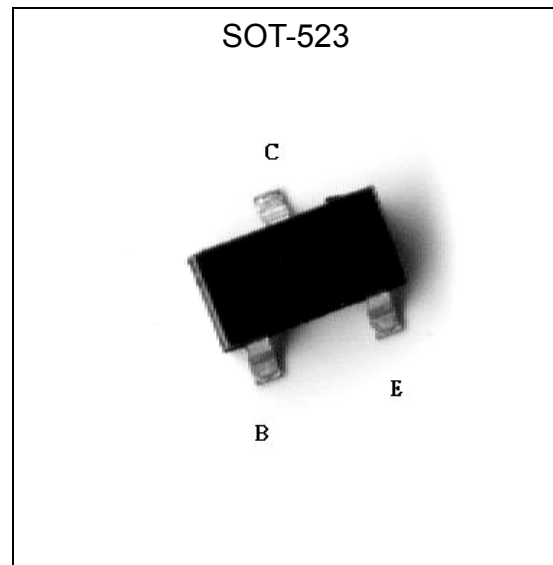


**NPN Digital Transistors (Built-in Resistors)**

# DTC124EC3

**Features**

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTA124EC3
- Pb-free lead plating and halogen-free package

**Equivalent Circuit**

**Outline**

**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Supply Voltage	V <sub>cc</sub>	50	V
Input Voltage	V <sub>in</sub>	-10~+40	V
Output Current	I <sub>o</sub>	30	mA
	I <sub>o(max.)</sub>	100	mA
Power Dissipation	P <sub>d</sub>	150	mW
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	833	°C/W
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C



**Electrical Characteristics (Ta=25°C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	Vi(off)	-	-	0.5	V	Vcc=5V, Io=100uA
	Vi(on)	3	-	-	V	Vo=0.2V, Io=5mA
Output Voltage	Vo(on)	-	0.1	0.3	V	Io/Ii=10mA/0.5mA
Input Current	Ii	-	-	0.36	mA	Vi=5V
Output Current	Io(off)	-	-	0.5	μA	Vcc=50V, Vi=0V
DC Current Gain	Gi	56	-	-	-	Vo=5V, Io=5mA
Input Resistance	R1	15.4	22	28.6	kΩ	-
Resistance Ratio	R2/R1	0.8	1	1.2	-	-
Transition Frequency	fT	-	250	-	MHz	VCE=10V, IC=5mA, f=100MHz*

\* Transition frequency of the device

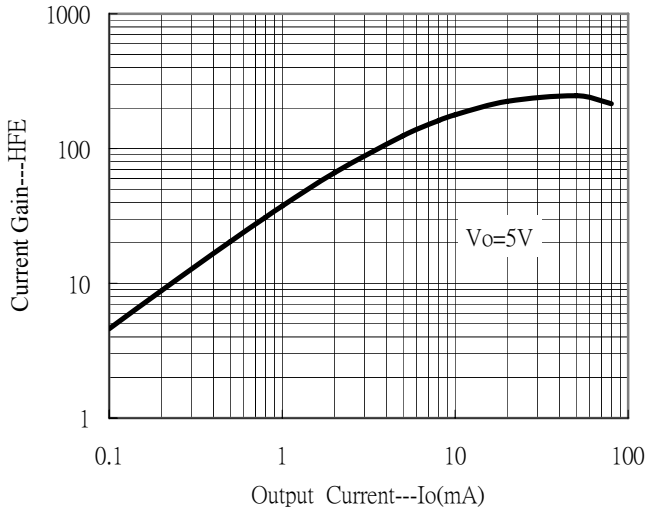
**Ordering Information**

Device	Package	Shipping	Marking
DTC124EC3	SOT-523 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel	8B

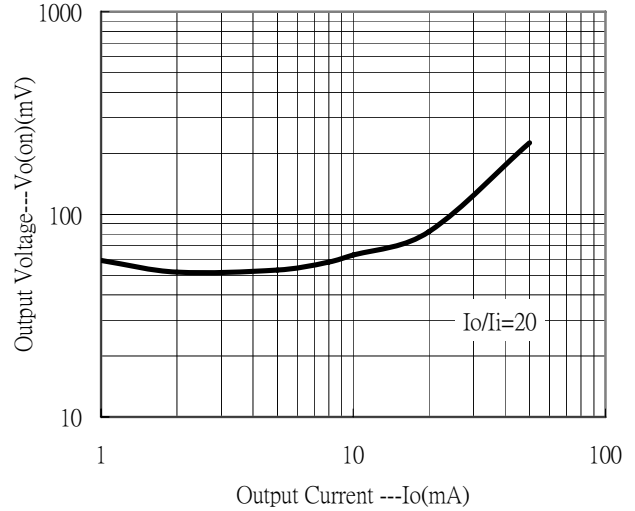


### Typical Characteristics

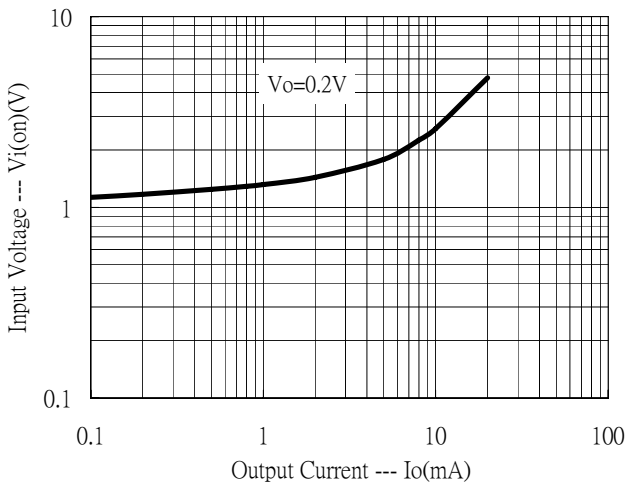
DC Current Gain vs Output Current



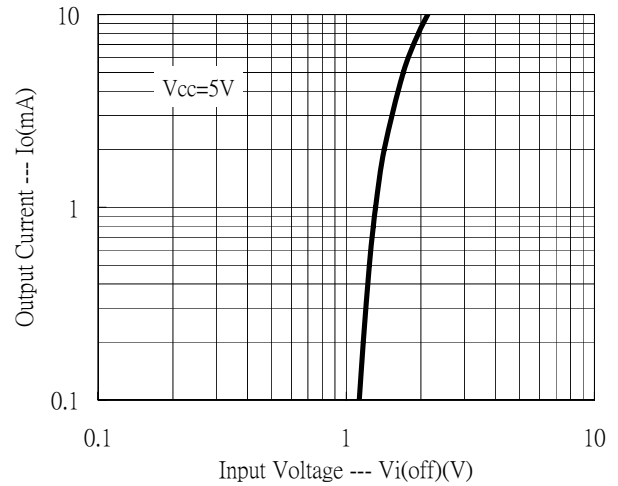
Output Voltage vs Output Current



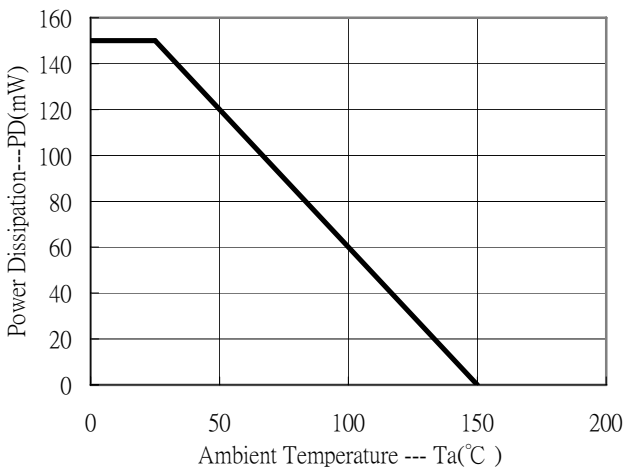
Input Voltage vs Output Current (ON Characteristics)



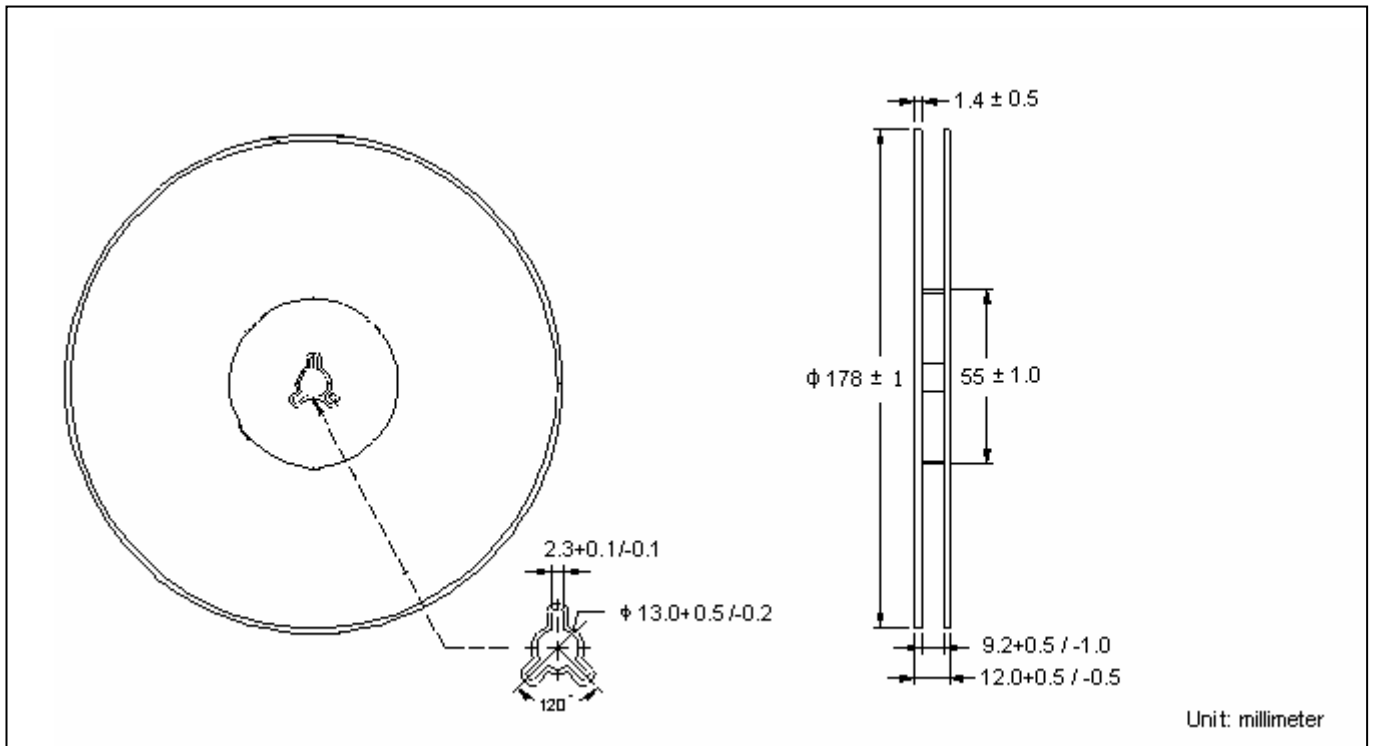
Output Current vs Input Voltage (OFF Characteristics)



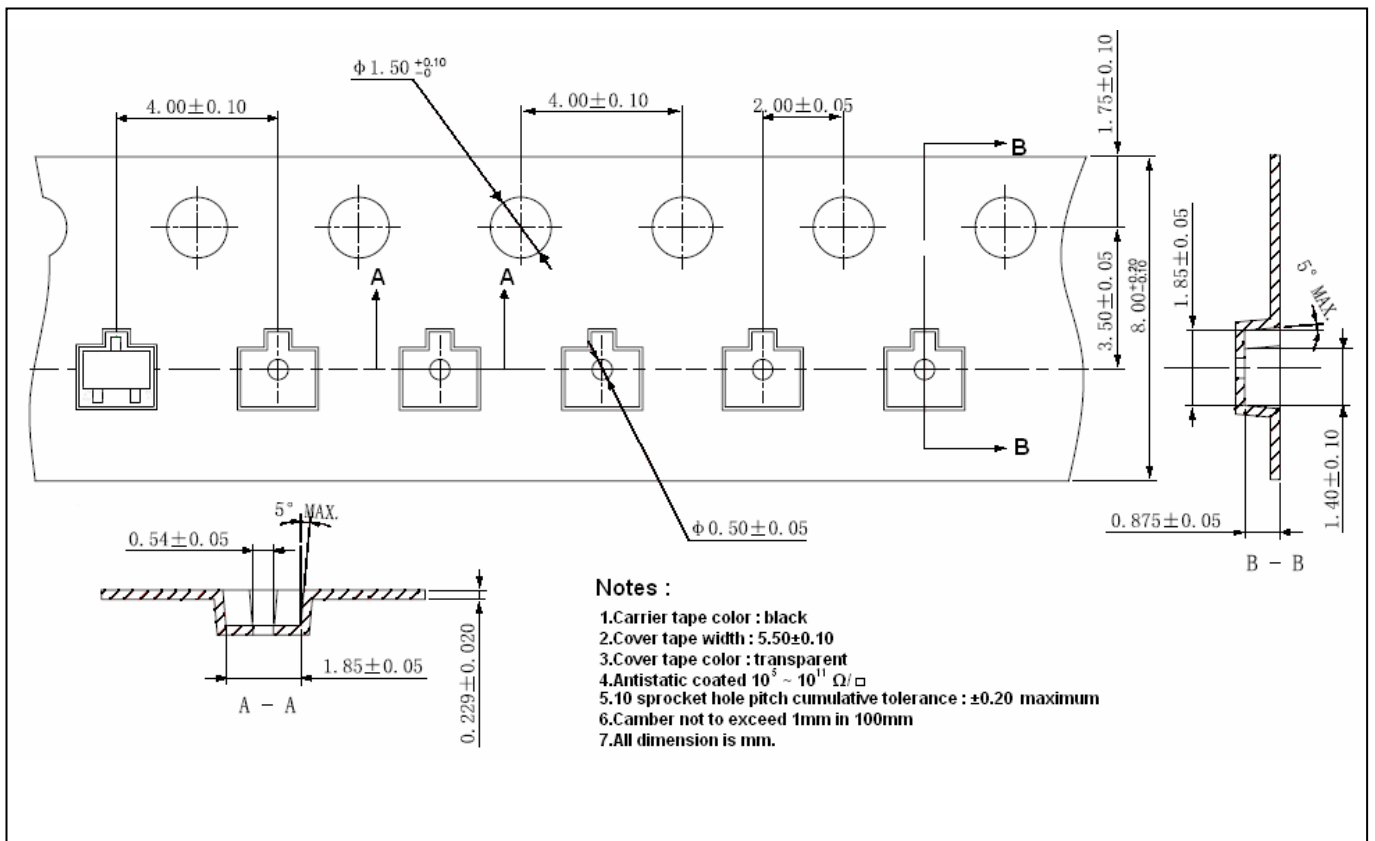
Power Derating Curve



**Reel Dimension**



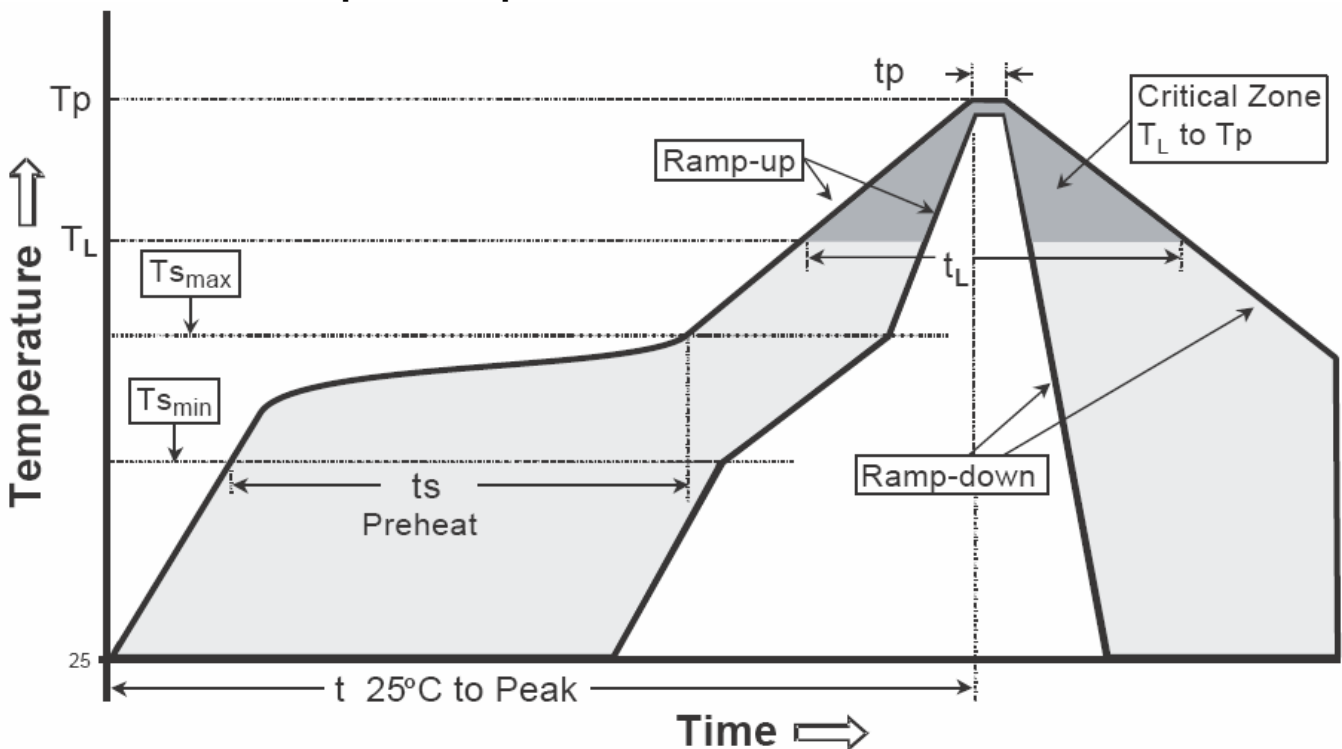
**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

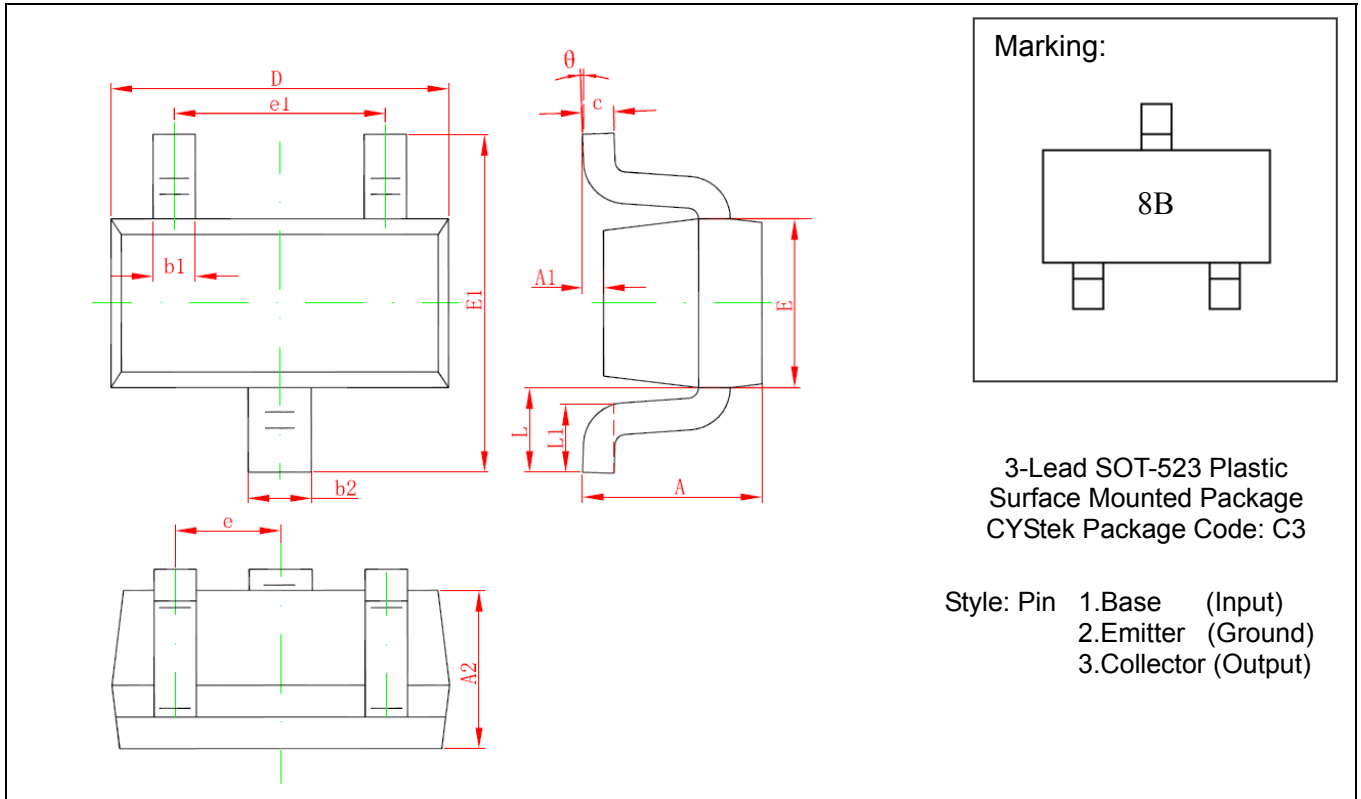
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**SOT-523 Dimension**



\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.028	0.035	0.700	0.900	E	0.028	0.035	0.700	0.900
A1	0.000	0.004	0.000	0.100	E1	0.057	0.069	1.450	1.750
A2	0.028	0.031	0.700	0.800	e	0.020*		0.500*	
b1	0.006	0.010	0.150	0.250	e1	0.035	0.043	0.900	1.100
b2	0.010	0.014	0.250	0.350	L	0.016	REF	0.400	REF
c	0.004	0.008	0.100	0.200	L1	0.010	0.018	0.260	0.460
D	0.059	0.067	1.500	1.700	θ	0°	8°	0°	8°

Notes: 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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