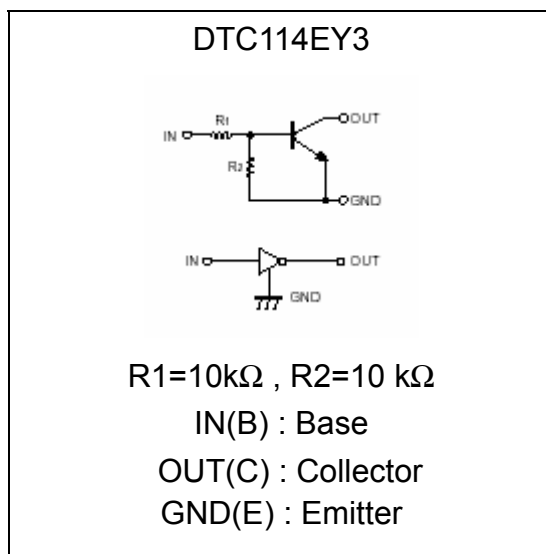
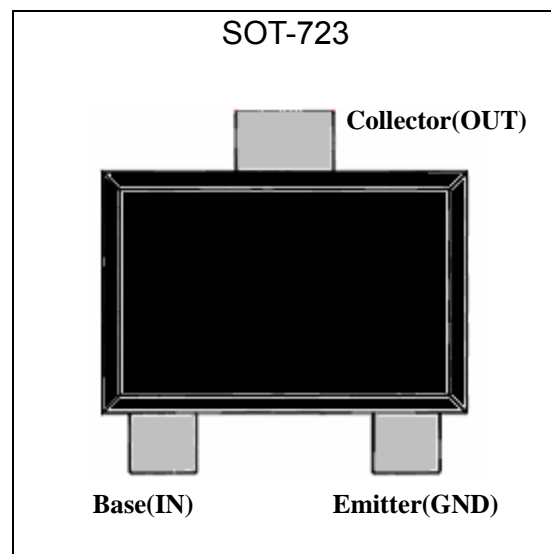


NPN Digital Transistors (Built-in Resistors)

DTC114EY3

Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTA114EY3
- Pb-free package

Equivalent Circuit

Outline

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	V _{CC}	50	V
Input Voltage	V _I	-10~+40	V
Output Current	I _O	50	mA
	I _{O(max.)}	100	mA
Power Dissipation	P _d	150	mW
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C



Electrical Characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	V _{I(off)}	-	-	0.5	V	V _{CC} =5V, I _O =100μA
	V _{I(on)}	3	-	-	V	V _O =0.3V, I _O =10mA
Output Voltage	V _{O(on)}	-	-	0.3	V	I _O /I _I =10mA/0.5mA
Input Current	I _I	-	-	0.88	mA	V _I =5V
Output Current	I _{O(off)}	-	-	0.5	μA	V _{CC} =50V, V _I =0V
DC Current Gain	G _I	30	-	-	-	V _O =5V, I _O =5mA
Input Resistance	R _I	7	10	13	kΩ	-
Resistance Ratio	R ₂ /R ₁	0.8	1	1.2	-	-
Transition Frequency	f _T	-	250	-	MHz	V _{CE} =10V, I _C =5mA, f=100MHz *

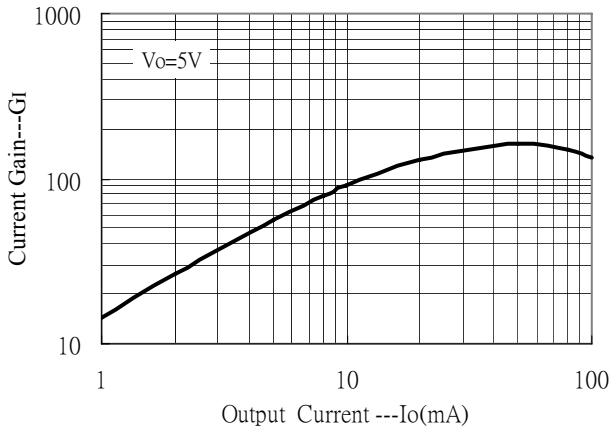
* Transition frequency of the device

Ordering Information

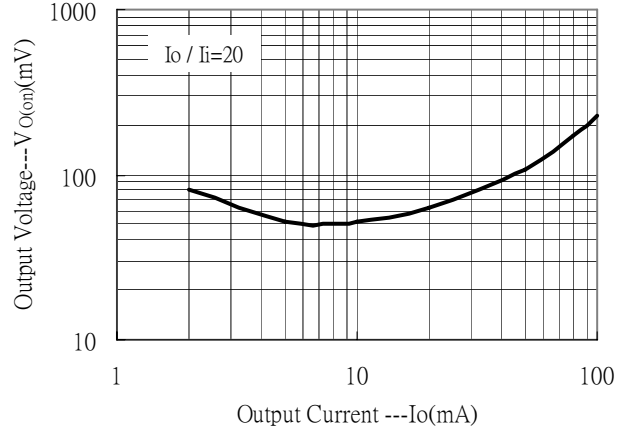
Device	Package	Shipping	Marking
DTC114EY3	SOT-723 (Pb-free)	8000 pcs / Tape & Reel	8A

Typical Characteristics

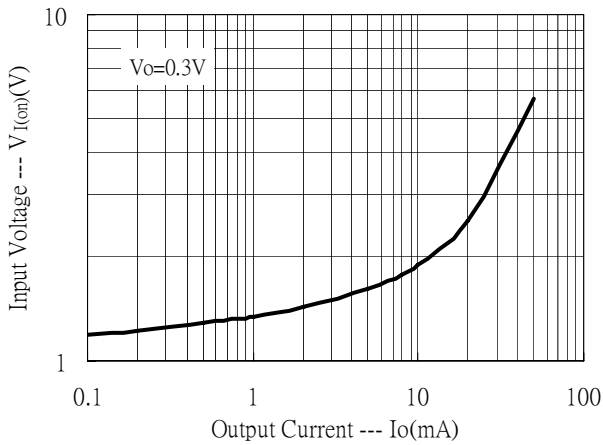
Current Gain vs Output Current



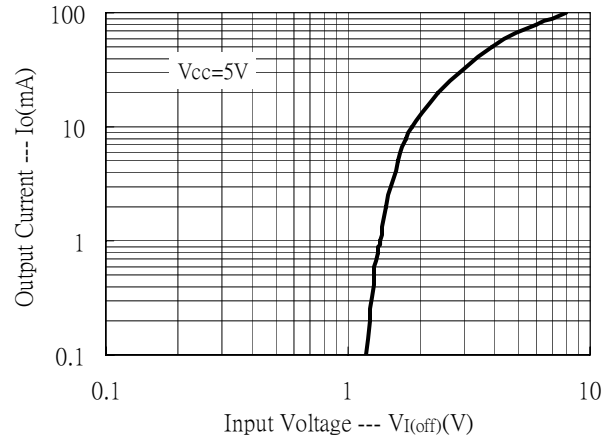
Output Voltage vs Output Current



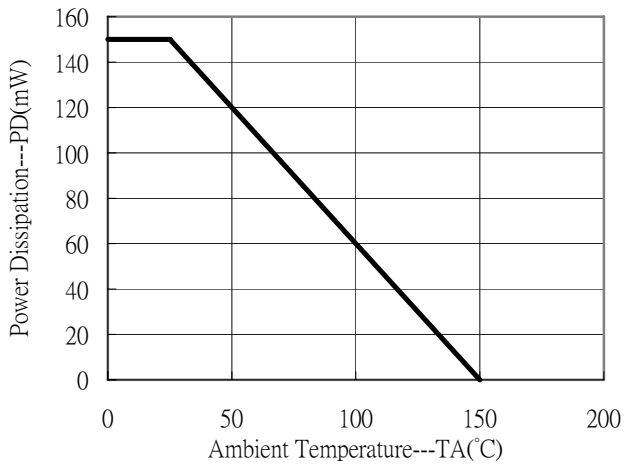
Input Voltage vs Output Current (ON characteristics)



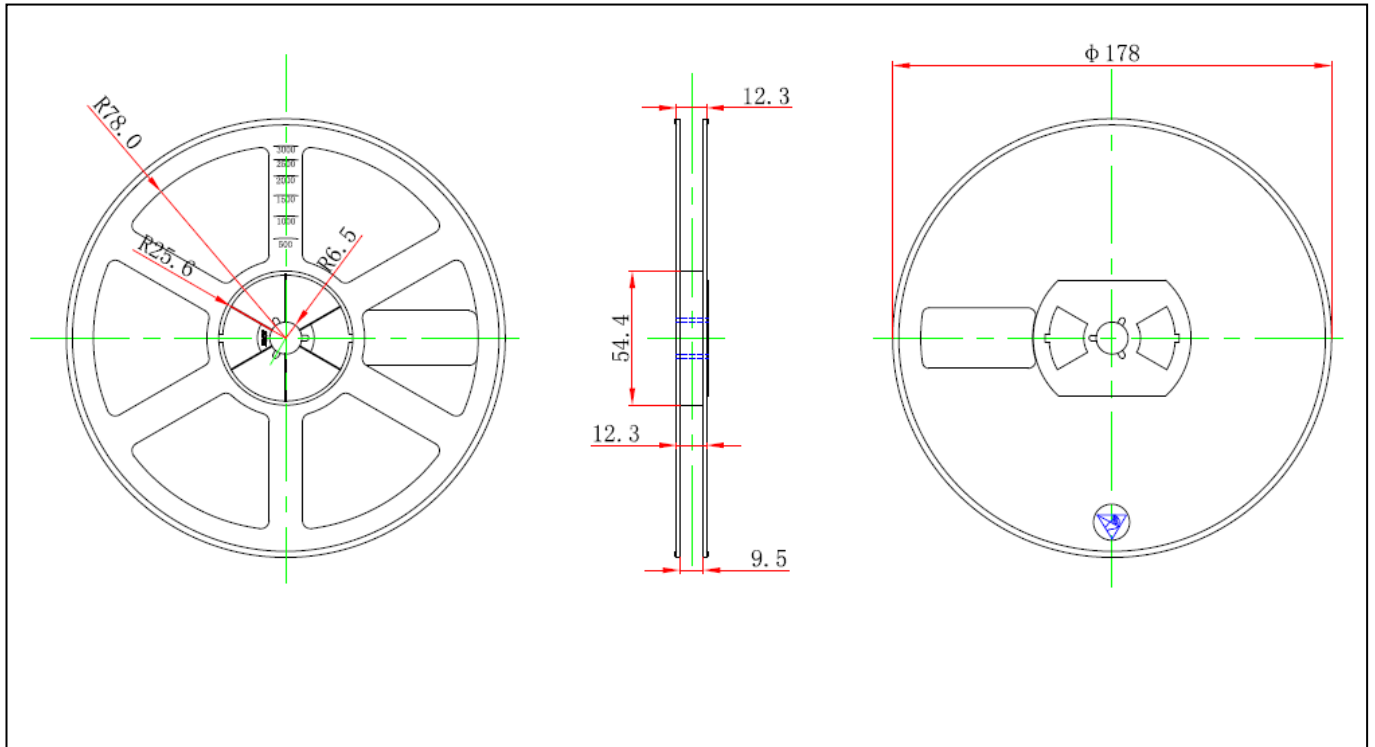
Output Current vs Input Voltage (OFF characteristics)



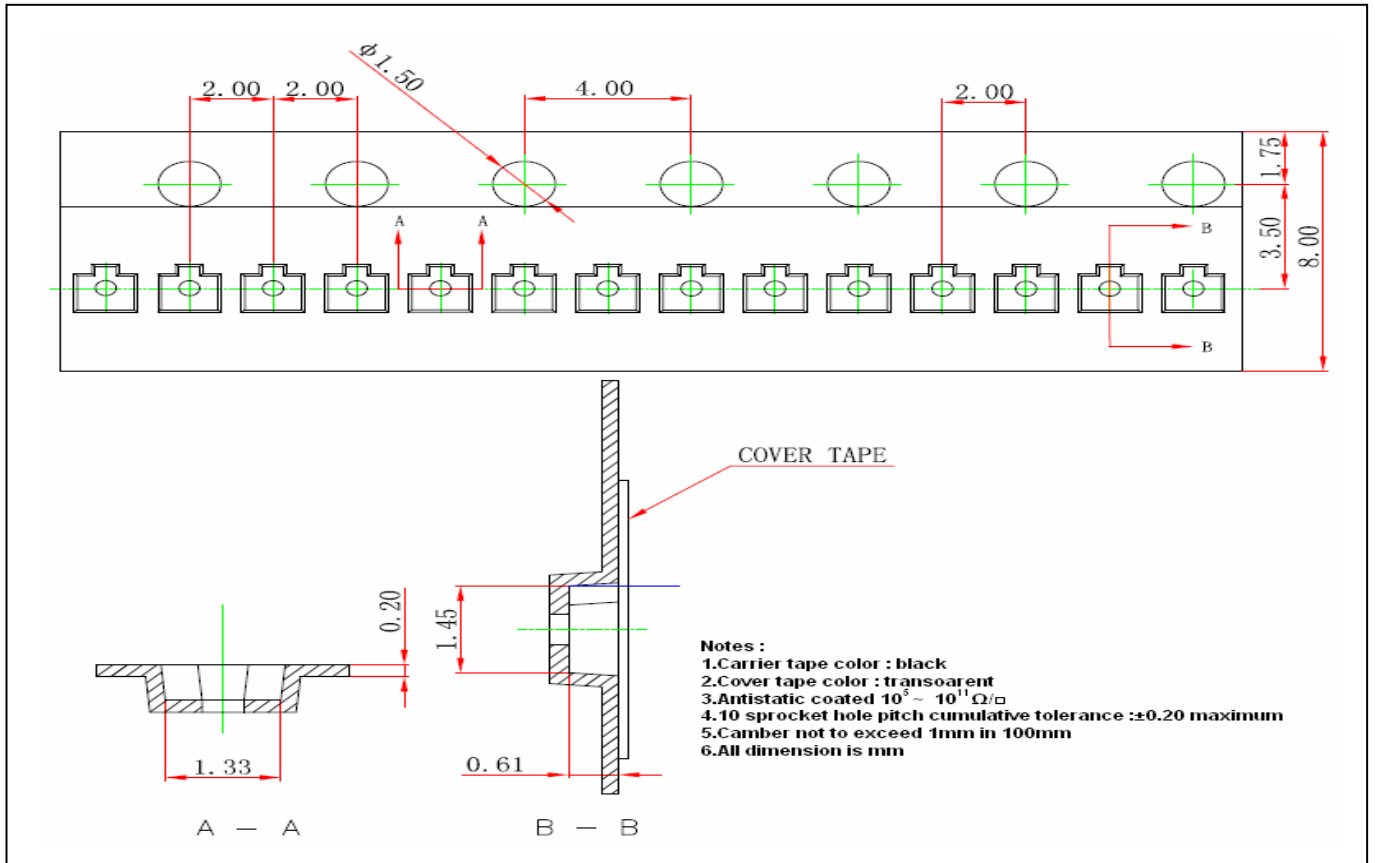
Power Derating Curve



Reel Dimension



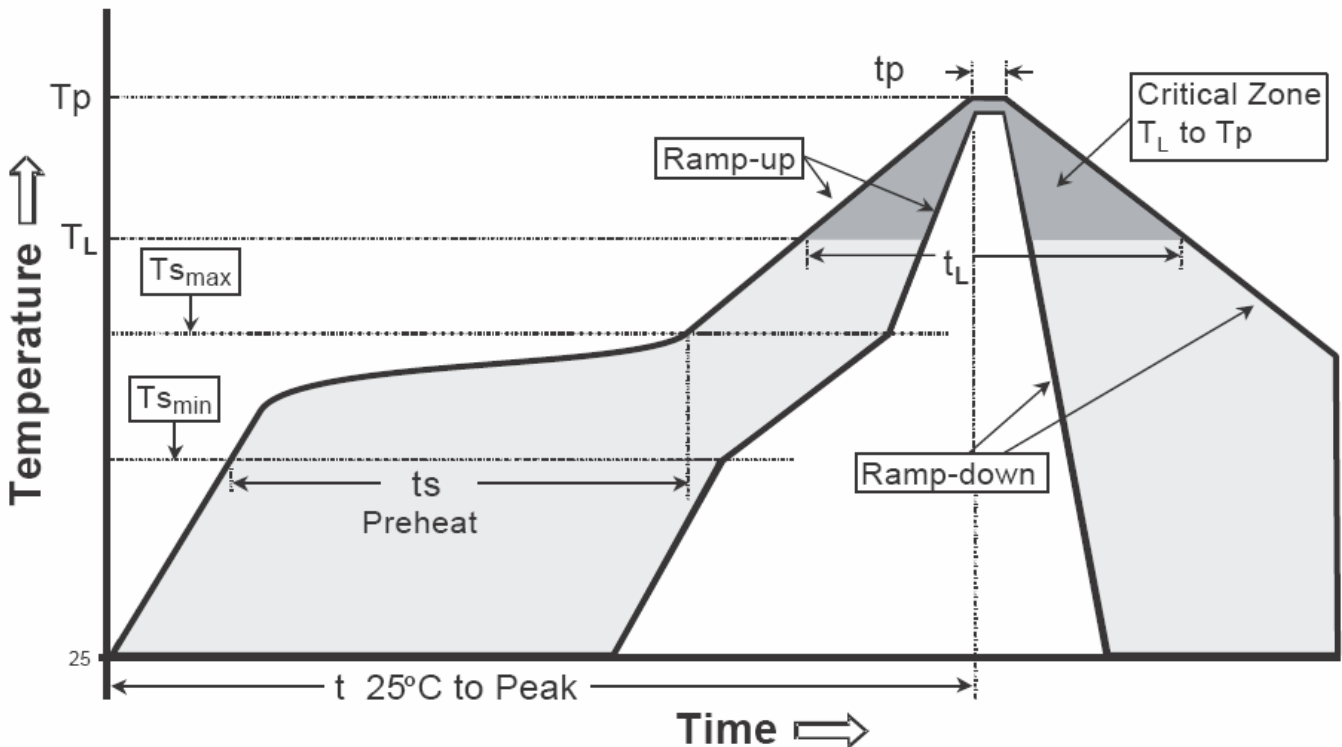
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

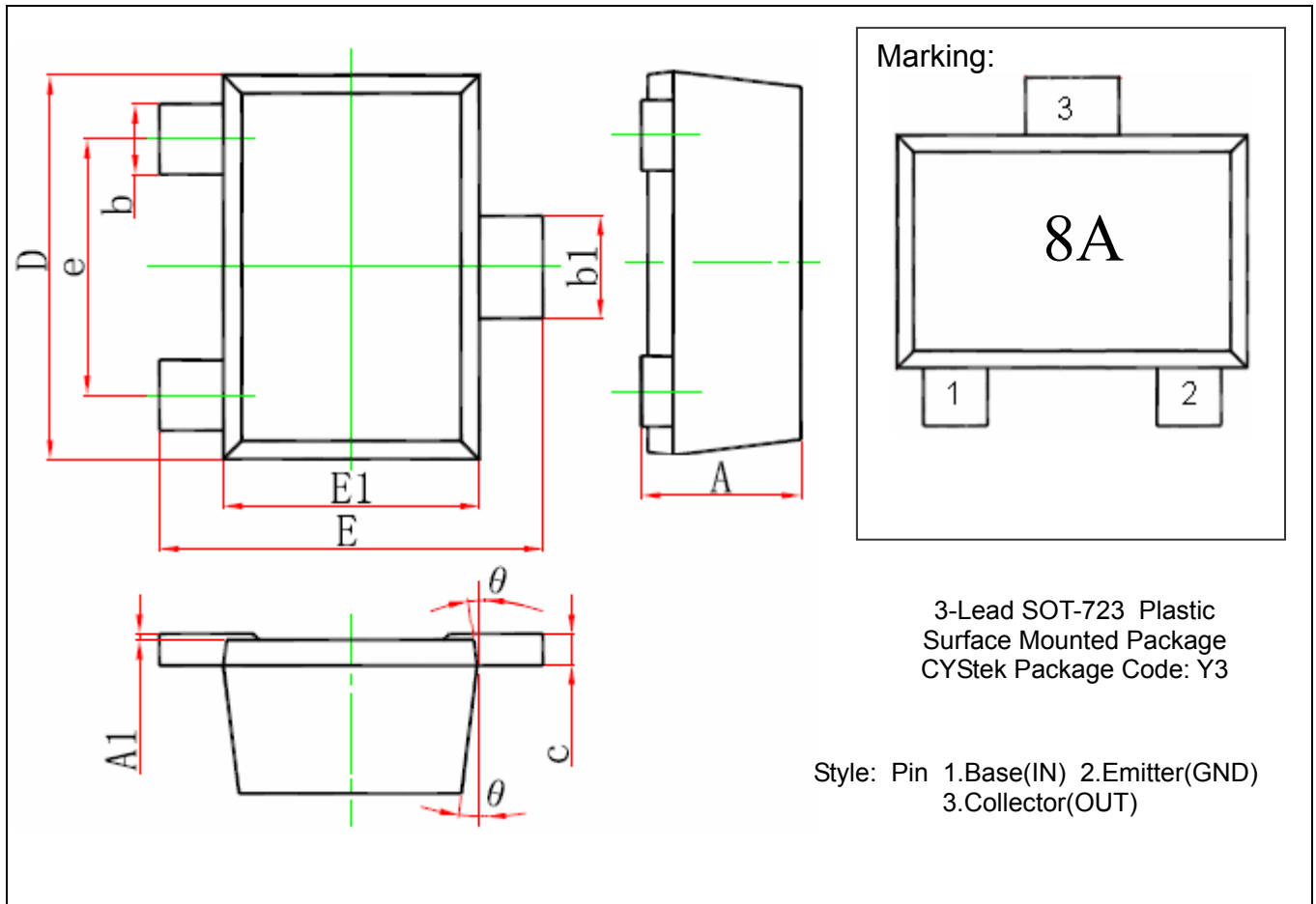
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-723 Dimension



*Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.000	0.500	0.000	0.020	D	1.150	1.250	0.045	0.049
A1	0.000	0.050	0.000	0.002	E	1.150	1.250	0.045	0.049
b	0.170	0.270	0.007	0.011	E1	0.750	0.850	0.030	0.033
b1	0.270	0.370	0.011	0.015	e	0.800*		0.031*	
c	0.000	0.150	0.000	0.006	θ	7° REF		7° REF	

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.