

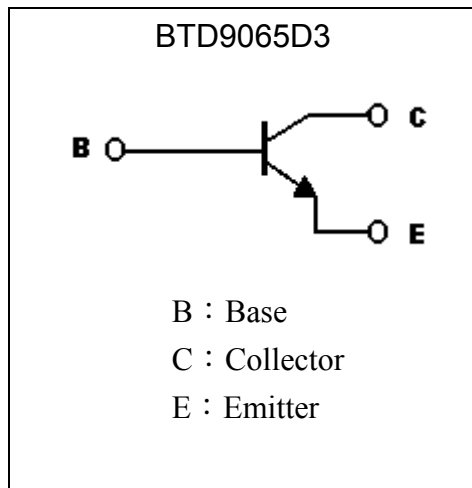
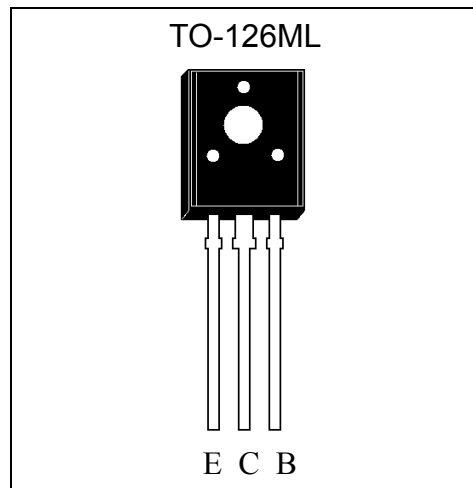
Low Vcesat NPN Epitaxial Planar Transistor

BTD9065D3

BV_{CEO}	20V
I_C	5A
R_{CESAT}	160m Ω (typ.)

Features

- Low $V_{CE(sat)}$, $V_{CE(sat)}=0.65$ V (typical), at $I_C / I_B = 4A / 0.1A$
- Excellent current gain characteristics
- Pb-free lead plating package

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CES}	40	V
Collector-Emitter Voltage	V_{CEO}	20	V
Emitter-Base Voltage	V_{EBO}	8	V
Collector Current(DC)	I_C	5	A
Collector Current(Pulse)	I_{CP}	10 *1	
Power Dissipation($T_A=25^\circ\text{C}$)	P_D	1.5	W
Power Dissipation($T_C=25^\circ\text{C}$)		10	
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55~+150	$^\circ\text{C}$

Note : *1. Single Pulse , $P_w \leq 380\mu\text{s}$, Duty $\leq 2\%$.

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	12.5	$^{\circ}C/W$
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	83.3	$^{\circ}C/W$

Characteristics (Ta=25°C)

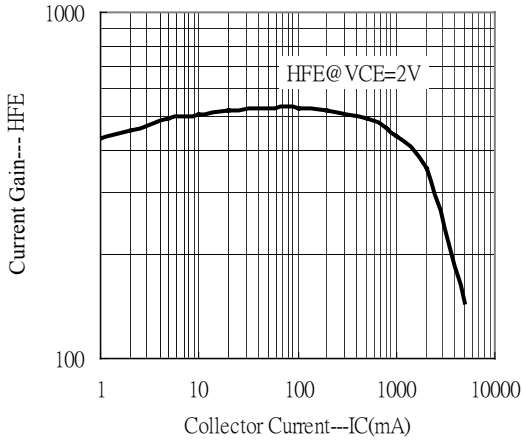
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	50	-	-	V	$I_C=50\mu A, I_E=0$
BV_{CES}	40	-	-	V	$I_C=50\mu A, V_{BE}=0$
BV_{CEO}	20	-	-	V	$I_C=1mA, I_B=0$
BV_{EBO}	8	-	-	V	$I_E=50\mu A, I_C=0$
I_{CBO}	-	-	100	nA	$V_{CB}=50V, I_E=0$
I_{CES}	-	-	100	nA	$V_{CE}=40V, I_E=0$
I_{EBO}	-	-	100	nA	$V_{EB}=8V, I_C=0$
* $V_{CE(sat)}$	-	0.65	1	V	$I_C=4A, I_B=0.1A$
* $R_{CE(sat)}$	-	160	250	$m\Omega$	$I_C=4A, I_B=0.1A$
* $V_{BE(on)}$	-	-	1.5	V	$V_{CE}=2V, I_C=4A$
* h_{FE}	300	-	600	-	$V_{CE}=2V, I_C=0.5A$
* h_{FE}	80	-	-	-	$V_{CE}=2V, I_C=4A$
f_T	-	150	-	MHz	$V_{CE}=6V, I_C=50mA, f=100MHz$
Cob	-	35	-	pF	$V_{CB}=20V, f=1MHz$

*Pulse Test : Pulse Width $\leq 380\mu s$, Duty Cycle $\leq 2\%$ **Ordering Information**

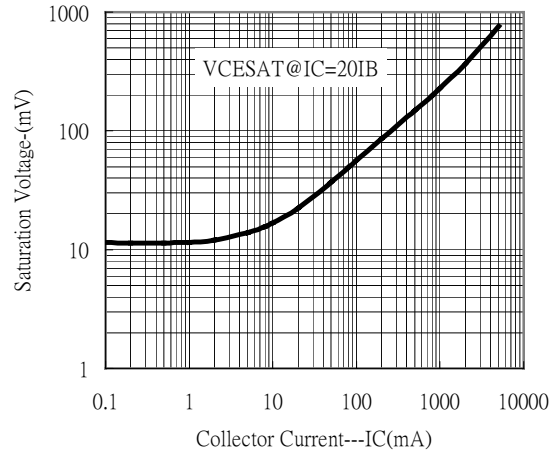
Device	Package	Shipping
BTD9065D3	TO-126ML (Pb-free lead plating package)	200 pcs / bag, 15 bags/box, 10 boxes/carton

Characteristic Curves

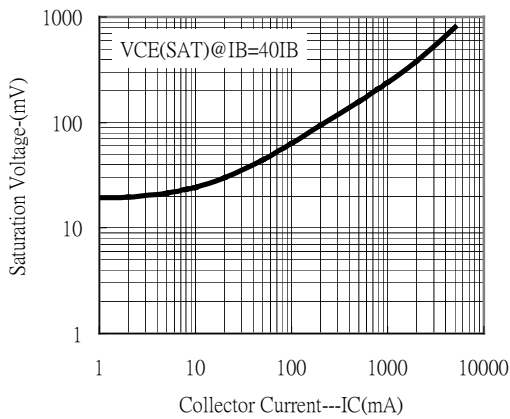
Current Gain vs Collector Current



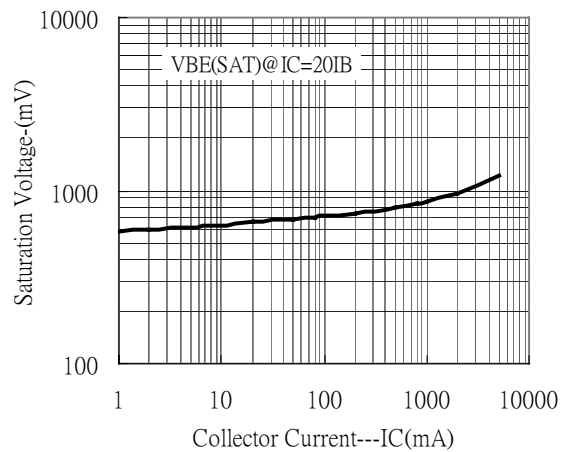
Saturation Voltage vs Collector Current



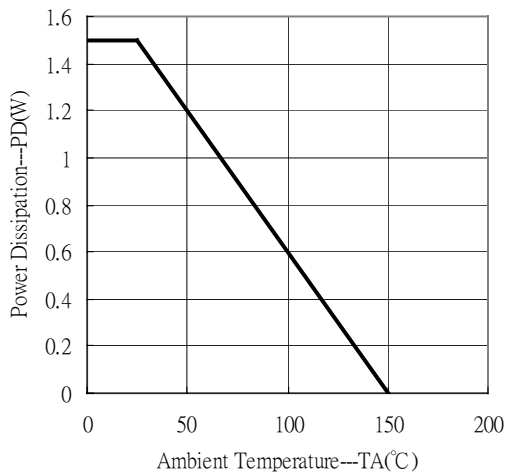
Saturation Voltage vs Collector Current



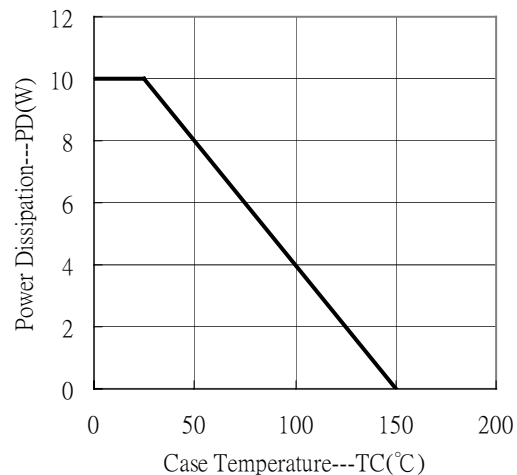
Saturation Voltage vs Collector Current



Power Derating Curve

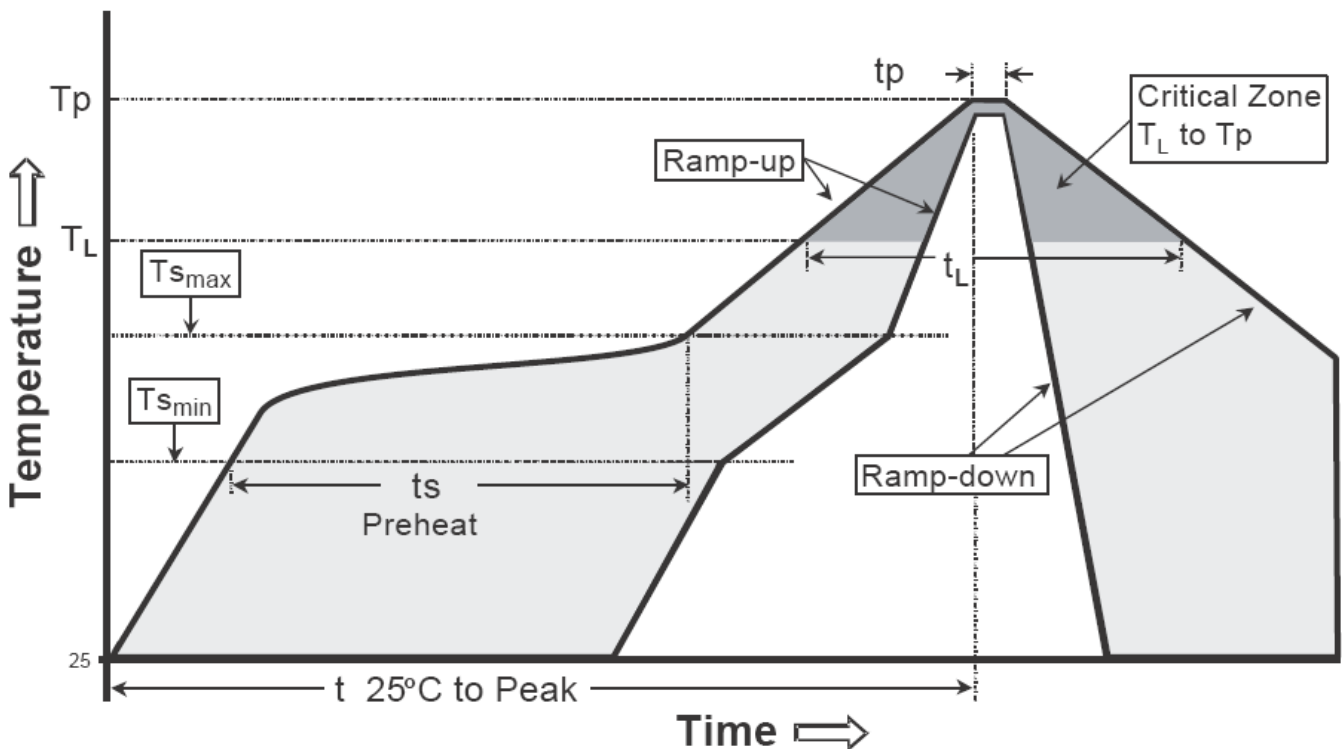


Power Derating Curve



Recommended wave soldering condition

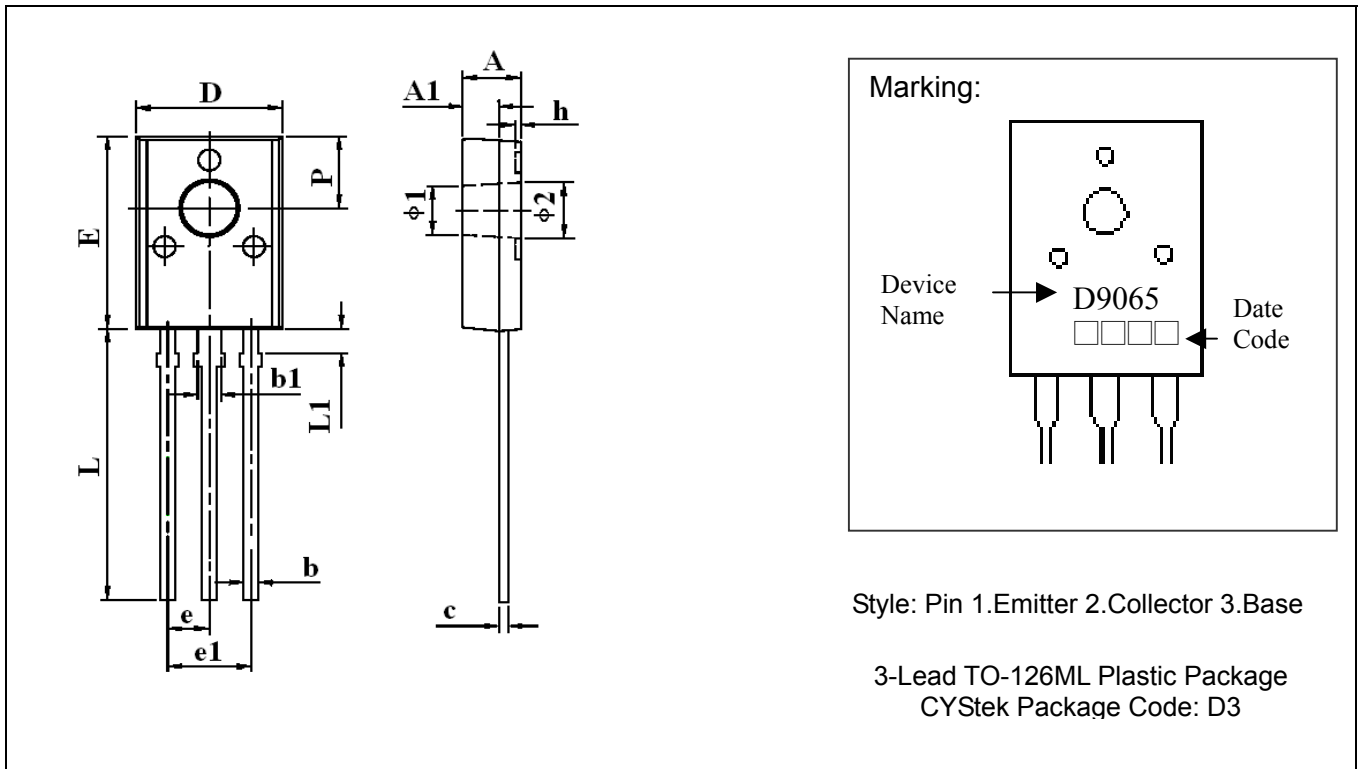
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-126ML Dimension



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.118	0.134	3.000	3.400	e	*0.090		*2.28	
A1	0.071	0.087	1.800	2.200	e1	0.176	0.183	4.460	4.660
b	0.026	0.034	0.660	0.860	L	0.594	0.610	15.100	15.500
b1	0.046	0.054	1.170	1.370	L1	0.051	0.059	1.300	1.500
c	0.018	0.024	0.450	0.600	P	0.159	0.167	4.040	4.240
D	0.307	0.323	7.800	8.200	Φ ₁	0.118	0.126	3.000	3.200
E	0.425	0.441	10.800	11.200	Φ ₂	0.122	0.130	3.100	3.300

*: Typical

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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