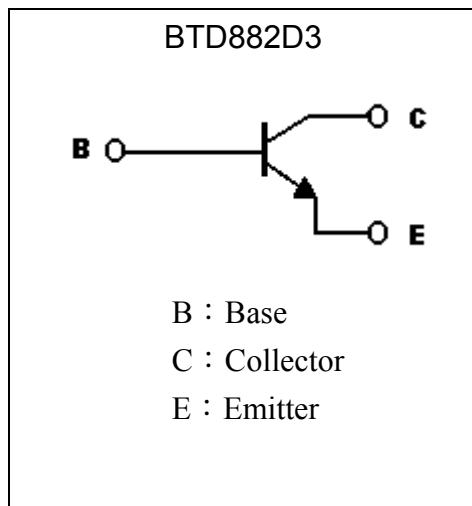
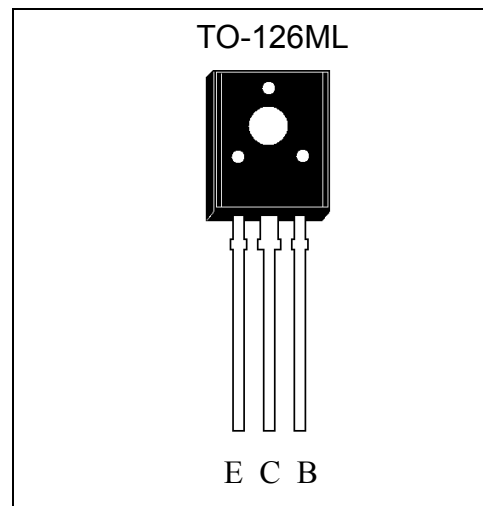


Low Vcesat NPN Epitaxial Planar Transistor

BTD882D3

Features

- Low $V_{CE(sat)}$, $V_{CE(sat)}=0.25$ V (typical), at $I_C / I_B = 2A / 200mA$
- Excellent current gain characteristics
- Complementary to BTB772D3
- Pb-free package

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current (DC)	I_C	3	A
Collector Current (Pulse)	I_{CP}	7 (Note)	
Power Dissipation ($T_A=25^\circ\text{C}$)	P_D	1	W
Power Dissipation ($T_C=25^\circ\text{C}$)		10	
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55~+150	$^\circ\text{C}$

Note : Pulse test, pulse width $\leq 380\mu\text{s}$, duty cycle $\leq 2\%$.



Characteristics (Ta=25°C)

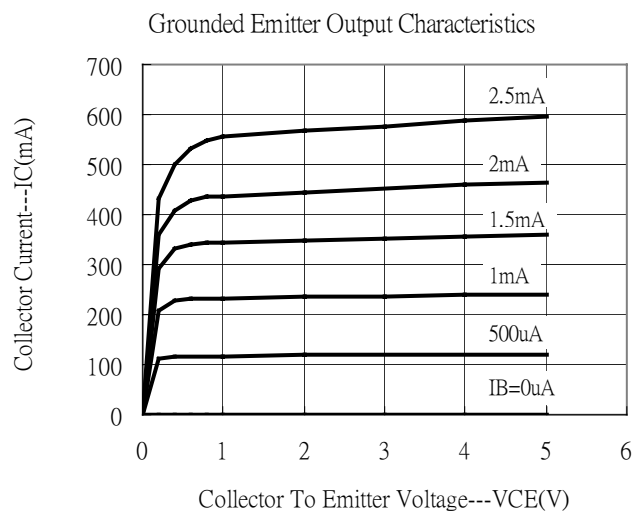
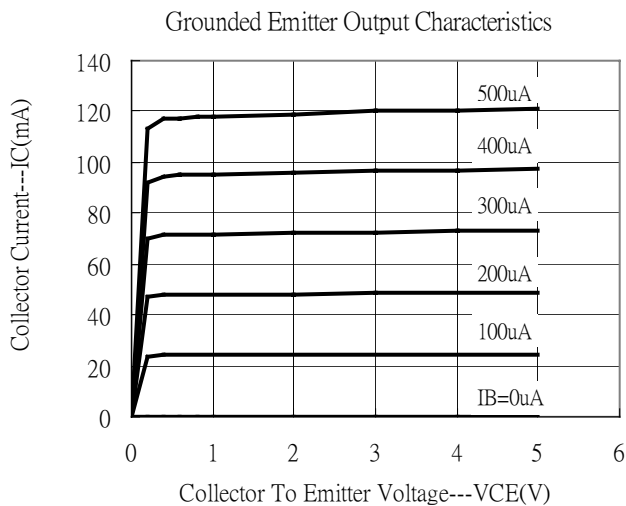
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	50	-	-	V	I _C =50μA, I _E =0
BV _{CE0}	50	-	-	V	I _C =1mA, I _B =0
BV _{EB0}	5	-	-	V	I _E =50μA, I _C =0
I _{CB0}	-	-	1	μA	V _{CB} =40V, I _E =0
I _{EB0}	-	-	1	μA	V _{EB} =5V, I _C =0
*V _{CE(sat)}	-	0.25	0.5	V	I _C =2A, I _B =200mA
*V _{BE(sat)}	-	-	2	V	I _C =2A, I _B =200mA
*h _{FE1}	150	-	-	-	V _{CE} =2V, I _C =20mA
*h _{FE2}	180	-	820	-	V _{CE} =2V, I _C =500mA
*h _{FE3}	100	-	-	-	V _{CE} =2V, I _C =1A
f _T	-	90	-	MHz	V _{CE} =5V, I _C =100mA, f=100MHz
Cob	-	45	-	pF	V _{CB} =10V, f=1MHz

*Pulse Test : Pulse Width ≤380μs, Duty Cycle ≤2%

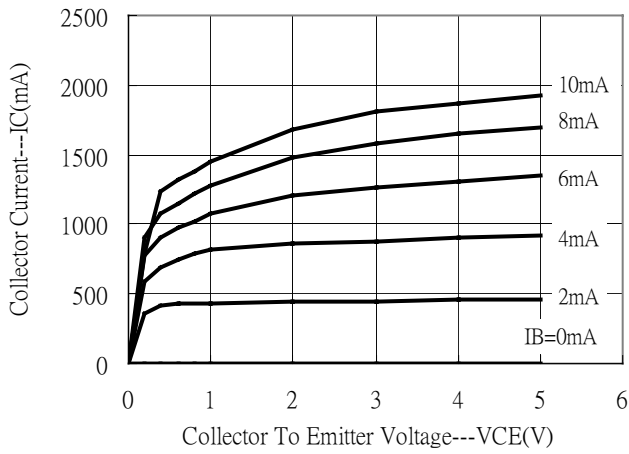
Classification Of hFE 2

Rank	R	S	T
Range	180~390	270~560	390~820

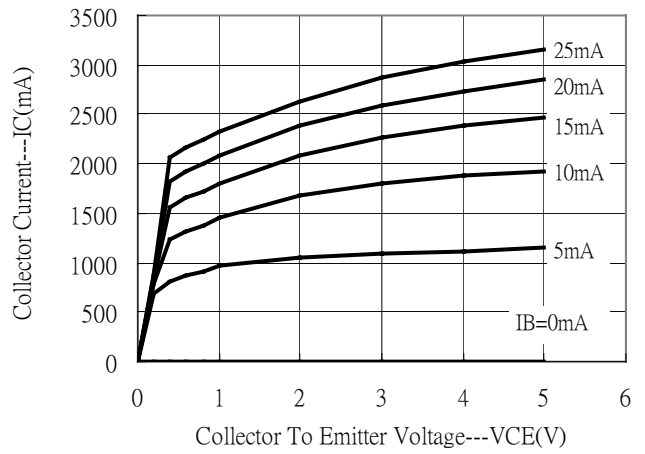
Characteristic Curves



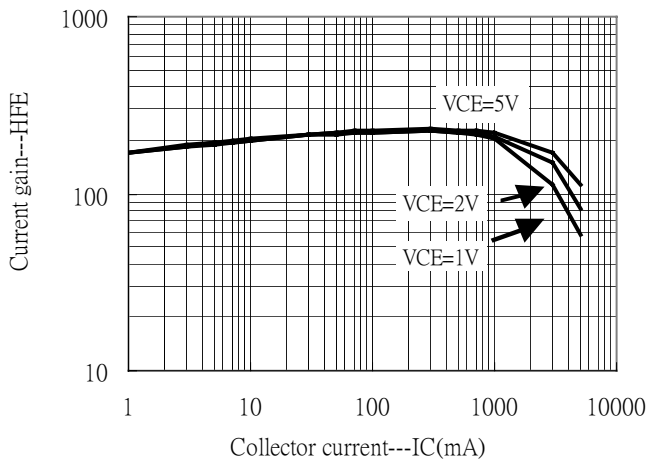
Grounded Emitter Output Characteristics



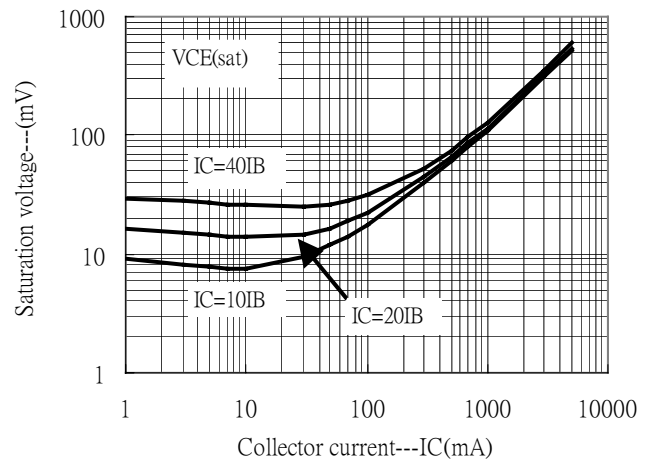
Grounded Emitter Output Characteristics



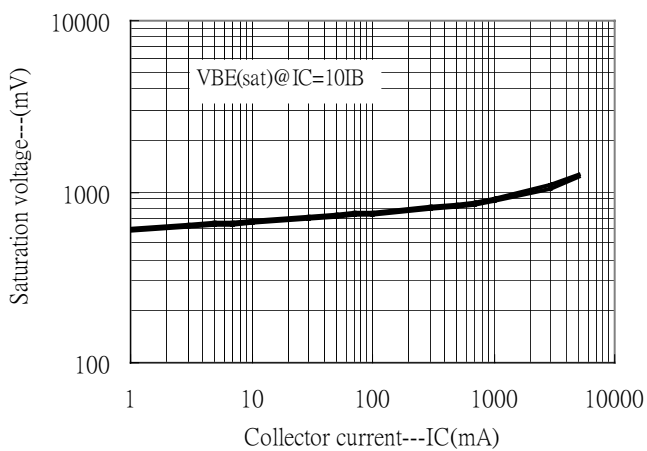
Current gain vs Collector current



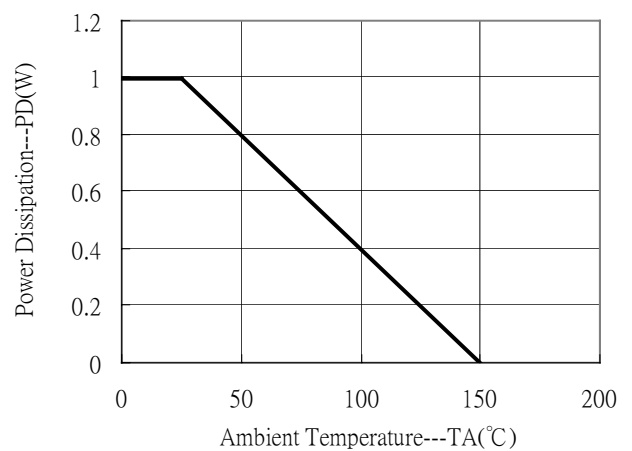
Saturation voltage vs Collector current



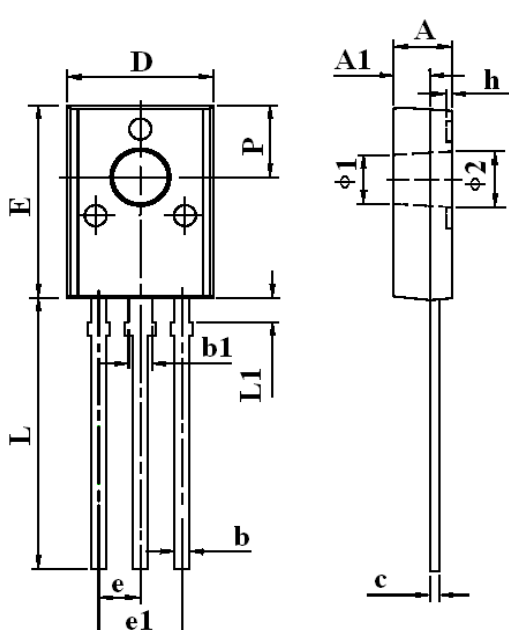
Saturation voltage vs Collector current



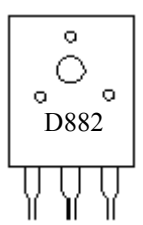
Power Derating Curve



TO-126ML Dimension



Marking:



Style: Pin 1. Emitter 2. Collector 3. Base

3-Lead TO-126ML Plastic Package
 CYStek Package Code: D3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.118	0.134	3.000	3.400	e	*0.090		*2.28	
A1	0.071	0.087	1.800	2.200	e1	0.176	0.183	4.460	4.660
b	0.026	0.034	0.660	0.860	L	0.594	0.610	15.100	15.500
b1	0.046	0.054	1.170	1.370	L1	0.051	0.059	1.300	1.500
c	0.018	0.024	0.450	0.600	P	0.159	0.167	4.040	4.240
D	0.307	0.323	7.800	8.200	Φ1	0.118	0.126	3.000	3.200
E	0.425	0.441	10.800	11.200	Φ2	0.122	0.130	3.100	3.300

- Notes:**
- Controlling dimension: millimeters.
 - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: 42 Alloy ; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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