

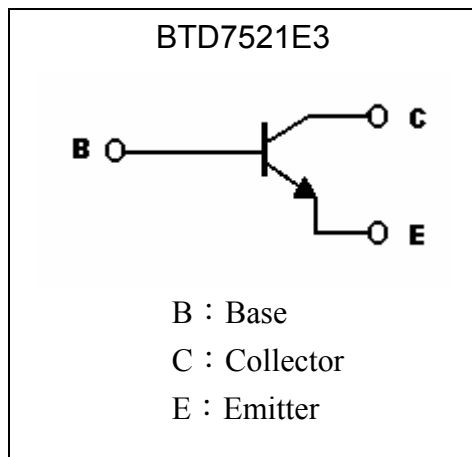
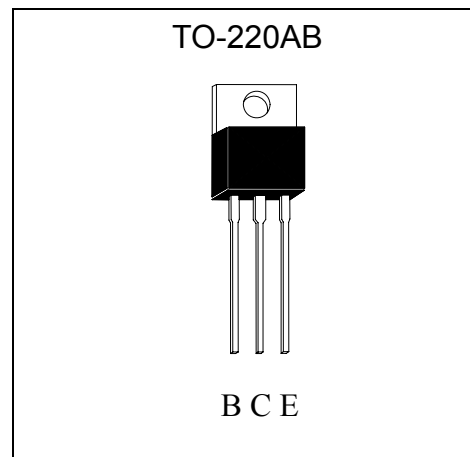
High Voltage NPN Epitaxial Planar Transistor

BTD7521E3

BV_{DSS}	90V
I_D	10A
$R_{CE(SAT)}$	50m Ω

Features

- High BV_{CEO}
- Very high current gain
- Pb-free lead plating package

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	90	V
Collector-Emitter Voltage	V_{CEO}	90	V
Emitter-Base Voltage	V_{EBO}	9	V
Collector Current (DC)	I_C	10	A
Collector Current (Pulse)	I_{CP}	20 (Note)	
Power Dissipation @ $T_A=25^\circ\text{C}$	P_D	2	W
Power Dissipation @ $T_c=25^\circ\text{C}$	P_D	80	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C/W}$
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55~+150	$^\circ\text{C}$

Note : Single Pulse , $P_w \leq 300\mu\text{s}$, $Duty \leq 2\%$.

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	90	-	-	V	I _C =1mA, I _E =0
BV _{CE0}	90	-	-	V	I _C =10mA, I _B =0
BV _{EB0}	9	-	-	V	I _C =100μA, I _C =0
I _{CB0}	-	-	10	μA	V _{CB} =90V, I _E =0
I _{EB0}	-	-	100	nA	V _{EB} =7V, I _C =0
*V _{CE(sat)}	-	120	250	mV	I _C =5A, I _B =50mA
*R _{CE(sat)}	-	24	50	mΩ	I _C =5A, I _B =50mA
*V _{CE(sat)}	-	170	300	mV	I _C =5A, I _B =30mA
*V _{CE(sat)}	-	320	500	mV	I _C =5A, I _B =20mA
*V _{BE(sat)}	-	0.74	0.9	V	I _C =6A, I _B =10mA
*h _{FE}	1000	-	-	-	V _{CE} =5V, I _C =1A
*h _{FE}	600	-	-	-	V _{CE} =5V, I _C =5A
*h _{FE}	300	-	-	-	V _{CE} =5V, I _C =10A
Cob	-	130	-	pF	V _{CB} =10V, f=1MHz

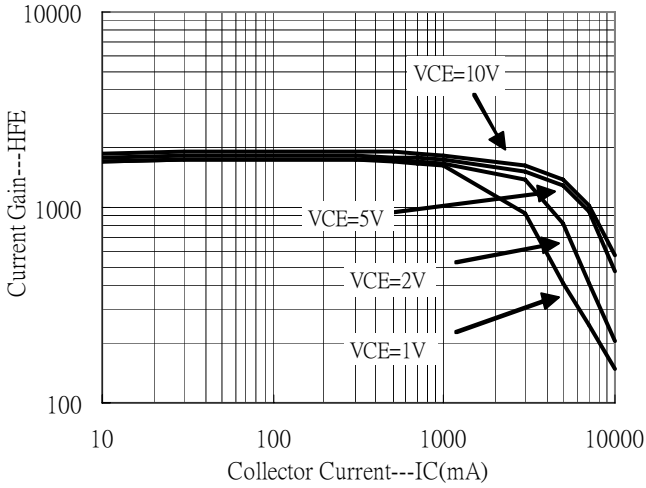
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

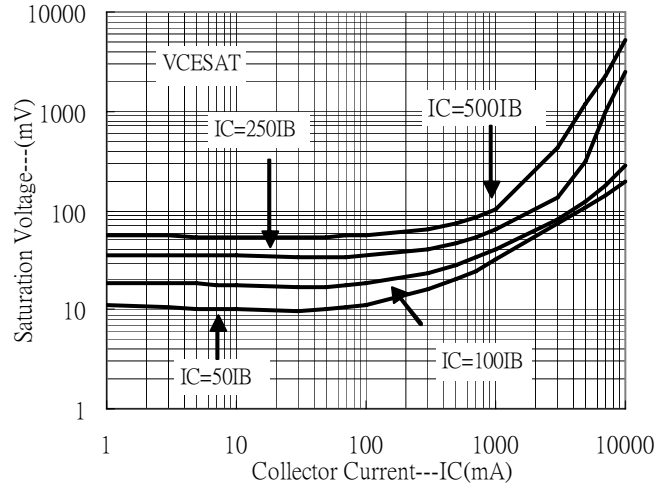
Device	Package	Shipping
BTD7521E3	TO-220 (RoHS compliant package)	50 pcs / tube , 40 tubes/box

Typical Characteristics

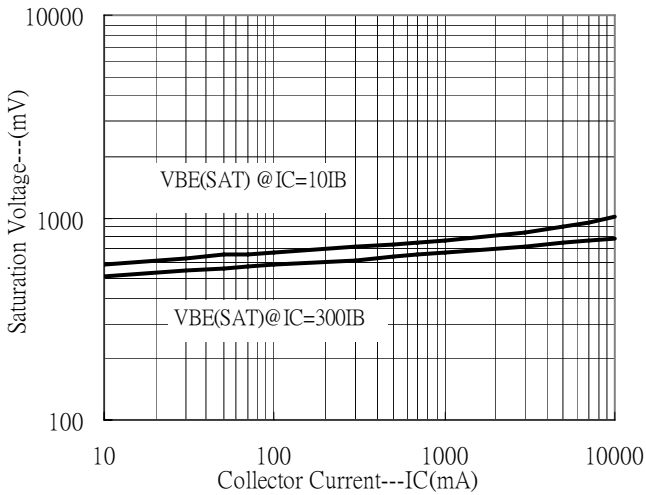
Current Gain vs Collector Current



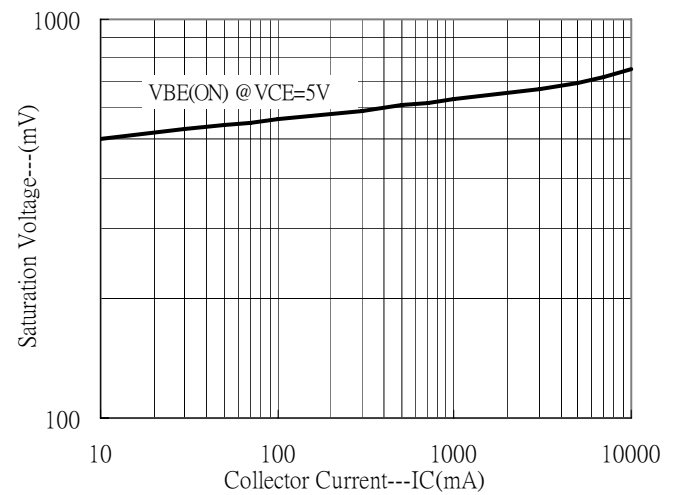
Saturation Voltage vs Collector Current



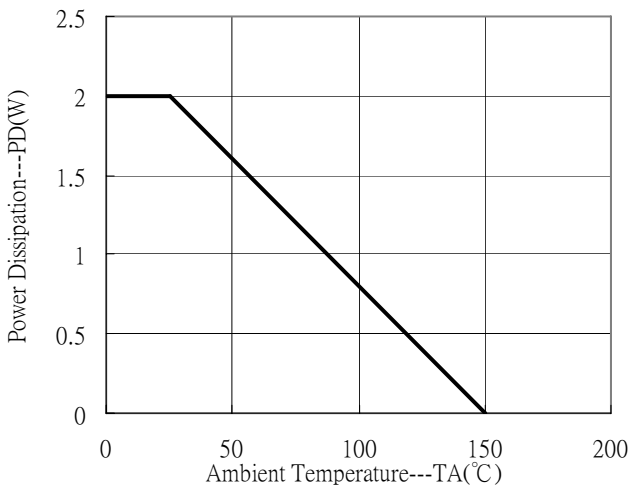
Saturation Voltage vs Collector Current



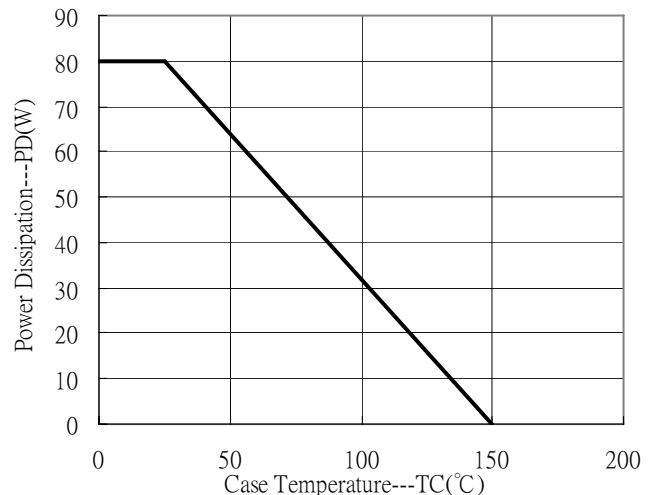
Saturation Voltage vs Collector Current



Power Derating Curve

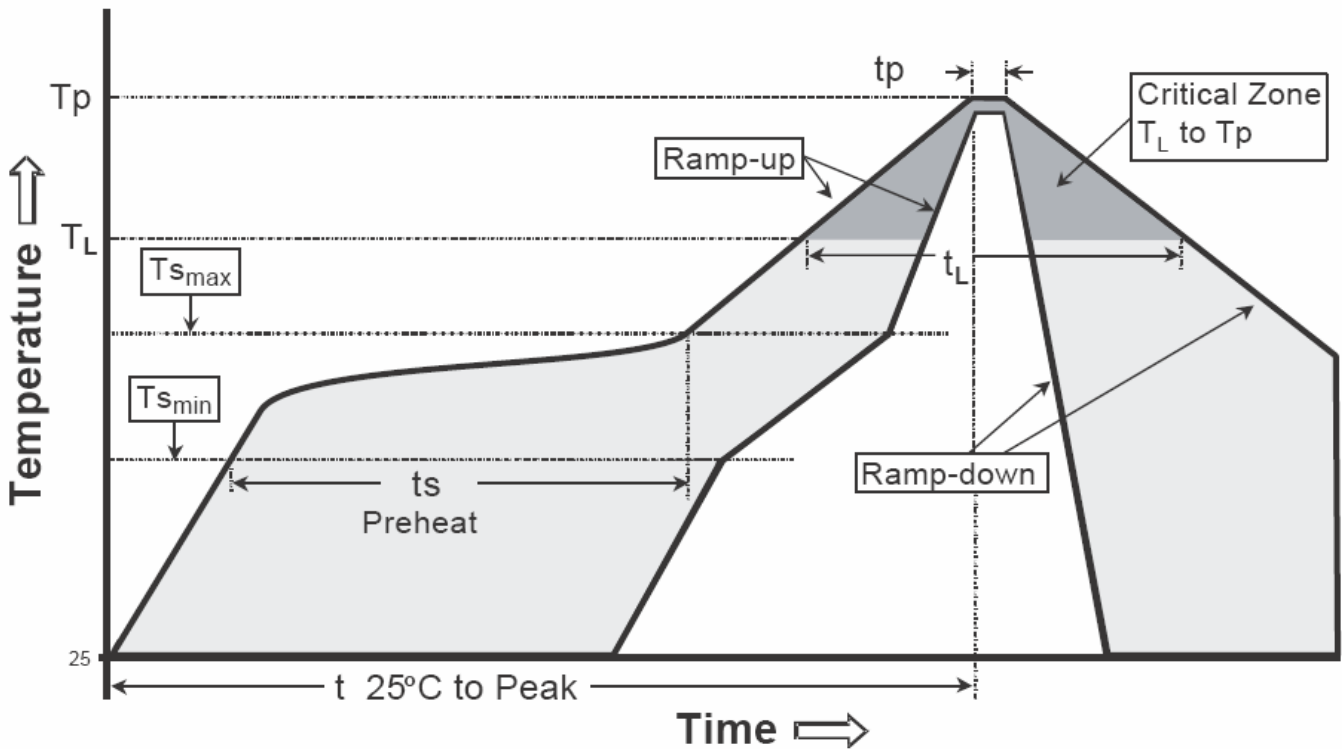


Power Derating Curve



Recommended wave soldering condition

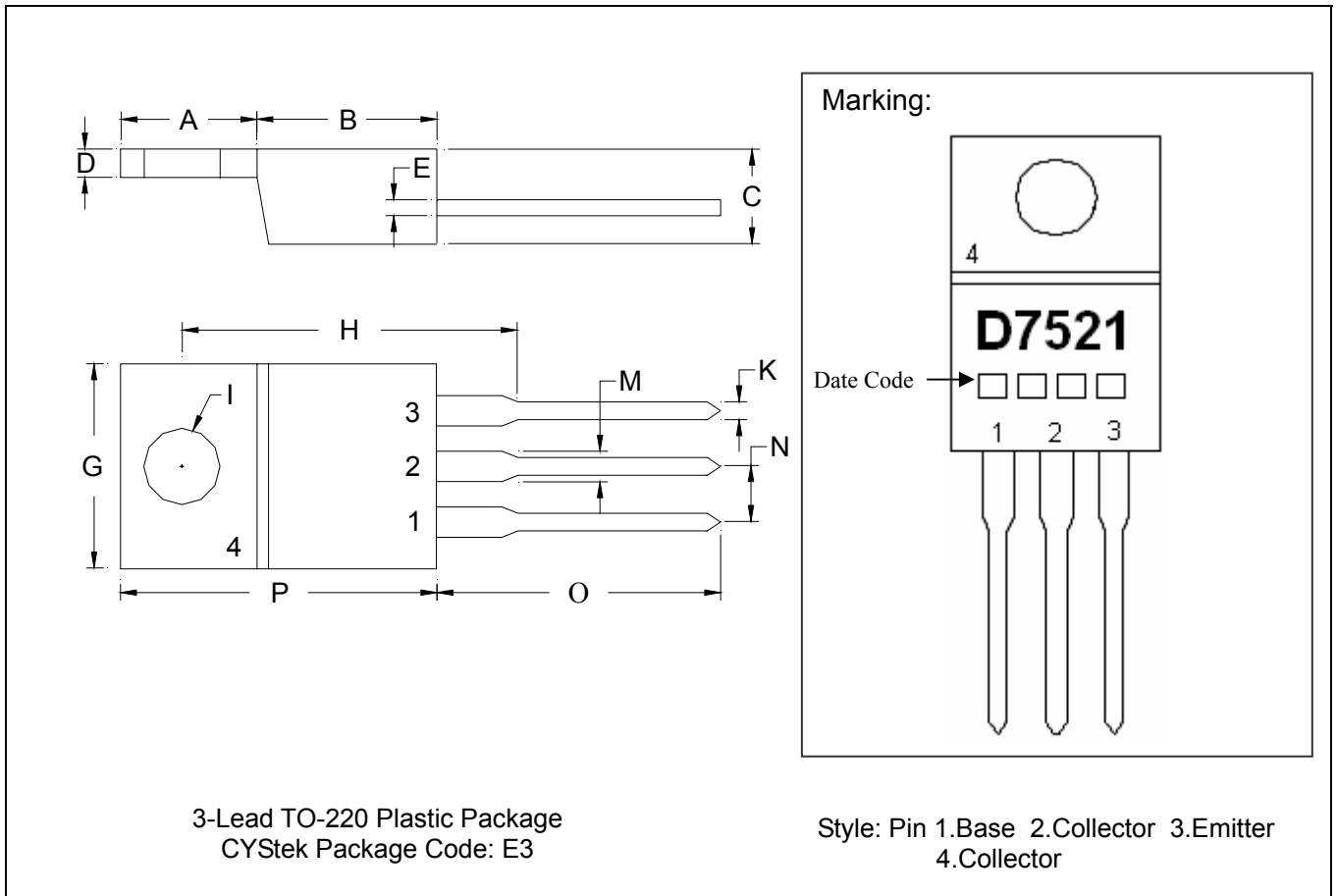
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.2197	0.2949	5.58	7.49	I	-	*0.1508	-	*3.83
B	0.3299	0.3504	8.38	8.90	K	0.0295	0.0374	0.75	0.95
C	0.1732	0.185	4.40	4.70	M	0.0449	0.0551	1.14	1.40
D	0.0453	0.0547	1.15	1.39	N	-	*0.1000	-	*2.54
E	0.0138	0.0236	0.35	0.60	O	0.5000	0.5618	12.70	14.27
G	0.3803	0.4047	9.66	10.28	P	0.5701	0.6248	14.48	15.87
H	-	*0.6398	-	*16.25					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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