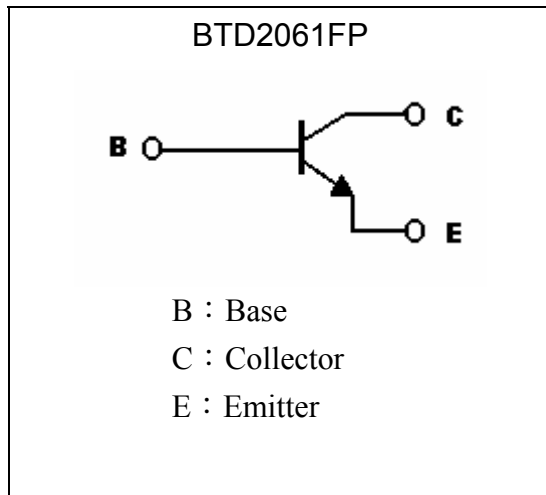
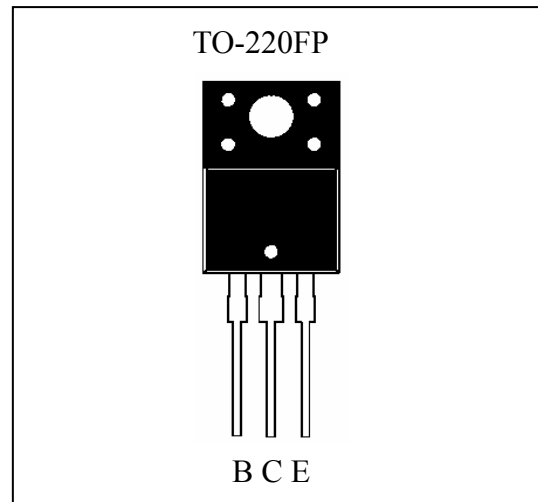


Low Vcesat NPN Epitaxial Planar Transistor

BTD2061FP

Features

- Low saturation voltage, typically $V_{CE(sat)}=0.25V$ at $I_C/I_B=2A/0.2A$.
- Excellent DC current gain characteristics.
- Wide SOA(safe operating area).
- Pb-free package.

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^\circ C$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	200	V
Collector-Emitter Voltage	V_{CEO}	80	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current (DC)	I_C	4	A
Collector Current (Pulse)	I_{CP}	7 (Note 1)	
Power Dissipation @ $T_A=25^\circ C$	P_D	2	W
Power Dissipation @ $T_C=25^\circ C$	P_D	30	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	$^\circ C/W$
Junction Temperature	T_j	150	$^\circ C$
Storage Temperature	T_{stg}	-55~+150	$^\circ C$

 Note : 1. Single Pulse , $P_w \leq 380\mu s, Duty \leq 2\%$.

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CB0}	200	-	-	V	$I_C=50\mu A, I_E=0$
BV_{CE0}	80	-	-	V	$I_C=10mA, I_B=0$
BV_{EB0}	5	-	-	V	$I_E=50\mu A, I_B=0$
I_{C0}	-	-	1	μA	$V_{CB}=180V, I_B=0$
I_{E0}	-	-	100	nA	$V_{EB}=5V, I_C=0$
* $V_{CE(sat)}$	-	0.3	0.5	V	$I_C=2A, I_B=0.2A$
* $V_{CE(sat)}$	-	0.36	0.6	V	$I_C=3A, I_B=0.3A$
* $V_{BE(sat)}$	-	-	1.5	V	$I_C=2A, I_B=0.2A$
* h_{FE}	100	-	320	-	$V_{CE}=5V, I_C=500mA$
* h_{FE}	50	-	-	-	$V_{CE}=5V, I_C=3A$
f_T	-	8	-	MHz	$V_{CE}=5V, I_C=500mA, f=5MHz$
Cob	-	70	-	pF	$V_{CB}=10V, f=1MHz$

*Pulse Test : Pulse Width $\leq 380\mu s$, Duty Cycle $\leq 2\%$ **Classification Of h_{FE}**

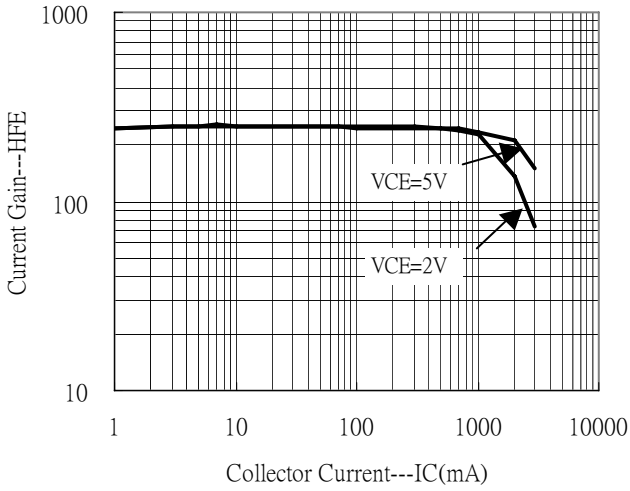
Rank	C	D
Range	100~200	160~320

Ordering Information

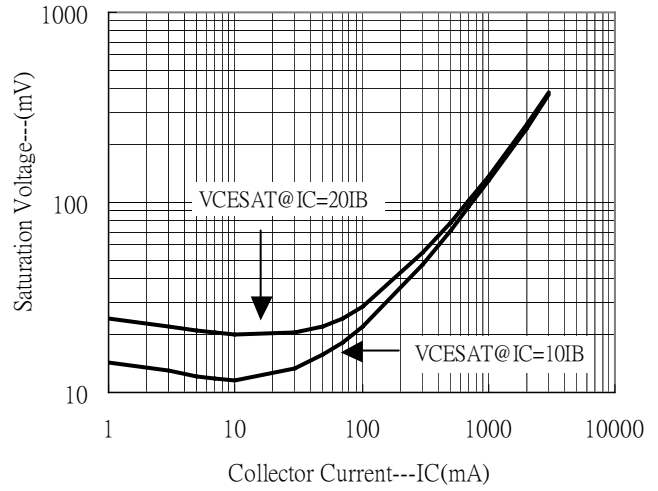
Device	Package	Shipping
BTD2061FP	TO-220FP (Pb-free lead plating package)	50 pcs / tube, 40 tubes / boxes

Characteristic Curves

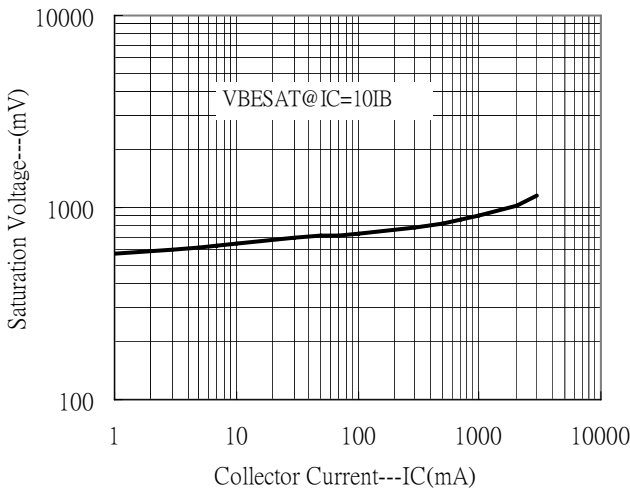
Current Gain vs Collector Current



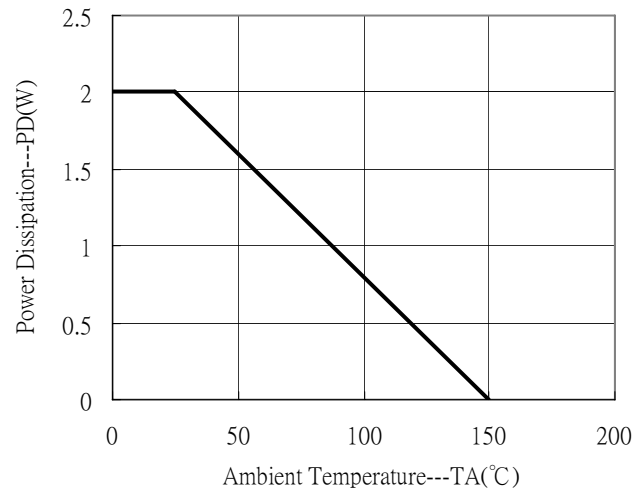
Saturation Voltage vs Collector Current



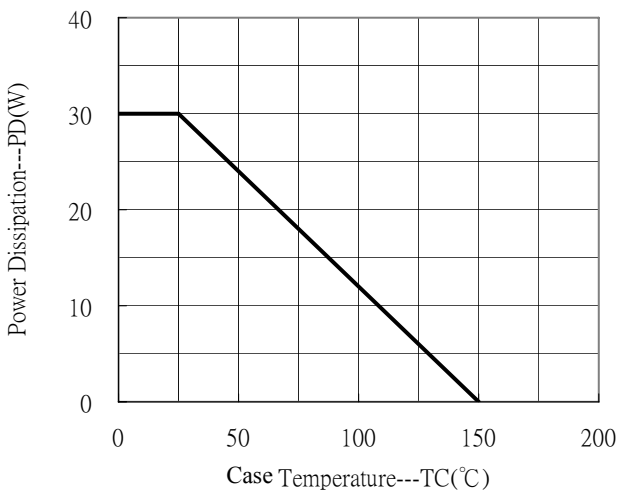
Saturation Voltage vs Collector Current



Power Derating Curve

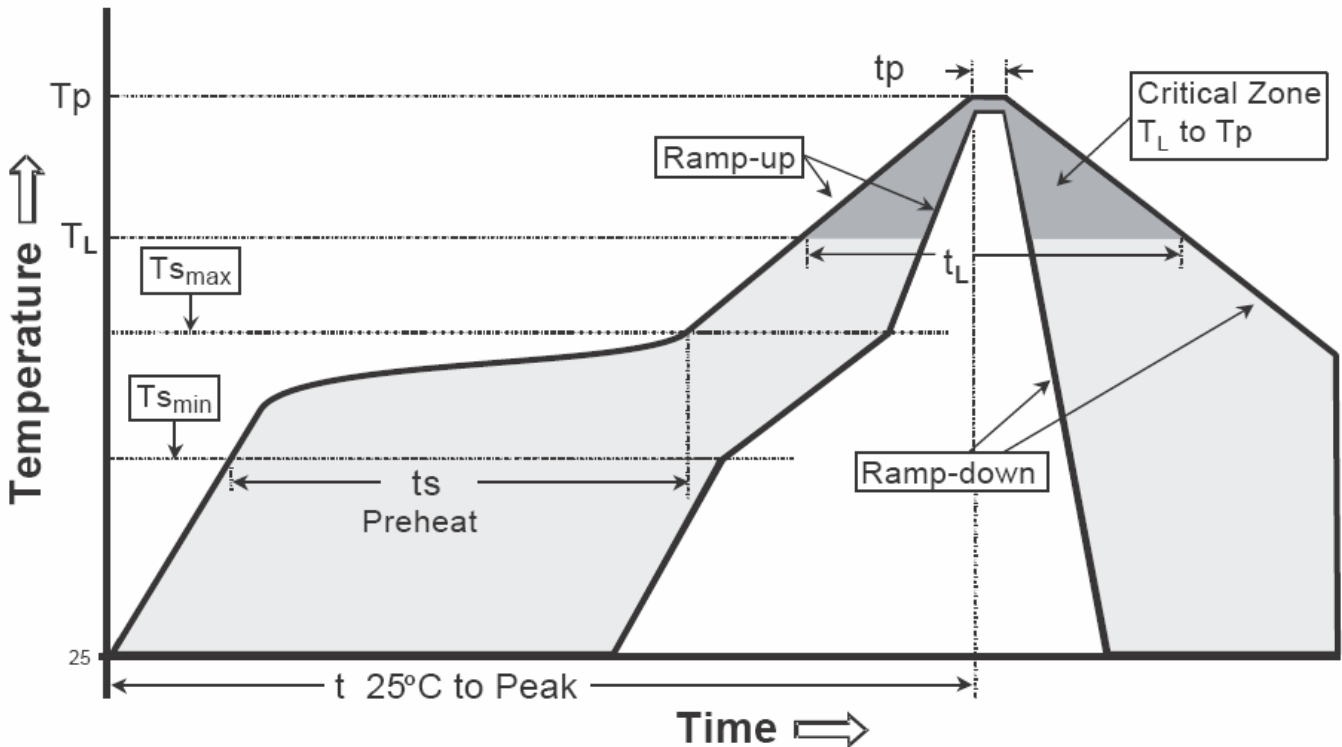


Power Derating Curve



Recommended wave soldering condition

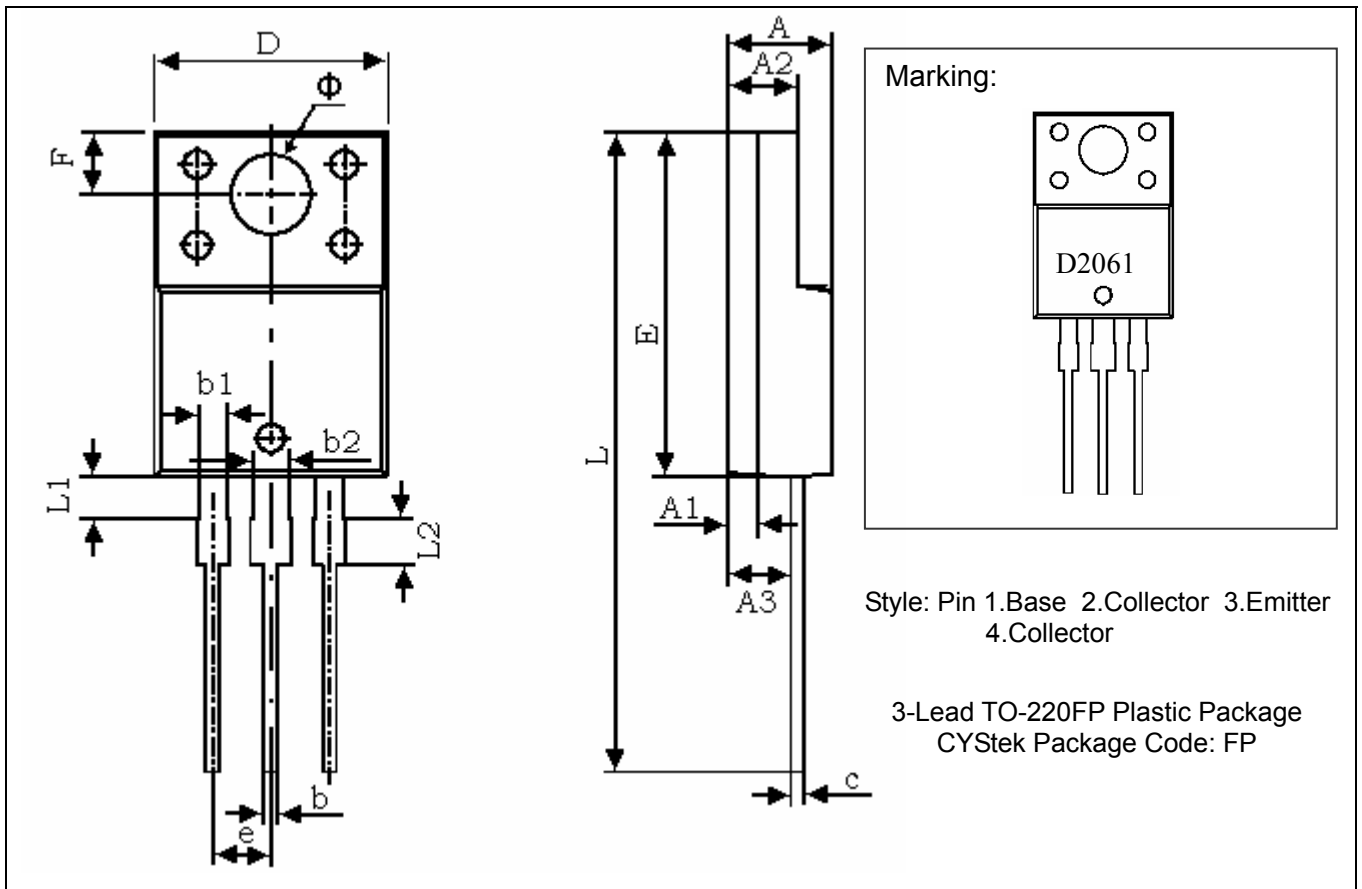
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220FP Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.169	0.185	4.300	4.700	D	0.392	0.408	9.960	10.360
A1	0.051 REF		1.300 REF		E	0.583	0.598	14.800	15.200
A2	0.110	0.126	2.800	3.200	e	0.100 TYP		2.540 TYP	
A3	0.098	0.114	2.500	2.900	F	0.106 REF		2.700 REF	
b	0.020	0.030	0.500	0.750	Φ	0.138 REF		3.500 REF	
b1	0.043	0.053	1.100	1.350	L	1.102	1.118	28.000	28.400
b2	0.059	0.069	1.500	1.750	L1	0.067	0.075	1.700	1.900
c	0.020	0.030	0.500	0.750	L2	0.075	0.083	1.900	2.100

- Notes:** 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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