

# Low Vcesat NPN Epitaxial Planar Transistor

## BTD1816I3

$BV_{CEO}$	100V
$I_C$	4A
$R_{CESAT}$	50mΩ

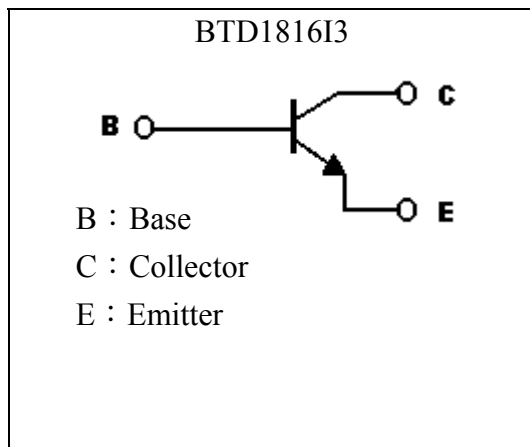
### Features

- Low collector-to-emitter saturation voltage
- High-speed switching
- Large current capability
- Good linearity of  $h_{FE}$
- High  $f_T$
- RoHS compliant package

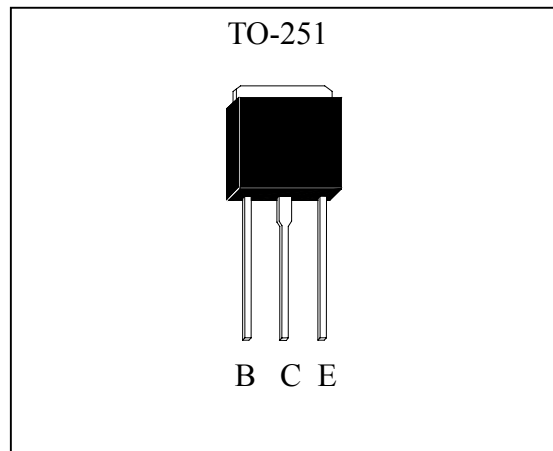
### Applications

- Suitable for relay drivers, high speed inverters, converters, and other high current switching applications.

### Symbol

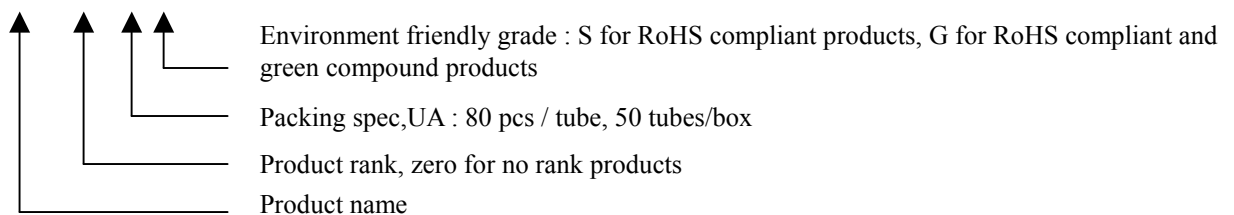


### Outline



### Ordering Information

Device	Package	Shipping
BTD1816I3-0-UA-G	TO-251 (Pb-free lead plating and halogen-free package)	80 pcs/tube, 50 tubes/box





**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V <sub>CBO</sub>	120	V
Collector-Emitter Voltage	V <sub>CEO</sub>	100	V
Emitter-Base Voltage	V <sub>EBO</sub>	6	V
Collector Current (DC)	I <sub>C</sub>	4	A
Collector Current (Pulse)	I <sub>CP</sub>	8 (Note 1)	
Base Current	I <sub>B</sub>	1.2	A
Power Dissipation @ T <sub>A</sub> =25°C	P <sub>D</sub>	1	W
Power Dissipation @ T <sub>C</sub> =25°C	P <sub>D</sub>	20	
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	125	°C/W
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	6.25	°C/W
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

Note : 1. Single Pulse , Pw≤380μs, Duty≤2%.

**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CBO</sub>	120	-	-	V	I <sub>C</sub> =10μA, I <sub>E</sub> =0
*BV <sub>CEO</sub>	100	-	-	V	I <sub>C</sub> =1mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	6	-	-	V	I <sub>C</sub> =10μA, I <sub>C</sub> =0
I <sub>CBO</sub>	-	-	1	μA	V <sub>CB</sub> =100V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	1	μA	V <sub>EB</sub> =4V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub> 1	-	50	120	mV	I <sub>C</sub> =1A, I <sub>B</sub> =50mA
*V <sub>CE(sat)</sub> 2	-	90	250	mV	I <sub>C</sub> =2A, I <sub>B</sub> =200mA
*V <sub>BE(sat)</sub>	-	0.9	1.2	V	I <sub>C</sub> =2A, I <sub>B</sub> =200mA
*h <sub>FE</sub> 1	180	-	560	-	V <sub>CE</sub> =5V, I <sub>C</sub> =500mA
*h <sub>FE</sub> 2	120	-	-	-	V <sub>CE</sub> =5V, I <sub>C</sub> =3A
f <sub>T</sub>	-	180	-	MHz	V <sub>CE</sub> =10V, I <sub>C</sub> =500mA
C <sub>ob</sub>	-	40	-	pF	V <sub>CB</sub> =10V, f=1MHz
t <sub>on</sub>	-	100	-	ns	V <sub>CC</sub> =50V, I <sub>C</sub> =10I <sub>B</sub> 1=-10I <sub>B</sub> 2=2A, R <sub>L</sub> =25Ω
t <sub>stg</sub>	-	900	-	ns	
t <sub>f</sub>	-	50	-	ns	

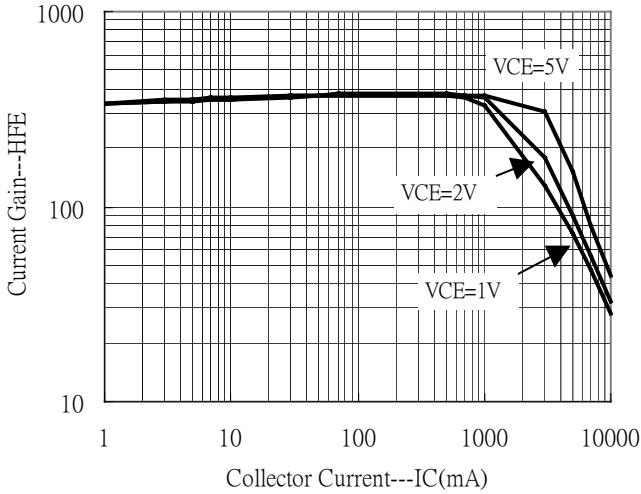
\*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

**Classification of hFE 1**

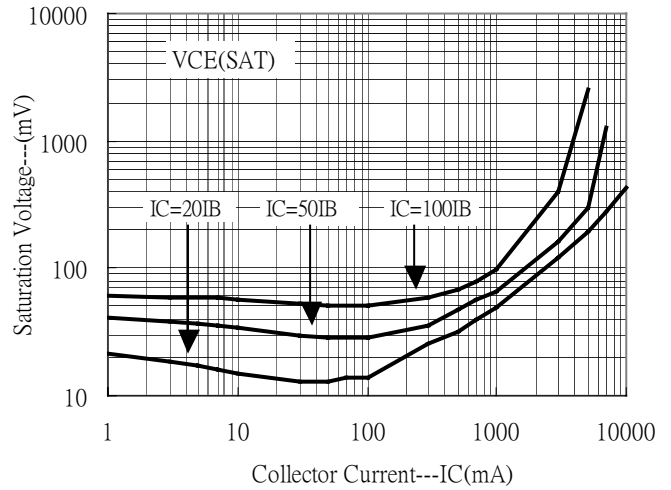
Rank	R	S
Range	180~390	270~560

**Characteristic Curves**

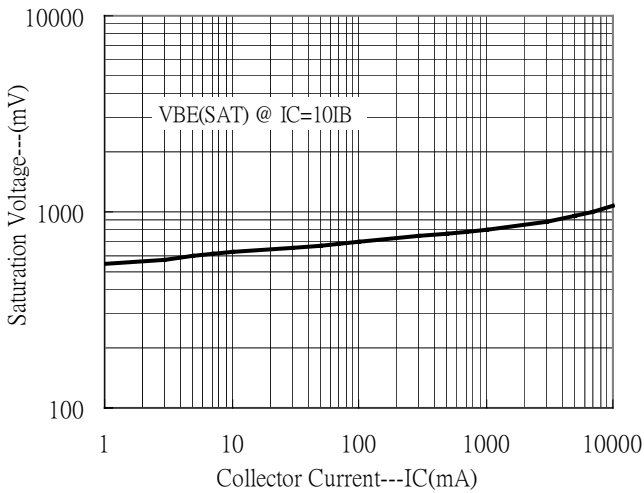
Current Gain vs Collector Current



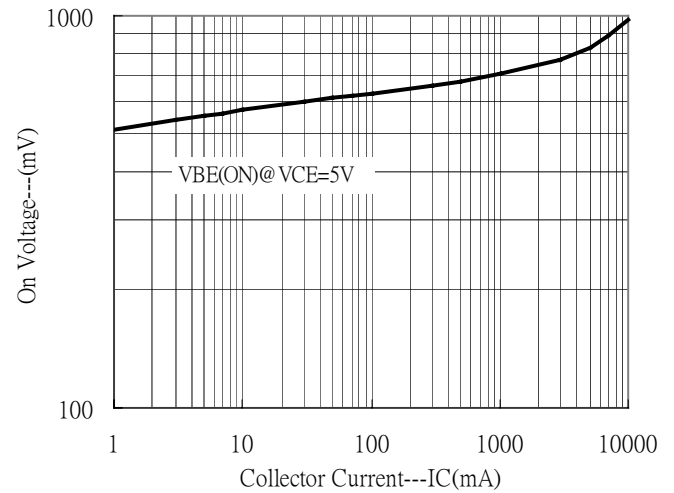
Saturation Voltage vs Collector Current



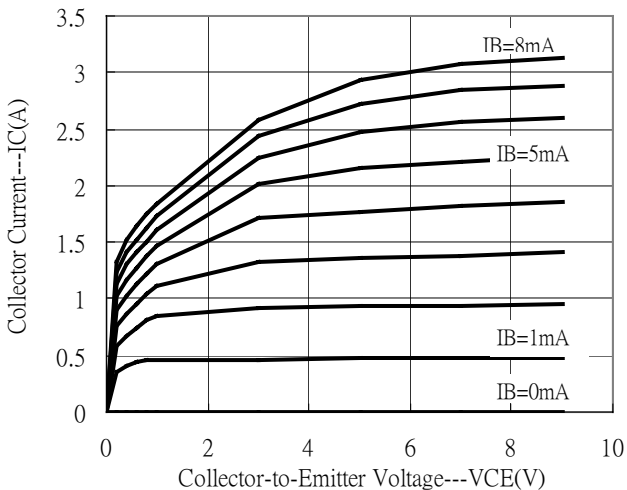
Saturation Voltage vs Collector Current



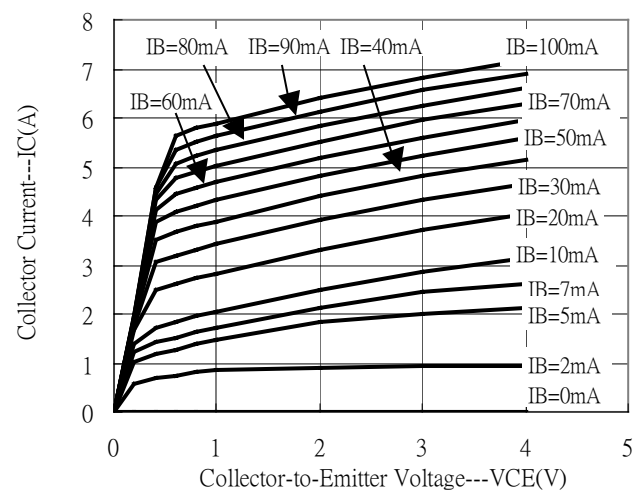
On Voltage vs Collector Current



Grounded Emitter Output Characteristics



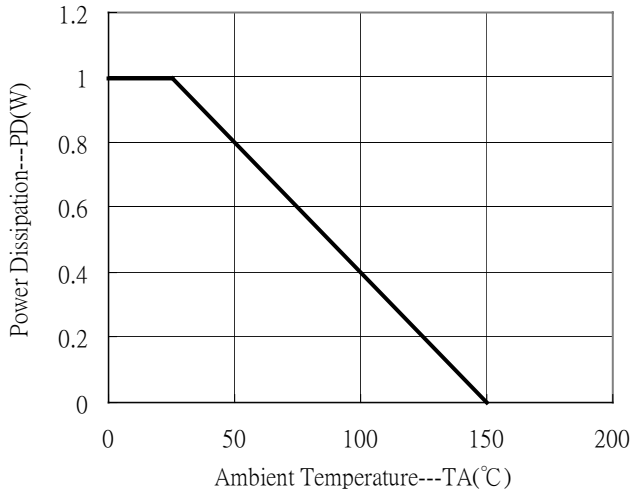
Grounded Emitter Output Characteristics



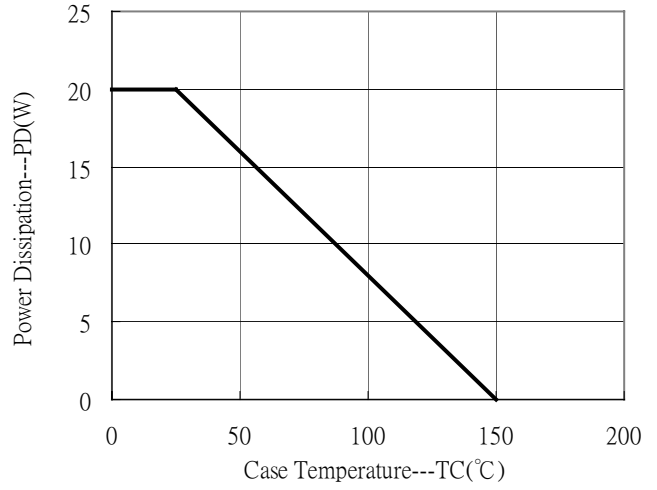


### Characteristic Curves(Cont.)

Power Derating Curve



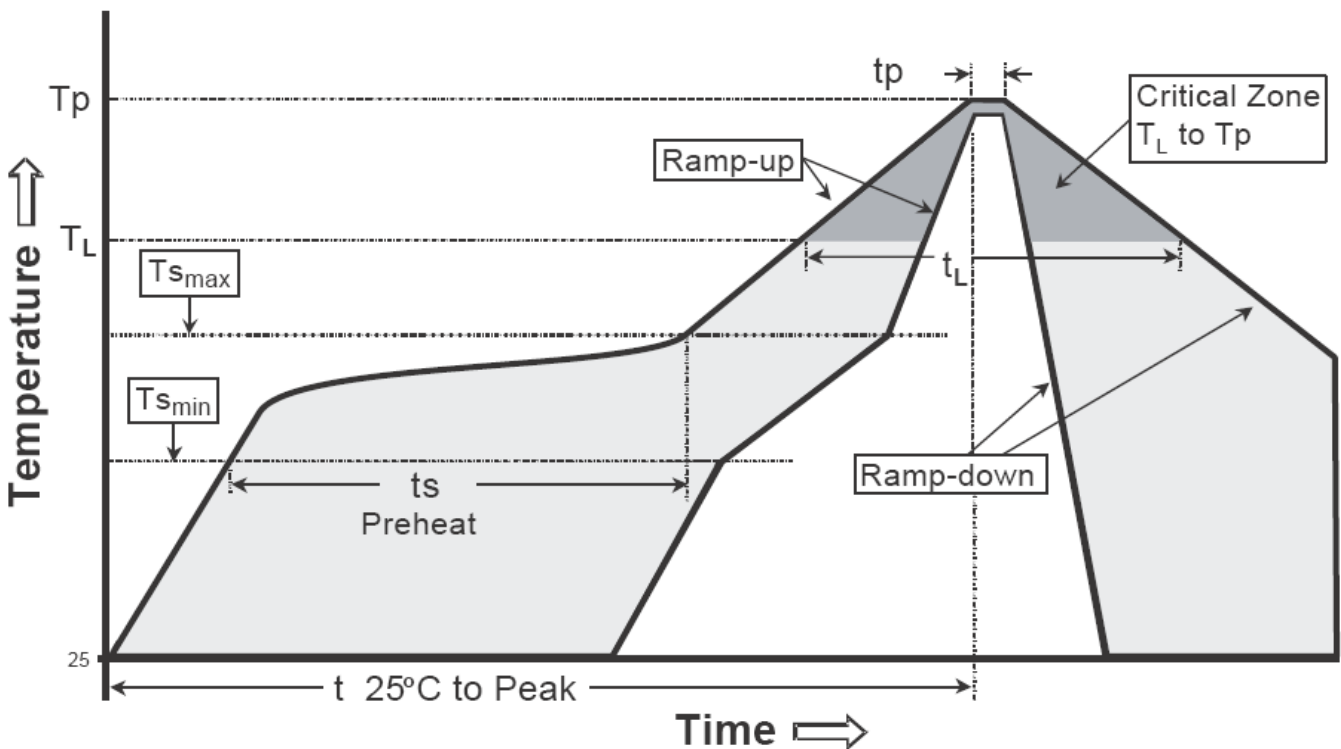
Power Derating Curve



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

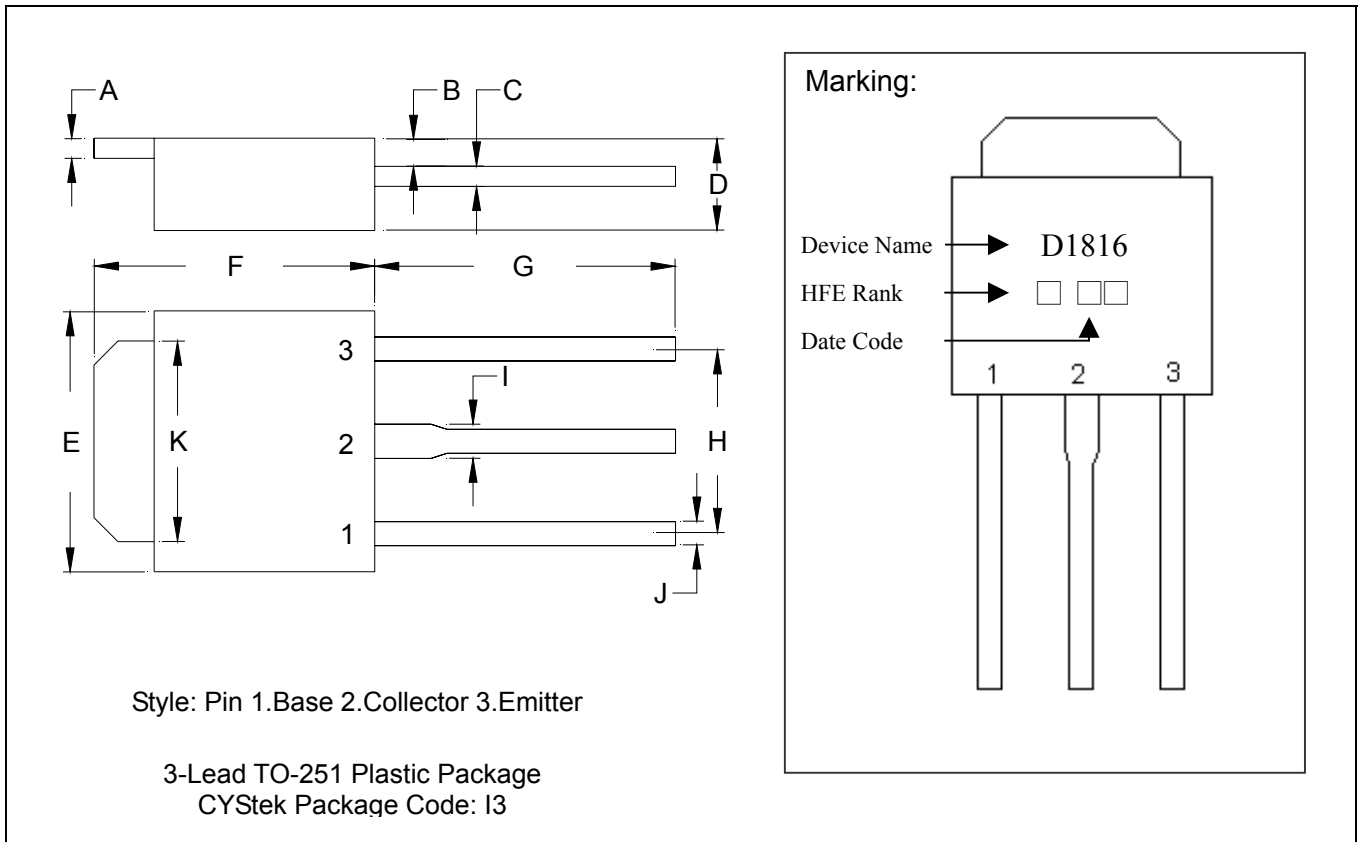
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-251 Dimension**



\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.0177	0.0217	0.45	0.55	G	0.2559	-	6.50	-
B	0.0354	0.0591	0.90	1.50	H	-	*0.1811	-	*4.60
C	0.0177	0.0236	0.45	0.60	I	-	0.0449	-	1.14
D	0.0866	0.0945	2.20	2.40	J	-	0.0346	-	0.88
E	0.2441	0.2677	6.20	6.80	K	0.2047	0.2165	5.20	5.50
F	0.2677	0.2835	6.80	7.20					

- Notes: 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.