Low Vcesat NPN Epitaxial Planar Transistor

BTD1760J3

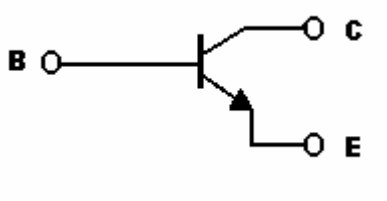
BV_{CEO}	50V
I_C	3A
R_{CESAT}	125mΩ typ.

Features

- Low V_{CE}(sat), V_{CE}(sat)=0.25 V (typical), at I_C / I_B = 2A / 0.2A
- Excellent current gain characteristics
- Complementary to BTB1184J3
- Pb-free package

Symbol

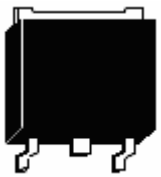
BTD1760J3



B：Base
C：Collector
E：Emitter

Outline

TO-252(DPAK)



B C E

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current(DC)	I_C	3	A
Collector Current(Pulse)	I_{CP}	7 *1	
Power Dissipation(T_A=25℃)	Pd(T_A=25℃)	1	W
Power Dissipation(T_C=25℃)	Pd(T_C=25℃)	15 *2	
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55~+150	°C

Note : *1. Single Pulse Pw=10ms
*2 Printed circuit board, 1.7mm thick, collector copper plating 10mm*10mm or larger

Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	50	-	-	V	I_C=50μA, I_E=0
BV_{CEO}	50	-	-	V	I_C=1mA, I_B=0
BV_{EBO}	5	-	-	V	I_E=50μA, I_C=0
I_{CBO}	-	-	1	μA	V_{CB}=30V, I_E=0
I_{EBO}	-	-	1	μA	V_{EB}=4V, I_C=0
*$V_{CE(sat)}$	-	0.25	0.5	V	I_C=2A, I_B=0.2A
*$V_{BE(sat)}$	-	-	2	V	I_C=2A, I_B=0.2A
*$h_{FE}1$	150	-	-	-	V_{CE}=2V, I_C=20mA
*$h_{FE}2$	180	-	560	-	V_{CE}=2V, I_C=0.1A
*$h_{FE}3$	82	-	-	-	V_{CE}=2V, I_C=1A
f_T	-	90	-	MHz	V_{CE}=5V, I_C=0.5A, f=100MHz
Cob	-	13	-	pF	V_{CB}=10V, f=1MHz

*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

Classification Of $h_{FE}2$

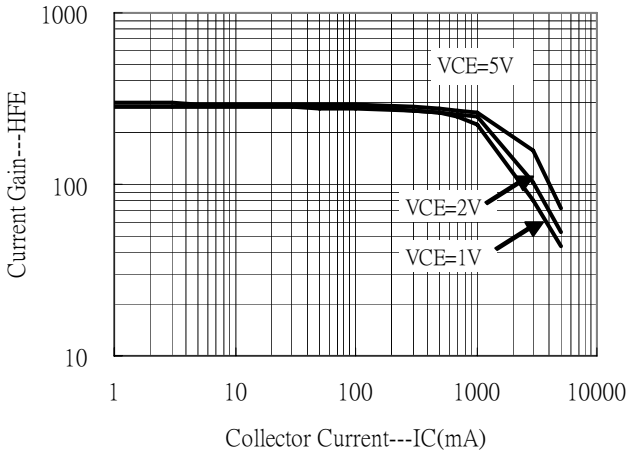
Rank	R	S
Range	180~390	270~560

Ordering Information

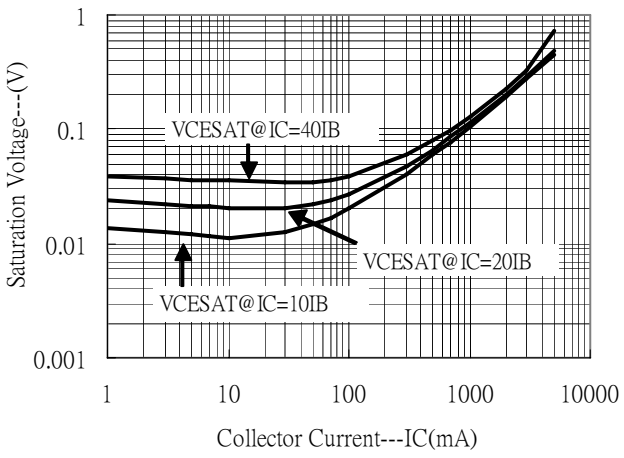
Device	H_{FE} rank	Package	Shipping
BTD1760J3-R-T3-G	R	TO-252 (Pb-free lead plating and halogen-free package)	2500 pcs / Tape & Reel
BTD1760J3-S-T3-G	S		

Typical Characteristics

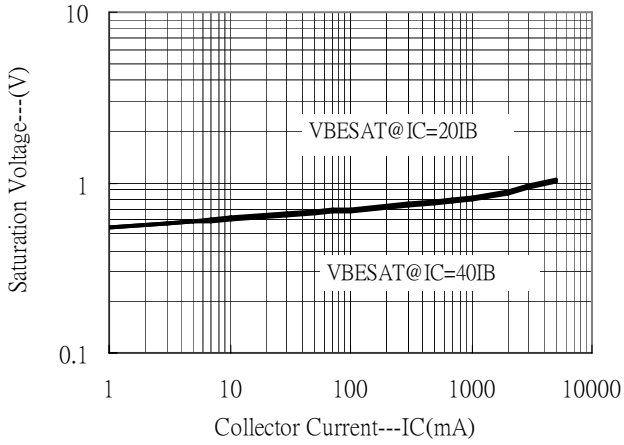
Current Gain vs Collector Current



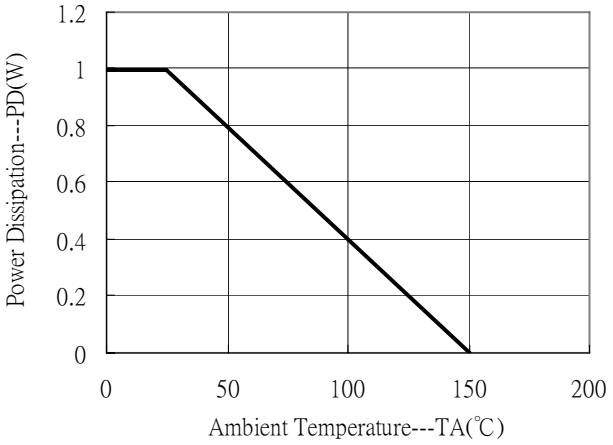
Saturation Voltage vs Collector Current



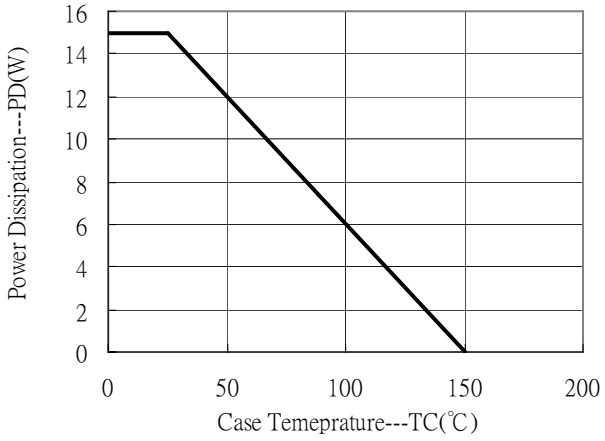
Saturation Voltage vs Collector Current



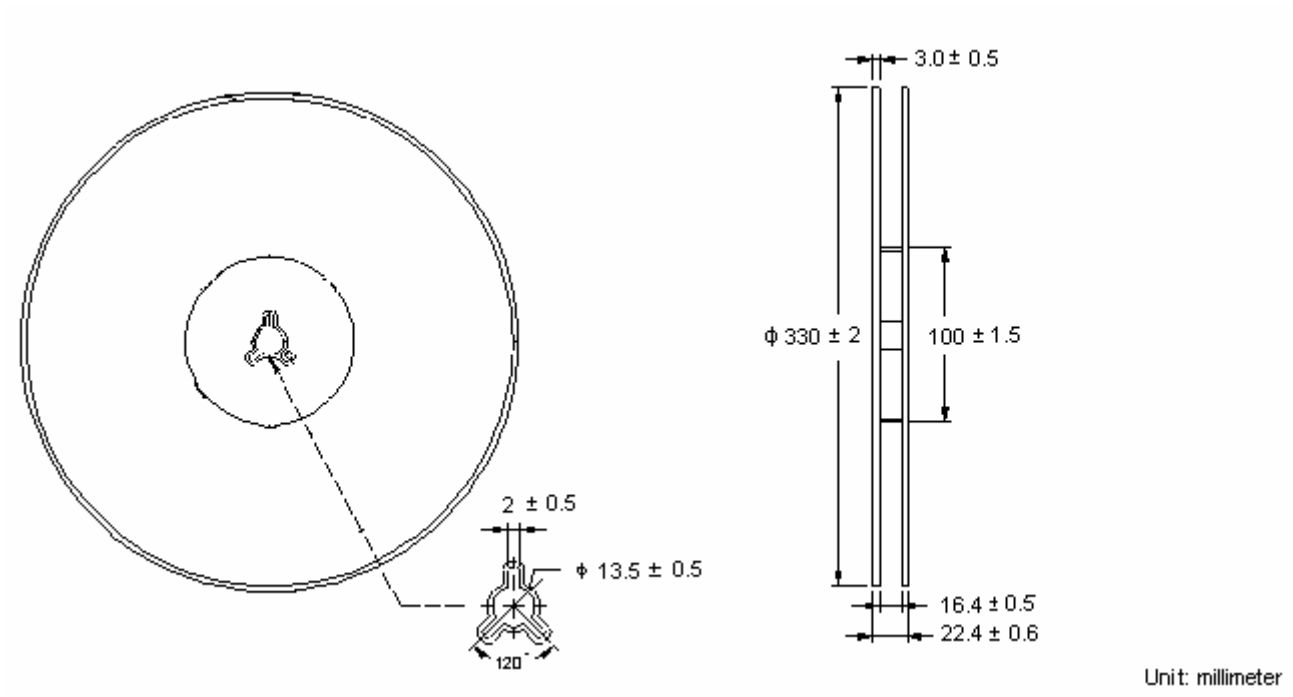
Power Derating Curve



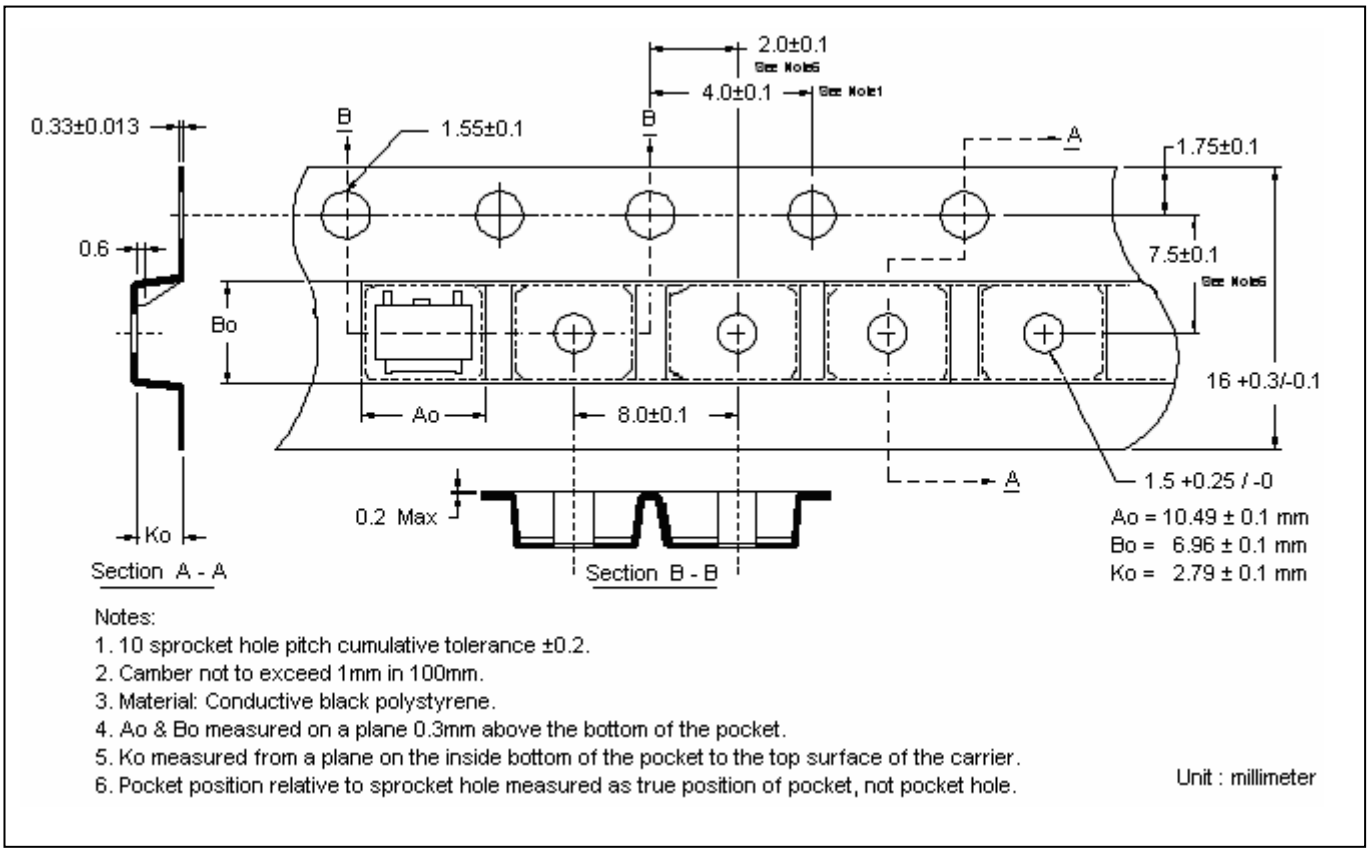
Power Derating Curve



Reel Dimension



Carrier Tape Dimension



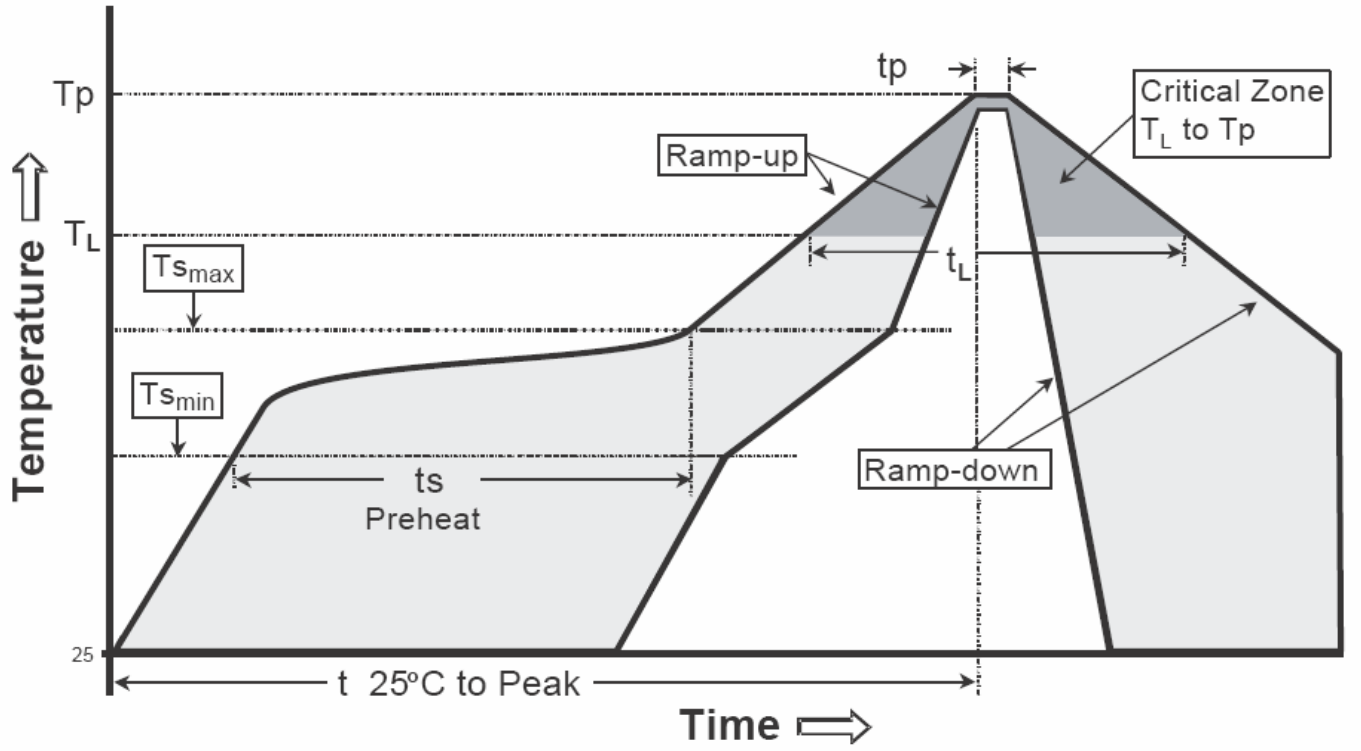
Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material: Conductive black polystyrene.
4. Ao & Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Unit : millimeter

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

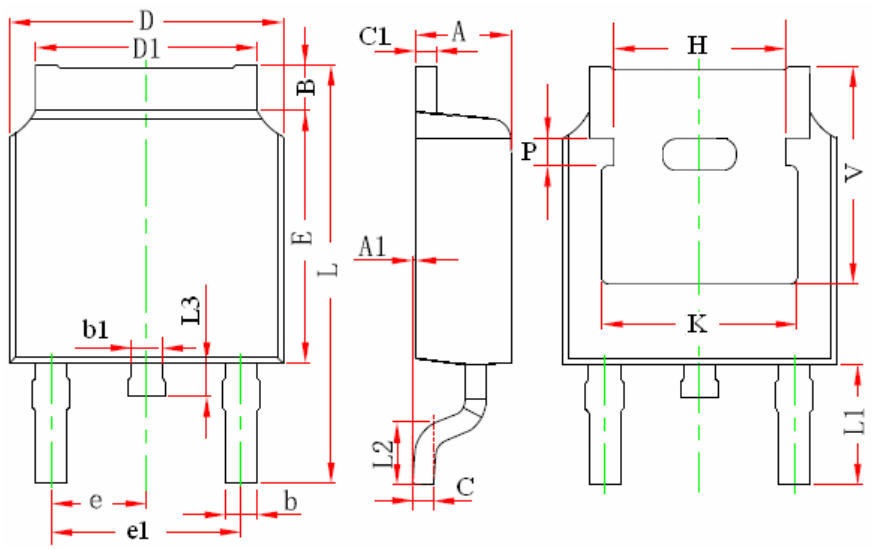
Recommended temperature profile for IR reflow

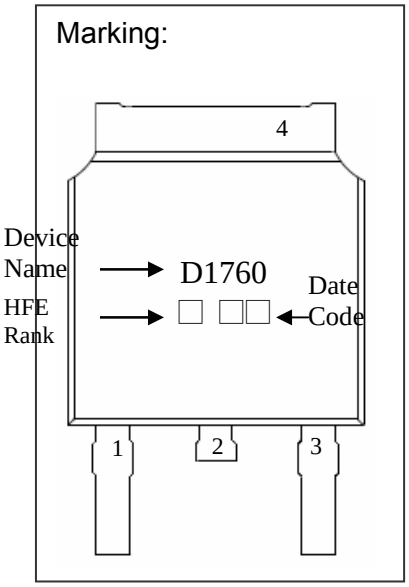


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-252 Dimension





3-Lead TO-252 Plastic Surface Mount Package
CYStek Package Code: J3

Style: Pin 1.Base 2.Collector 3.Emitter 4.Collector

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	e	0.086	0.094	2.186	2.386
A1	0.000	0.005	0.000	0.127	e1	0.172	0.188	4.372	4.772
B	0.039	0.048	0.990	1.210	H	0.163	REF	4.140	REF
b	0.026	0.034	0.660	0.860	K	0.190	REF	4.830	REF
b1	0.026	0.034	0.660	0.860	L	0.386	0.409	9.800	10.400
C	0.018	0.023	0.460	0.580	L1	0.114	REF	2.900	REF
C1	0.018	0.023	0.460	0.580	L2	0.055	0.067	1.400	1.700
D	0.256	0.264	6.500	6.700	L3	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	P	0.026	REF	0.650	REF
E	0.236	0.244	6.000	6.200	V	0.211	REF	5.350	REF

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.