

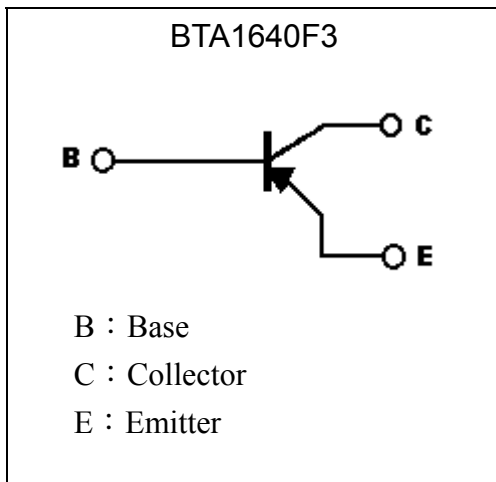
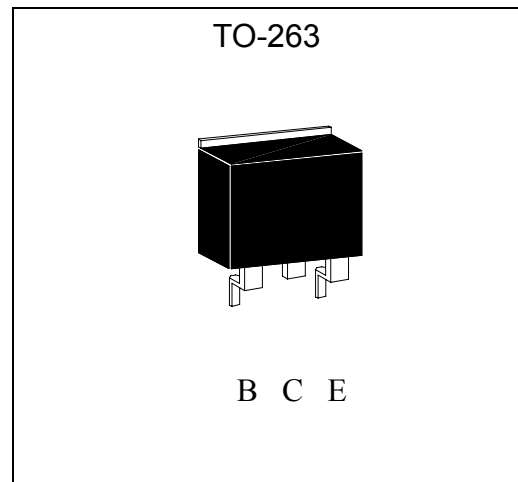
PNP Epitaxial Planar Power Transistor

BTA1640F3

BV_{CEO}	-30V
I_C	-7A
$V_{CE(SAT)}$	-0.4V(max)

Features

- Low collector-emitter saturation voltage, $V_{CE(sat)} = -0.4V(max)$ @ $I_C = -3A, I_B = -0.1A$
- Excellent current gain linearity
- Pb-free lead plating package

Symbol

Outline

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-30	V
Collector-Emitter Voltage	V_{CEO}	-30	V
Emitter-Base Voltage	V_{EBO}	-18	V
Collector Current (DC)	I_C	-7	A
Collector Current (Pulse)	I_{CP}	-10 (Note 1)	
Power Dissipation @ $T_A=25^\circ C$	P_D	2	W
Power Dissipation @ $T_C=25^\circ C$	P_D	60	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Operating Junction Temperature Range	T_j	-55~+150	°C
Storage Temperature Range	T_{stg}	-55~+150	°C

Note : 1. Single Pulse , $P_w \leq 300\mu s$, Duty $\leq 2\%$.



Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
*BV _{CEO}	-30	-	-	V	I _C =-10mA, I _B =0
BV _{CBO}	-30	-	-	V	I _C =-1mA, I _E =0
BV _{EBO}	-18	-	-	V	I _E =-1mA, I _C =0
I _{CEO}	-	-	-50	μA	V _{CE} =-30V, I _B =0
I _{CBO}	-	-	-10	μA	V _{CB} =-30V, I _B =0
I _{EBO}	-	-	-10	μA	V _{EB} =-18V, I _C =0
*V _{CE(sat)}	-	-	-0.4	V	I _C =-3A, I _B =-100mA
*V _{BE(sat)}	-	-	-1	V	I _C =-3A, I _B =-100mA
*h _{FE}	180	-	350	-	V _{CE} =-2V, I _C =-200mA

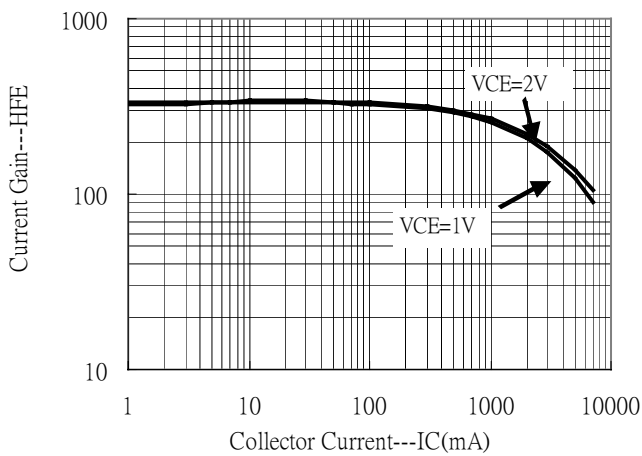
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

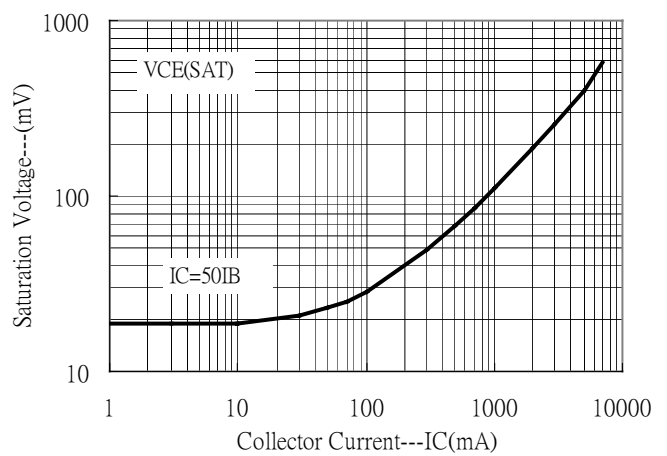
Device	Package	Shipping	Marking
BTA1640F3	TO-263 (Pb-free lead plating package)	800 pcs / Tape & Reel	A1640

Typical Characteristics

Current Gain vs Collector Current

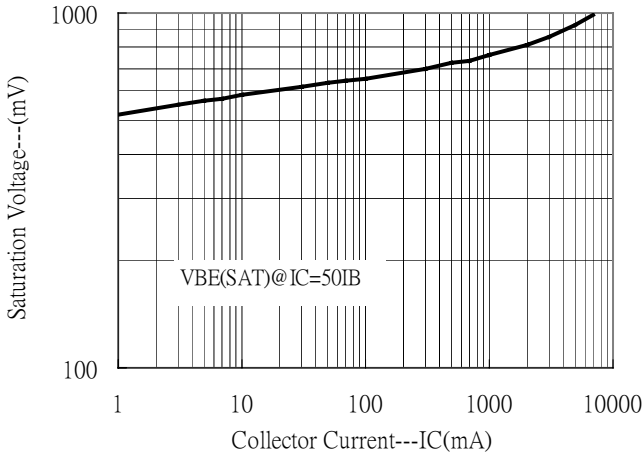


Saturation Voltage vs Collector Current

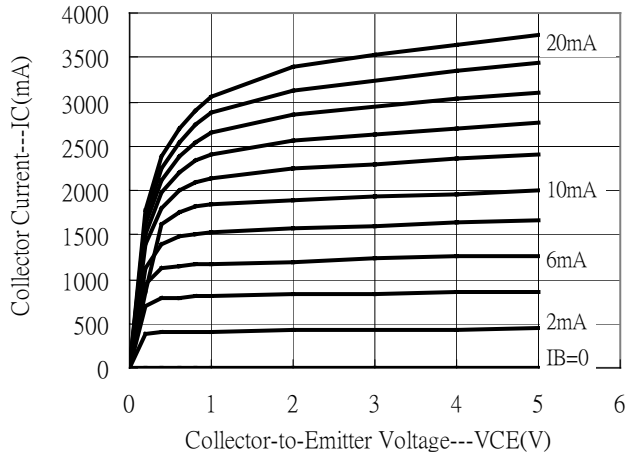


Typical Characteristics(Cont.)

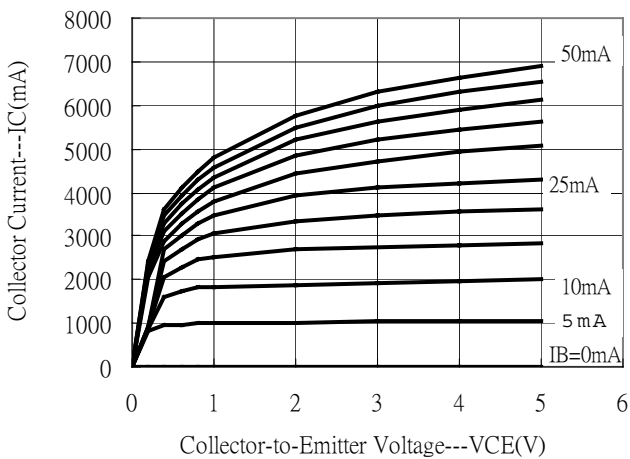
Saturation Voltage vs Collector Current



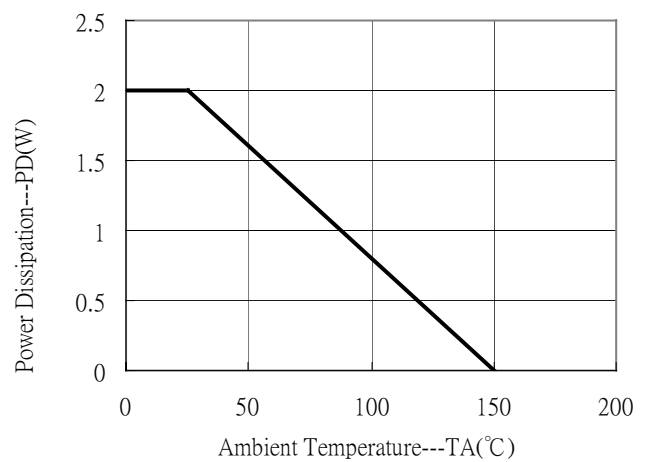
Grounded Emitter Output Characteristics



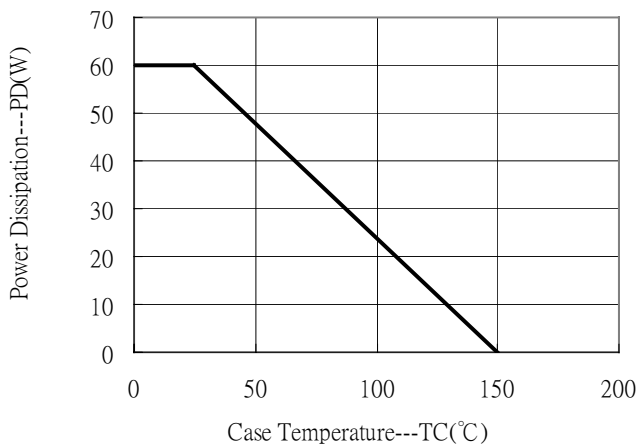
Grounded Emitter Output Characteristics



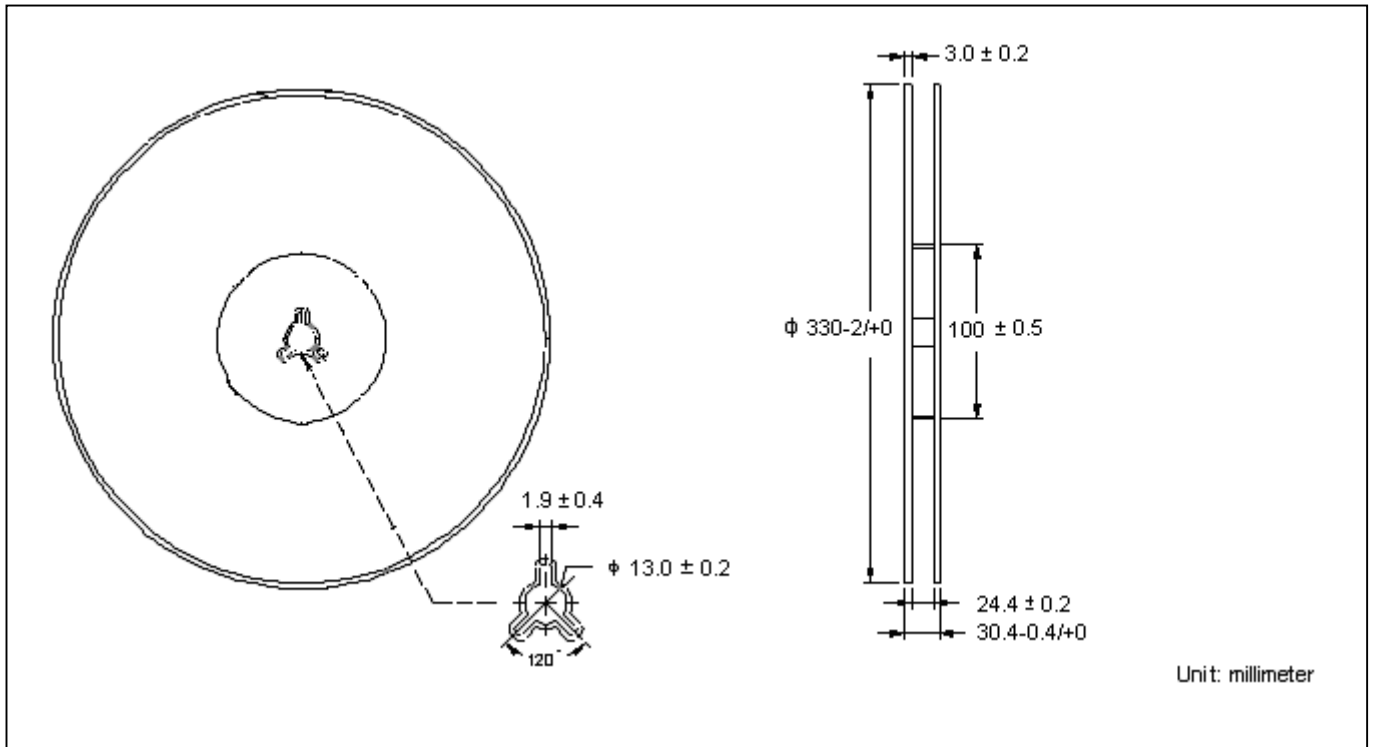
Power Derating Curve



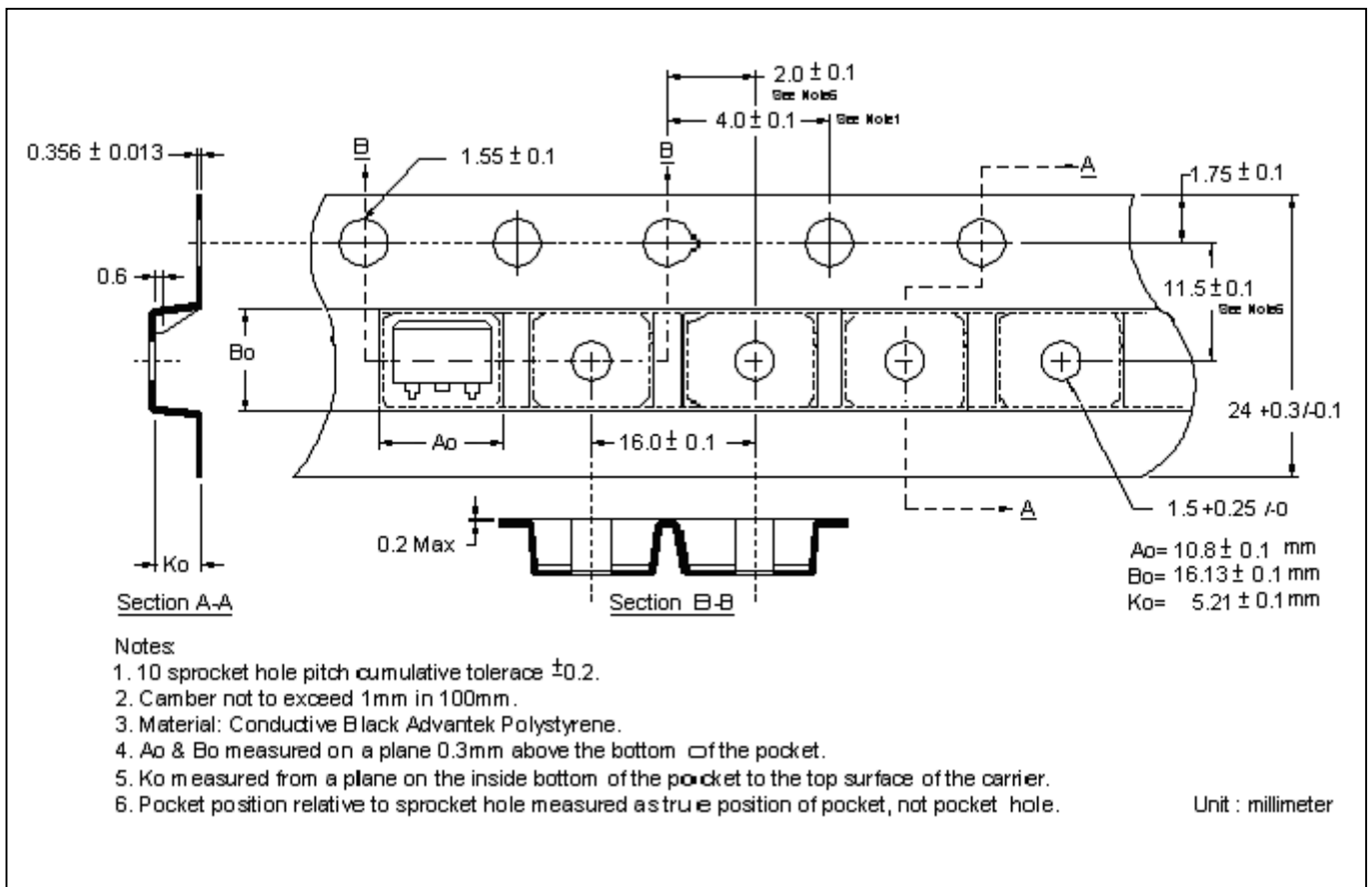
Power Derating Curve



Reel Dimension



Carrier Tape Dimension

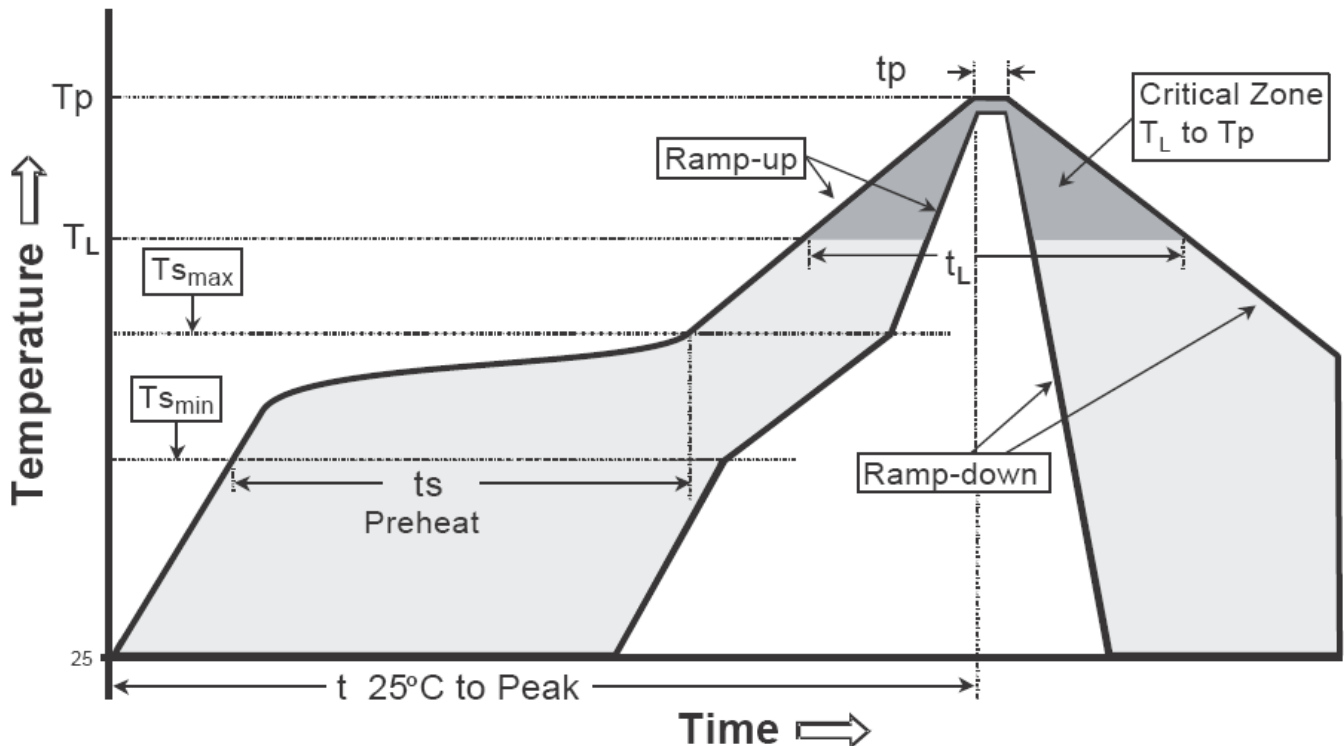


Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
2. Camber not to exceed 1mm in 100mm.
3. Material: Conductive Black Advantek Polystyrene.
4. A_o & B_o measured on a plane 0.3mm above the bottom of the pocket.
5. K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Recommended wave soldering condition

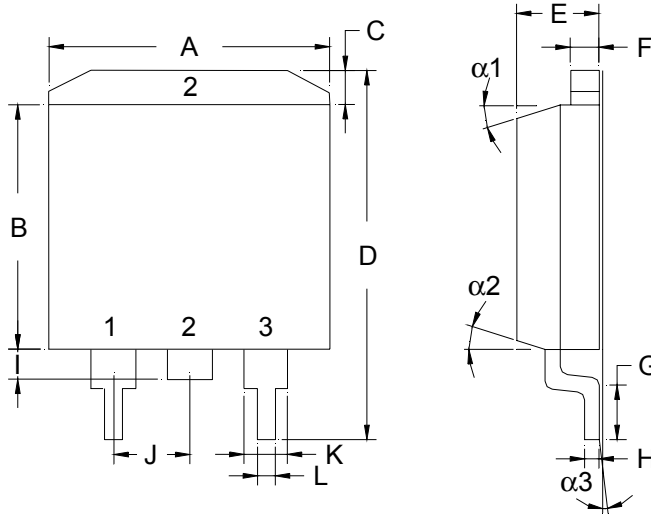
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


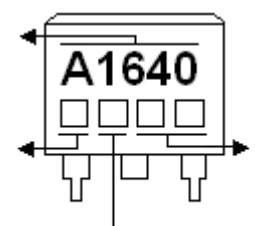
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-263 Dimension



Marking :



Device Name ← **A1640**

Year Code:
 9→2009, 0→2010, ..., etc ← **01** Lot No.: 01~99

Month Code:
 1→Jan, 2→Feb, ..., 9→Sep, A→Oct, B→Nov, C→Dec ← **99**

Style : Pin 1.Base 2.Collector 3.Emitter
 3-Lead Plastic Surface Mounted Package
 CYStek Package Code : F3

*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.3800	0.4050	9.65	10.29	I	0.0500	0.0700	1.27	1.78
B	0.3300	0.3700	8.38	9.40	J	-	*0.1000	-	*2.54
C	-	0.0550	-	1.40	K	0.0450	0.0550	1.14	1.40
D	0.5750	0.6250	14.61	15.88	L	0.0200	0.0390	0.51	0.99
E	0.1600	0.1900	4.06	4.83	$\alpha 1$	-	-	6°	8°
F	0.0450	0.0550	1.14	1.40	$\alpha 2$	-	-	6°	8°
G	0.0900	0.1100	2.29	2.79	$\alpha 3$	-	-	0°	5°
H	0.0180	0.0290	0.46	0.74					

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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