Silicon PNP Epitaxial Planar Transistor

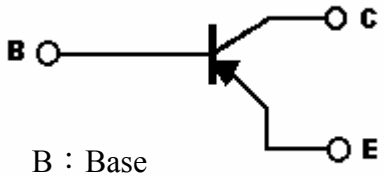
BTA1972K3

Description

- High BV_{CEO}
- High current capability
- Pb-free lead plating and halogen-free package

Symbol

BTA1972K3



B：Base
C：Collector
E：Emitter

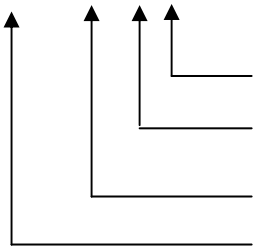
Outline

TO-92L

E C B

Ordering Information

Device	Package	Shipping
BTA1972K3-0-TB-G	TO-92L (Pb-free lead plating and halogen-free package)	2000 pcs / tape & box
BTA1972K3-0-BM-G	TO-92L (Pb-free lead plating and halogen-free package)	500 pcs / bag, 10 bags/box, 10 boxes/carton



Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

Packing spec, TB : 2000 pcs / tape & box ; BM : 500 pcs/bag, 10 bags/box, 10 boxes/carton

Product rank, zero for no rank products

Product name

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-400	V
Collector-Emitter Voltage	V_{CEO}	-400	V
Emitter-Base Voltage	V_{EBO}	-7	V
Collector Current (DC)	I_C	-0.3	A
Collector Current (Pulse)	I_{CP}	-7	A
Base Current	I_B	-0.1	A
Collector Power Dissipation	P_C	900	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55~+150	°C

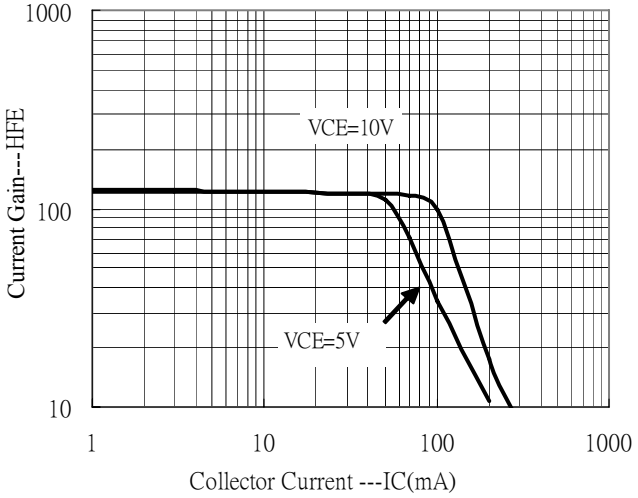
Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	-400	-	-	V	I_C=-50μA
BV_{CEO}	-400	-	-	V	I_C=-1mA
BV_{EBO}	-7	-	-	V	I_E=-50μA
I_{CBO}	-	-	-1	μA	V_{CB}=-400V
I_{EBO}	-	-	-100	nA	V_{EB}=-7V
I_{CES}	-	-	-1	μA	V_{CE}=-400V, V_{BE}=0V
*$V_{CE(sat)}$ 1	-	-0.08	-0.15	V	I_C=-10mA, I_B=-1mA
*$V_{CE(sat)}$ 2	-	-0.12	-0.2	V	I_C=-50mA, I_B=-5mA
*$V_{CE(sat)}$ 3	-	-0.2	-0.4	V	I_C=-100mA, I_B=-10mA
*$V_{BE(sat)}$	-	-0.8	-1	V	I_C=-100mA, I_B=-10mA
h_{FE} 1	120	-	-	-	V_{CE}=-10V, I_C=-1mA
*h_{FE} 2	120	-	270	-	V_{CE}=-10V, I_C=-10mA
*h_{FE} 3	120	-	-	-	V_{CE}=-10V, I_C=-50mA
*h_{FE} 4	100	-	-	-	V_{CE}=-10V, I_C=-100mA
f_T	40	-	-	MHz	V_{CE}=-10V, I_C=-10mA
Cob	-	-	8	pF	V_{CB}=-10V, I_E=0A,f=1MHz

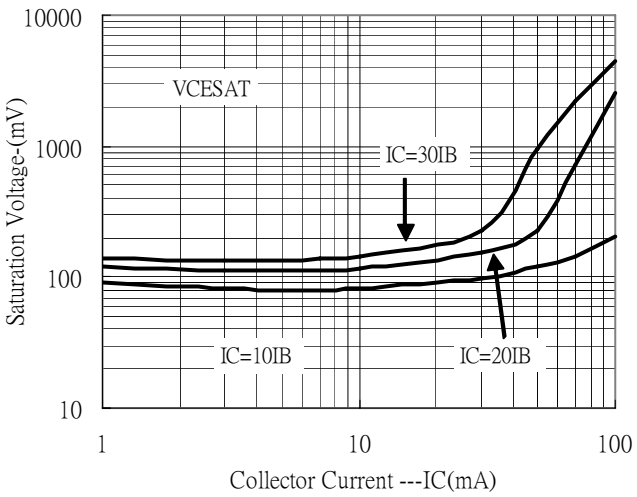
*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

Typical Characteristics

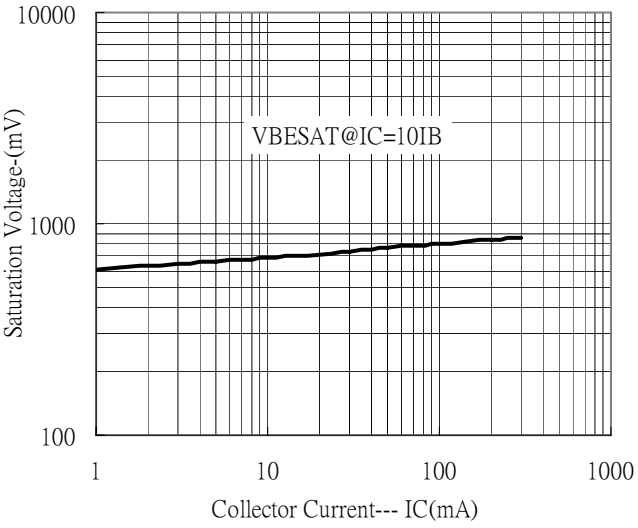
Current Gain vs Collector Current



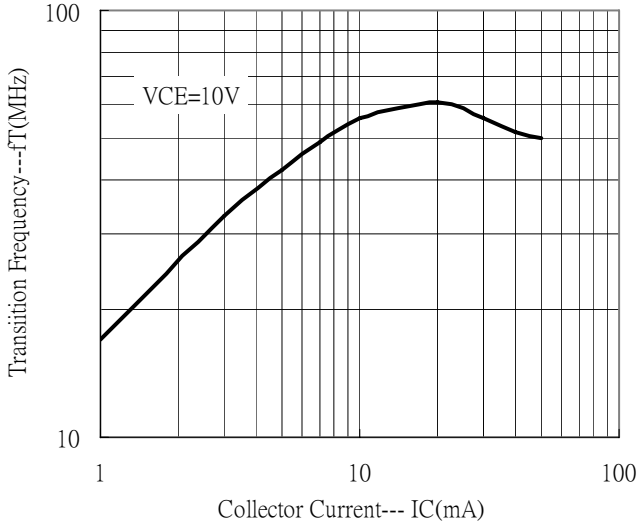
Saturation Voltage vs Collector Current



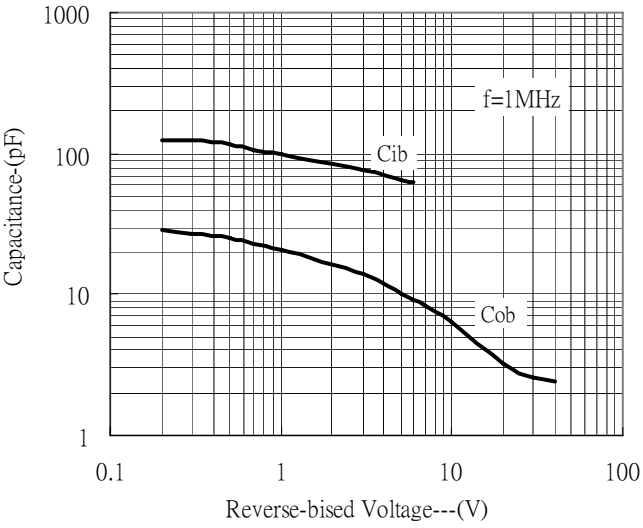
Saturation Voltage vs Collector Current



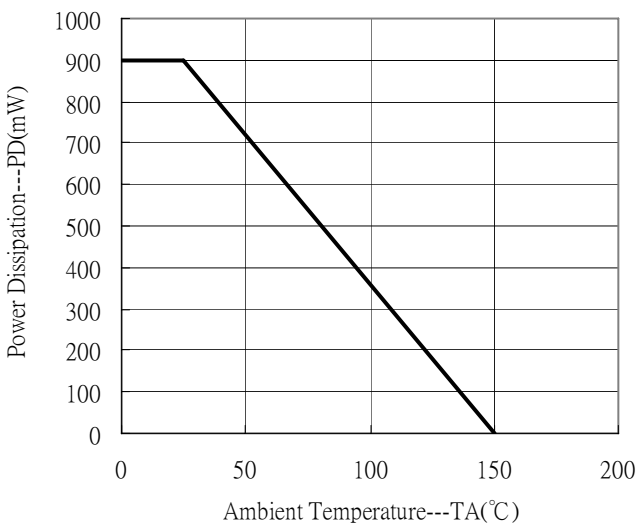
Transition Frequency vs Collector Current



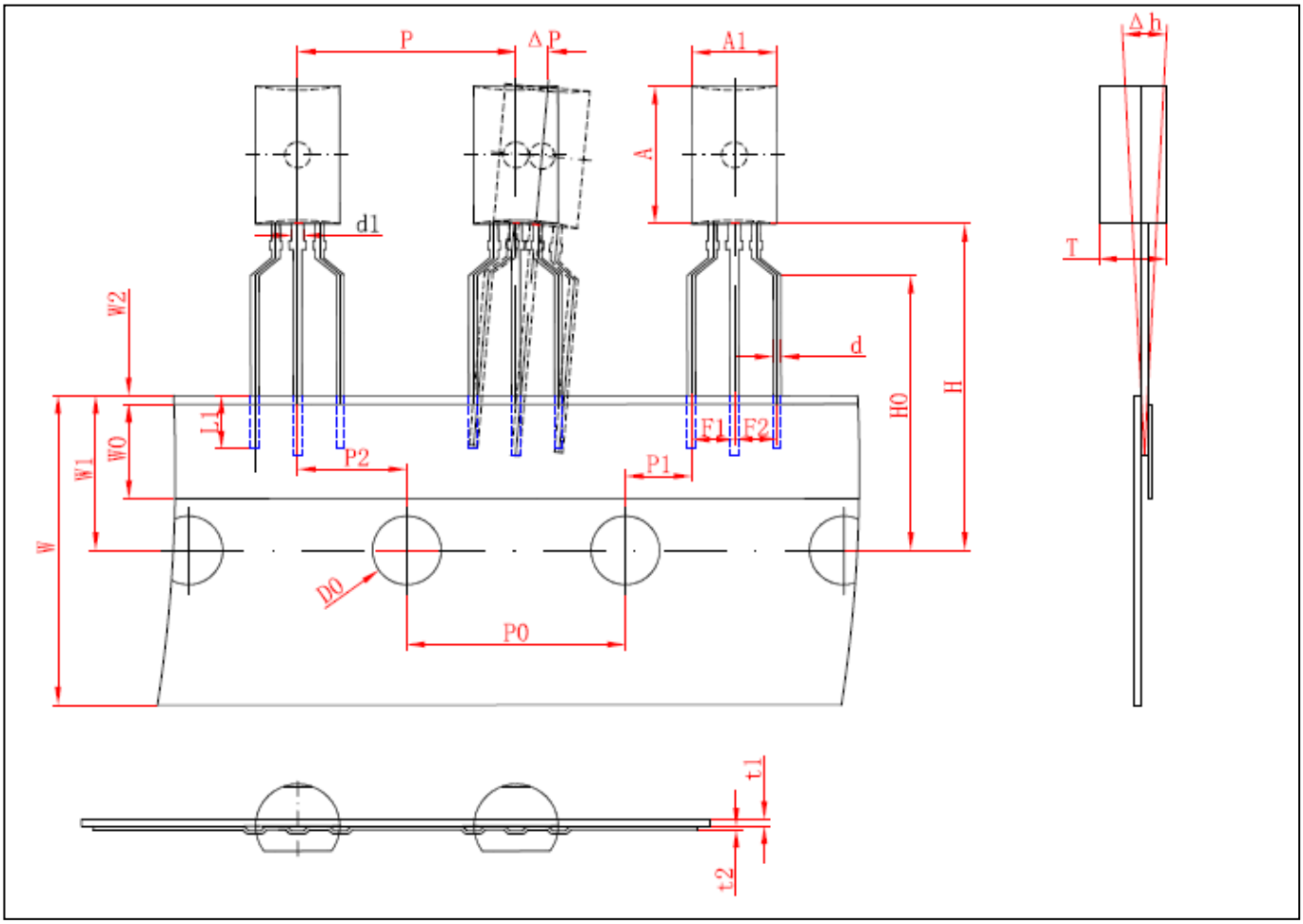
Capacitance Characteristics



Power Derating Curve



TO-92L Taping Outline

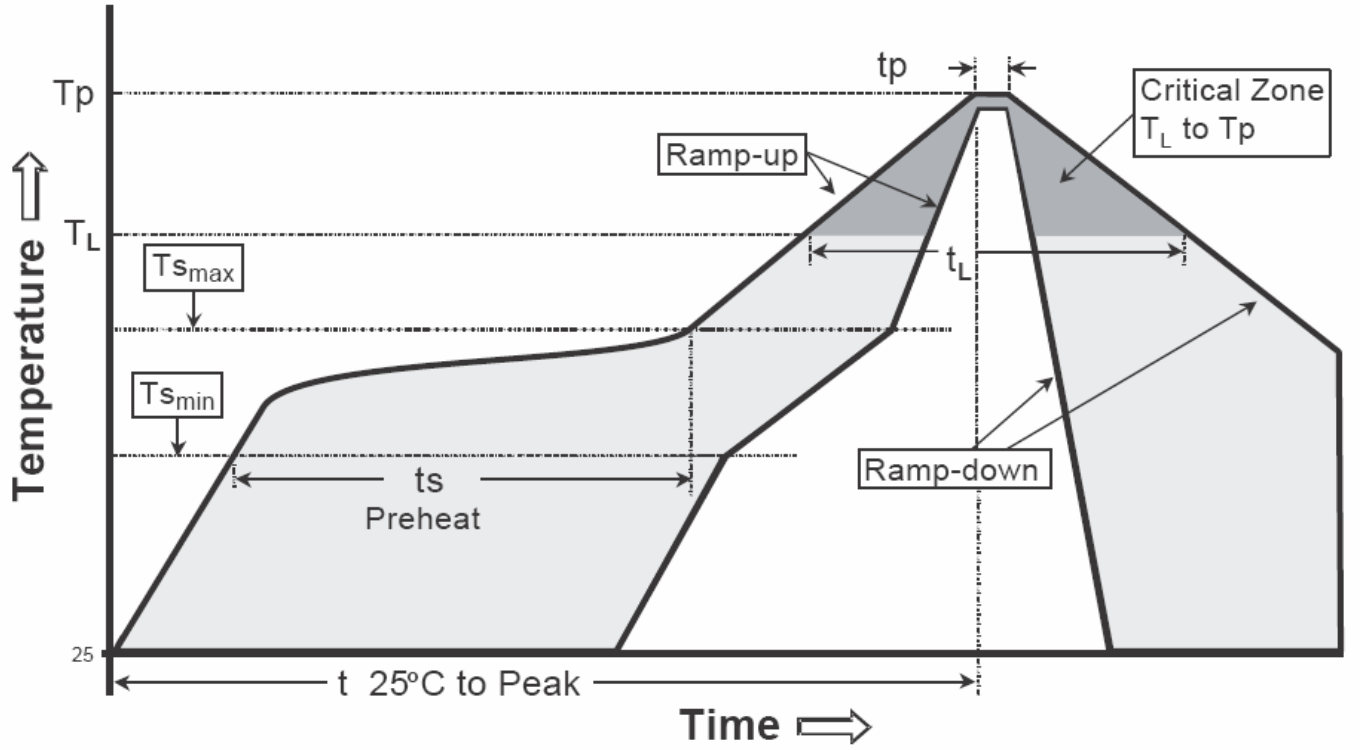


DIM	Item	Millimeters	
		Min.	Max.
A1	Component body width	4.70	5.10
A	Component body height	7.80	8.20
T	Component body thickness	3.70	4.10
d	Lead wire diameter	0.35	0.55
d1	Lead wire diameter 1	0.60	0.80
P	Pitch of component	12.40	13.00
P0	Feed hole pitch	12.50	12.90
P2	Hole center to component center	6.05	6.65
F1, F2	Lead to lead distance	2.20	2.80
△h	Component alignment, F-R	-1.00	1.00
W	Tape width	17.50	19.00
W0	Hole down tape width	5.50	6.50
W1	Hole position	8.50	9.50
W2	Hole down tape position	-	1.00
H	Height of component from tape center	19.00	21.00
H0	Lead wire clinch height	15.50	16.50
L1	Lead wire (tape portion)	2.50	-
D0	Feed hole diameter	3.80	4.20
t1	Taped lead thickness	0.35	0.45
t2	Carrier tape thickness	0.15	0.25
P1	Position of hole	3.55	4.15
△P	Component alignment	-1.00	1.00

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

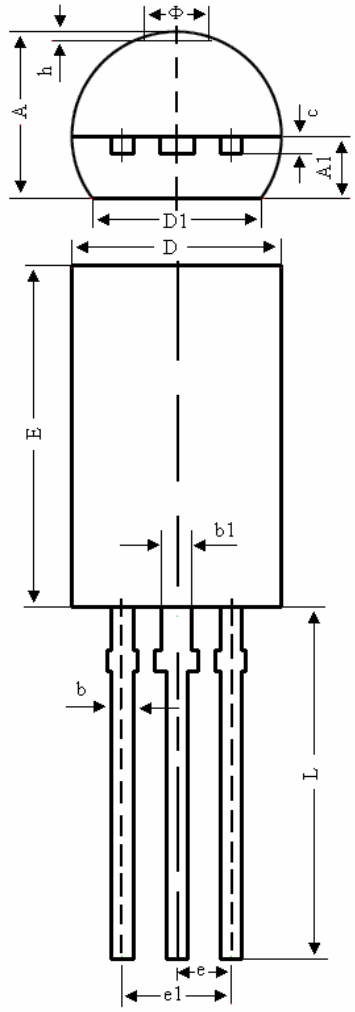
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-92L Dimension



Marking:

Product Name

A1972

□□

Date Code: Year+Month

Year: 7→2007, 8→2008

Month: 1→1, 2→2, • • • ,

9→9, A→10, B→11, C→12

Style: Pin 1.Emitter 2.Collector 3.Base

3-Lead TO-92L Plastic Package
CYStek Package Code: K3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.146	0.161	3.700	4.100	E	0.307	0.323	7.800	8.200
A1	0.050	0.062	1.280	1.580	e	*0.05		*1.270	
b	0.014	0.022	0.350	0.550	e1	0.096	0.104	2.440	2.640
b1	0.024	0.031	0.600	0.800	L	0.543	0.559	13.800	14.200
c	0.014	0.018	0.350	0.450	φ	-	0.063	-	1.600
D	0.185	0.201	4.700	5.100	h	0.000	0.012	0.000	0.300
D1	0.157	-	4.000	-					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.