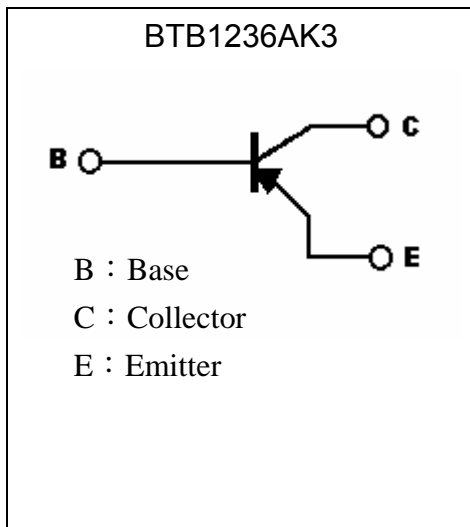
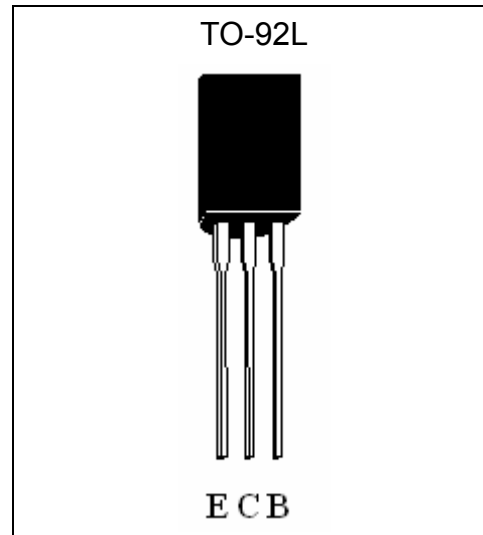


Silicon PNP Epitaxial Planar Transistor

BTB1236AK3

Description

- High BV_{CEO}
- High current capability
- Pb-free lead plating package

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^{\circ}\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-180	V
Collector-Emitter Voltage	V_{CEO}	-160	V
Emitter-Base Voltage	V_{EBO}	-7	V
Collector Current (DC)	I_C	-1.5	A
Collector Current (Pulse)	I_{CP}	-3	A
Base Current	I_B	0.5	A
Collector Power Dissipation	P_C	900	mW
Junction Temperature	T_j	150	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55~+150	$^{\circ}\text{C}$

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	-180	-	-	V	$I_C=-50\mu A, I_E=0$
BV_{CEO}	-160	-	-	V	$I_C=-1mA, I_B=0$
BV_{EBO}	-7	-	-	V	$I_E=-50\mu A, I_C=0$
I_{CBO}	-	-	-1	μA	$V_{CB}=-160V, I_E=0$
I_{EBO}	-	-	-1	μA	$V_{EB}=-5V, I_C=0$
* $V_{CE(sat)}$	-	-	-0.3	V	$I_C=-500mA, I_B=-50mA$
* $V_{CE(sat)}$	-	-	-0.6	V	$I_C=-1A, I_B=-100mA$
* $V_{BE(on)}$	-0.45	-	-0.75	V	$V_{CE}=-5V, I_C=-5mA$
h_{FE1}	100	-	320	-	$V_{CE}=-5V, I_C=-200mA$
h_{FE2}	30	-	-	-	$V_{CE}=-5V, I_C=-500mA$
f_T	-	180	-	MHz	$V_{CE}=-5V, I_C=-150mA$
Cob	-	24	-	pF	$V_{CB}=-10V, I_E=0, f=1MHz$

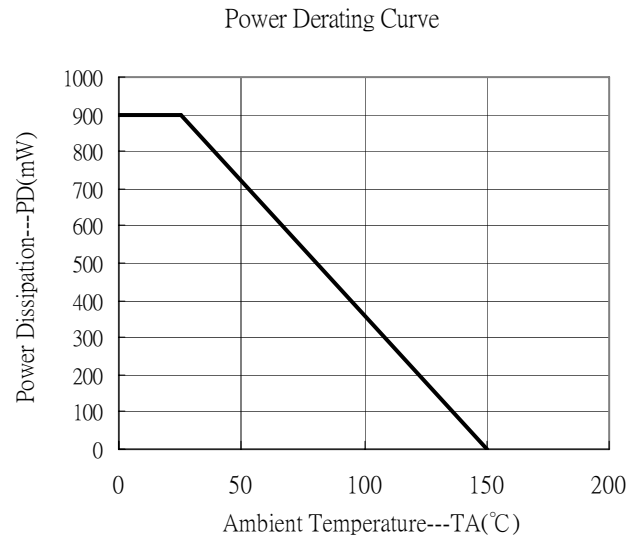
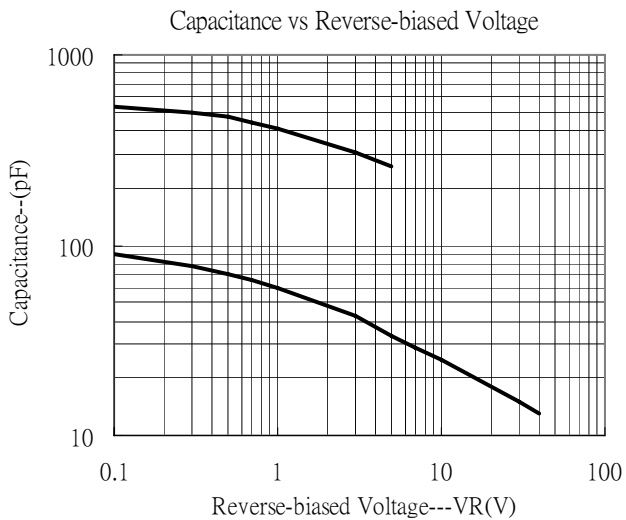
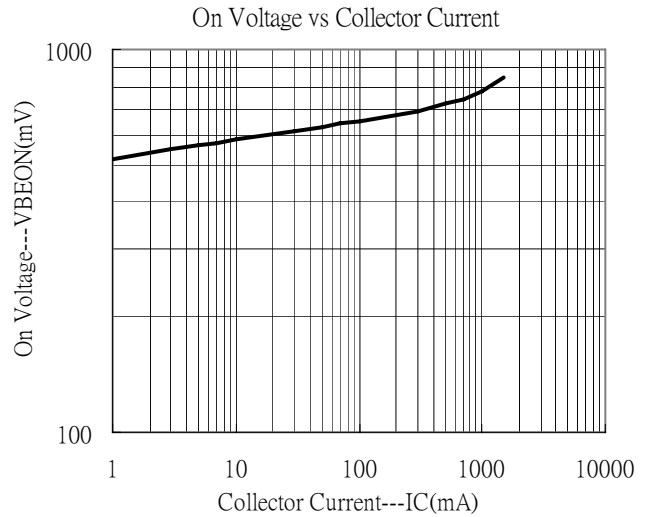
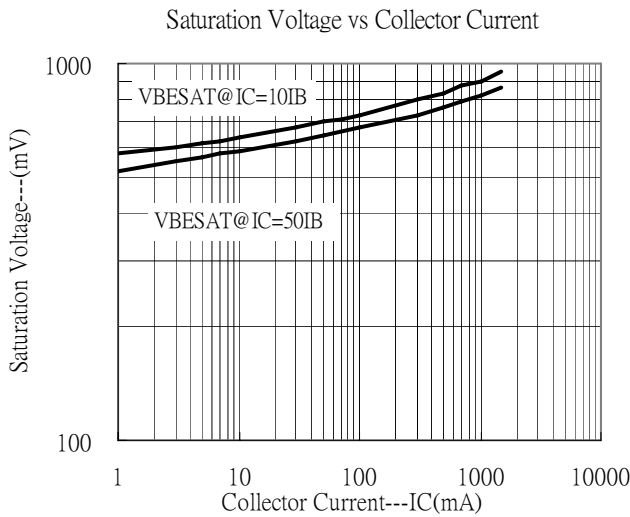
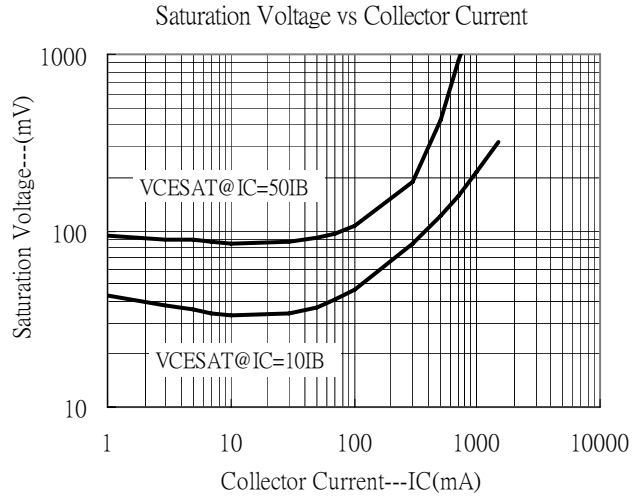
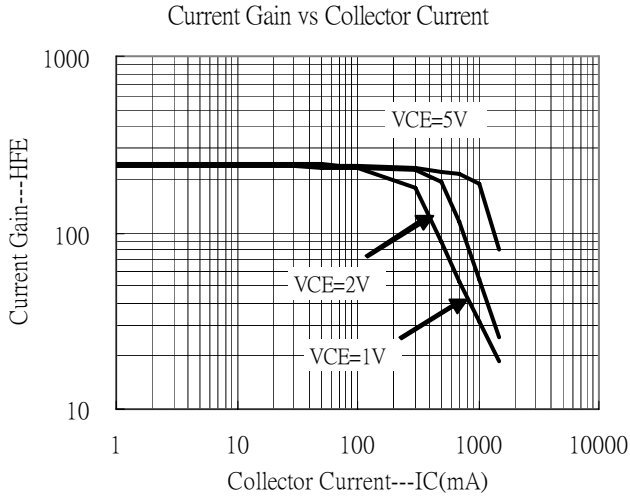
*Pulse Test: Pulse Width $\leq 380\mu s$, Duty Cycle $\leq 2\%$ **Classification Of h_{FE1}**

Rank	O	Y
Range	100~200	160~320

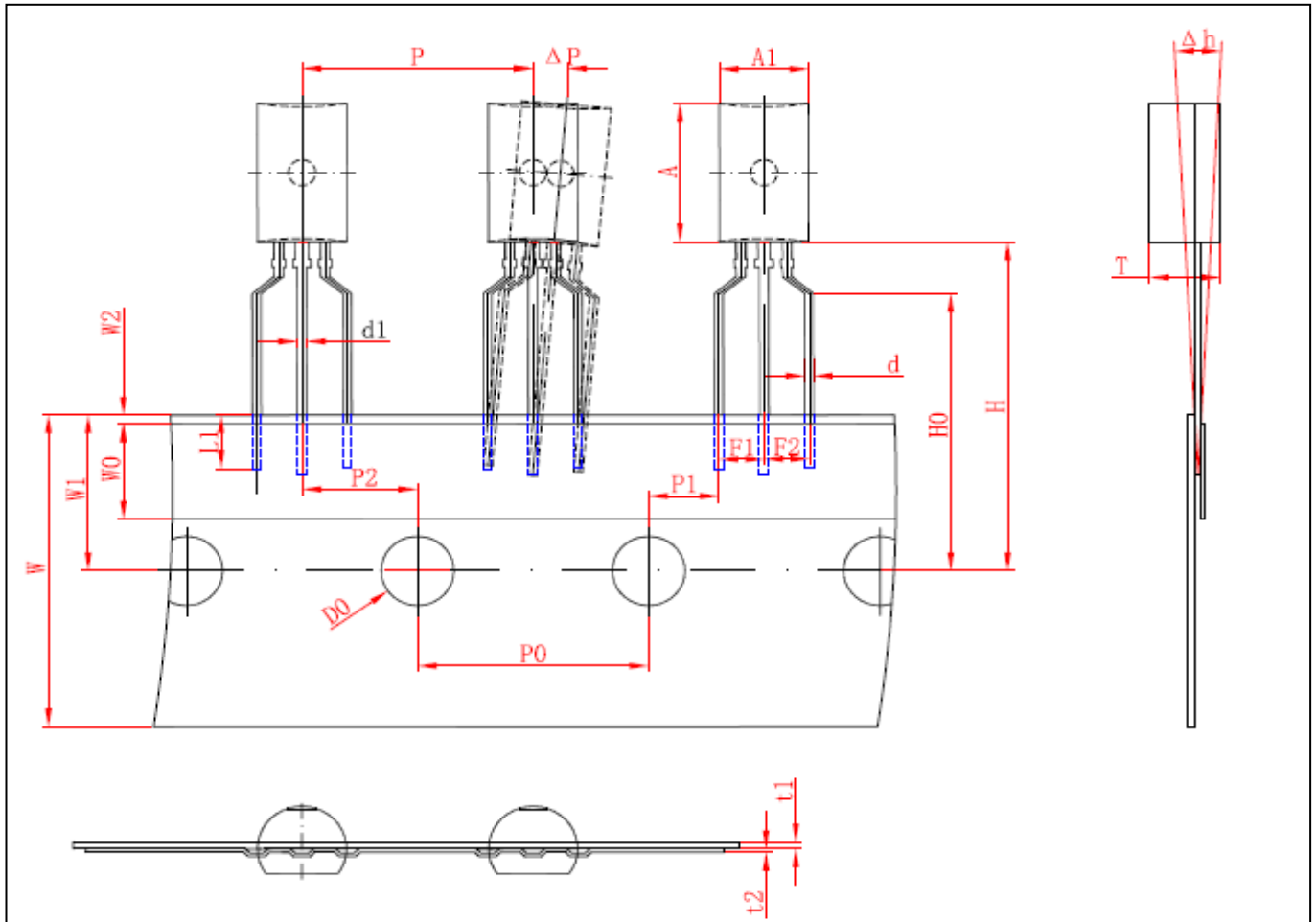
Ordering Information

Device	HFE rank	Package	Shipping
BTB1236AK3-O-BK-S	O	TO-92L (Pb-free lead plating)	500 pcs / bag, 10 bags/box, 10 boxes/carton
BTB1236AK3-Y-BK-S	Y	TO-92L (Pb-free lead plating)	500 pcs / bag, 10 bags/box, 10 boxes/carton
BTB1236AK3-O-TB-S	O	TO-92L (Pb-free lead plating)	2000 pcs / Tape & Box
BTB1236AK3-Y-TB-S	Y	TO-92L (Pb-free lead plating)	2000 pcs / Tape & Box

Typical Characteristics



TO-92L Taping Outline

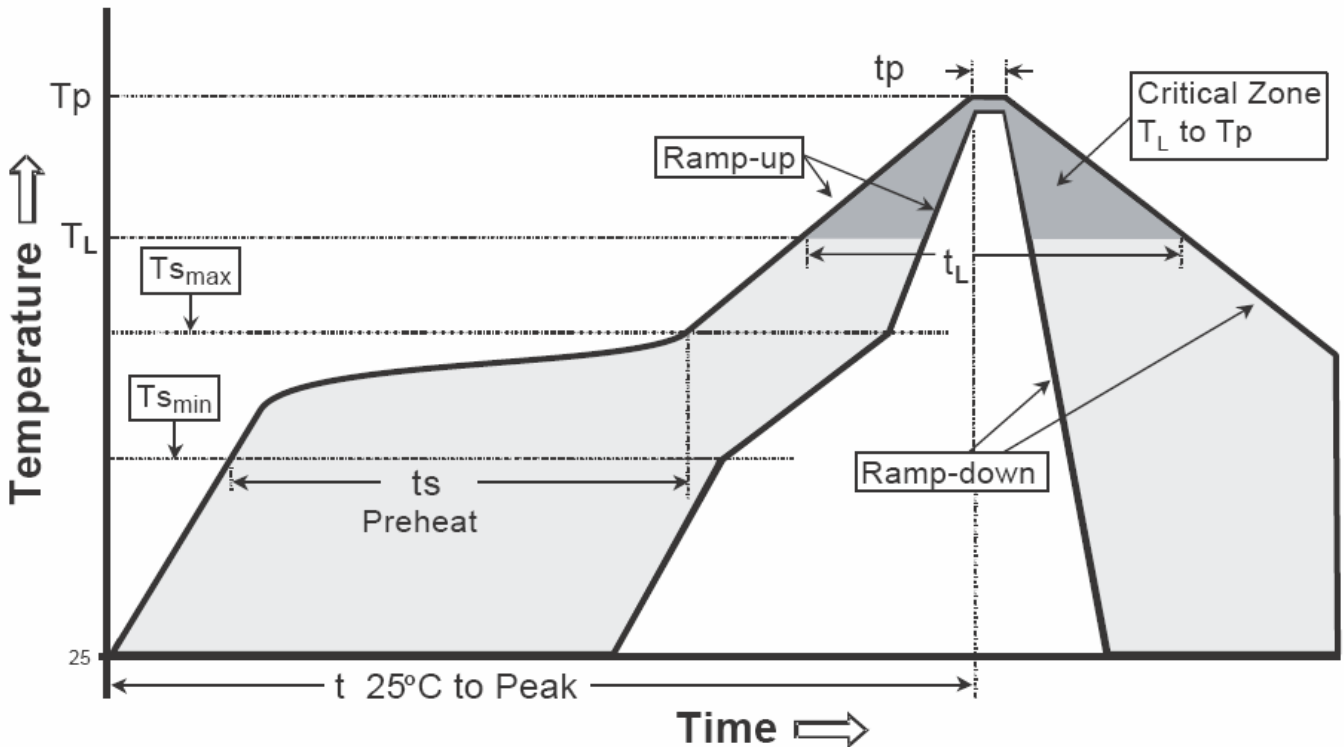


DIM	Item	Millimeters	
		Min.	Max.
A1	Component body width	4.70	5.10
A	Component body height	7.80	8.20
T	Component body thickness	3.70	4.10
d	Lead wire diameter	0.40	0.50
d1	Lead wire diameter 1	0.62	0.78
P	Pitch of component	12.40	13.00
P0	Feed hole pitch	12.50	12.90
P2	Hole center to component center	6.05	6.65
F1, F2	Lead to lead distance	2.20	2.80
Δh	Component alignment, F-R	-1.00	1.00
W	Tape width	17.50	19.00
W0	Hole down tape width	5.50	6.50
W1	Hole position	8.50	9.50
W2	Hole down tape position	-	1.00
H	Height of component from tape center	19.00	21.00
H0	Lead wire clinch height	15.50	16.50
L1	Lead wire (tape portion)	2.50	-
D0	Feed hole diameter	3.80	4.20
t1	Taped lead thickness	0.35	0.45
t2	Carrier tape thickness	0.15	0.25
P1	Position of hole	3.55	4.15
ΔP	Component alignment	-1.00	1.00

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

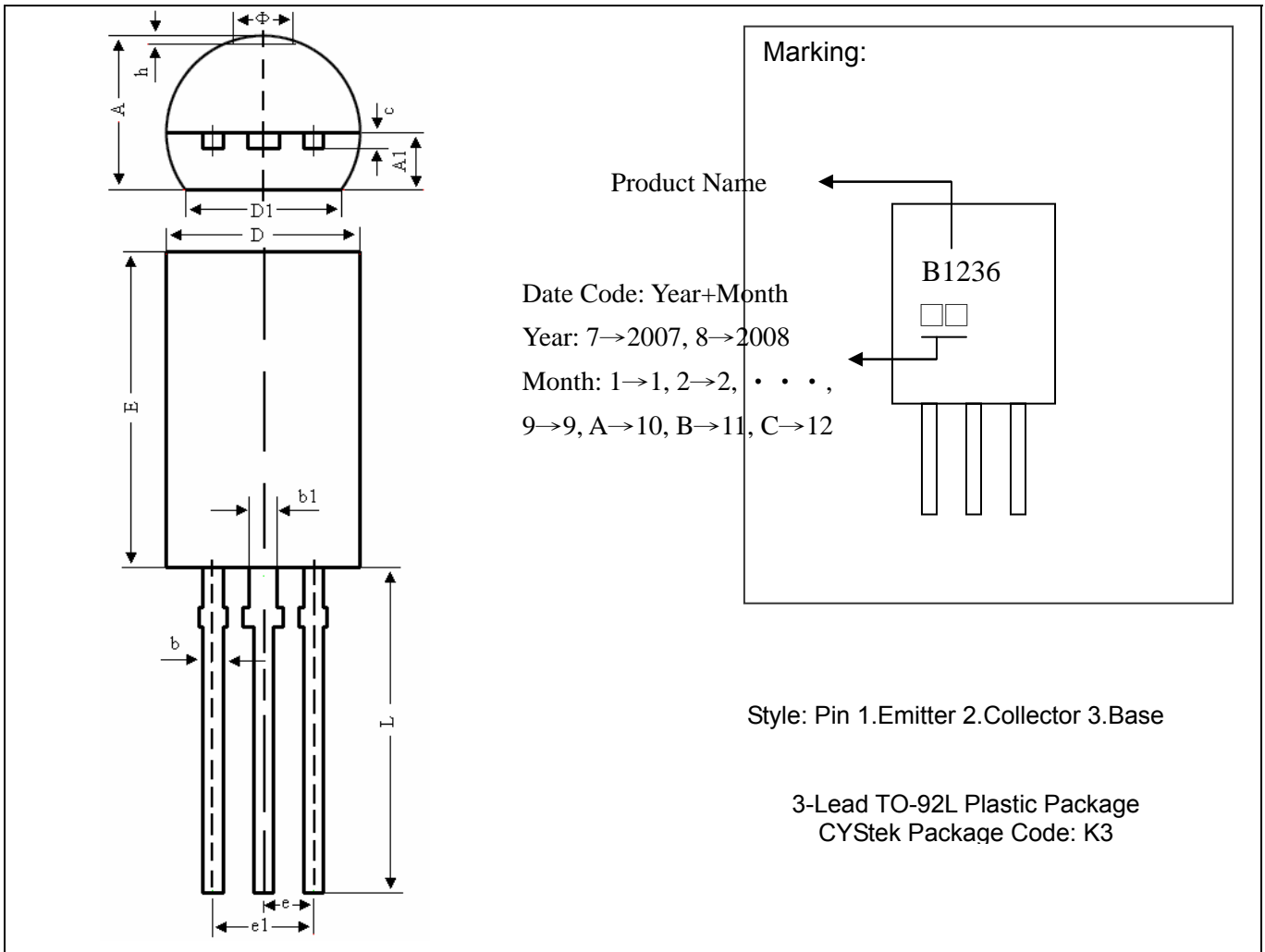
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-92L Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.146	0.161	3.700	4.100	E	0.307	0.323	7.800	8.200
A1	0.050	0.062	1.280	1.580	e	*0.05		*1.270	
b	0.014	0.022	0.350	0.550	e1	0.096	0.104	2.440	2.640
b1	0.024	0.031	0.600	0.800	L	0.543	0.559	13.800	14.200
c	0.014	0.018	0.350	0.450	phi	-	0.063	-	1.600
D	0.185	0.201	4.700	5.100	h	0.000	0.012	0.000	0.300
D1	0.157	-	4.000	-					

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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