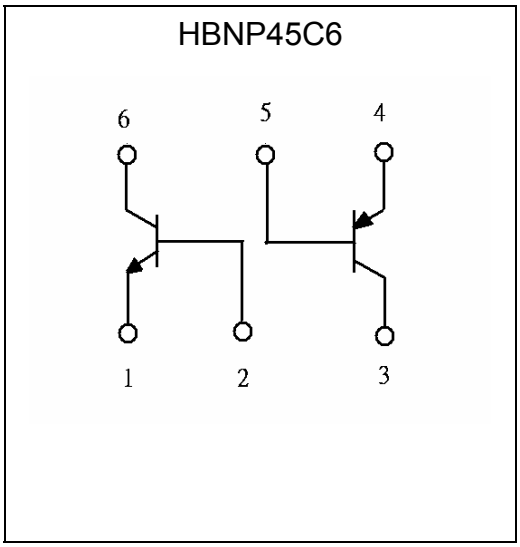
General Purpose NPN / PNP Epitaxial Planar Transistors (dual transistors)

HBNP45C6

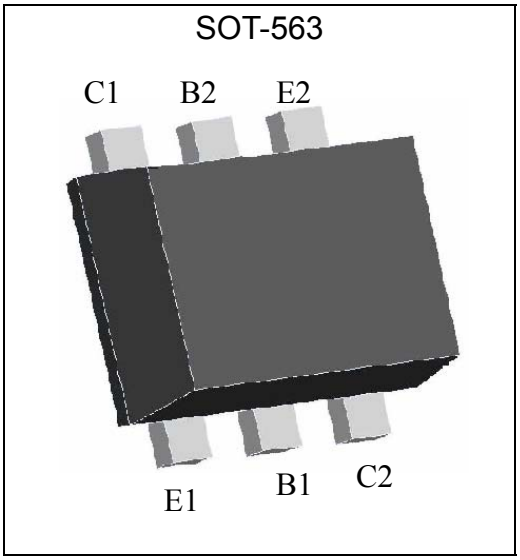
Features

- Includes a BTC2412 chip and a BTA1037 chip in a SOT-563 package.
- Mounting possible with SOT-523 automatic mounting machines.
- Transistor elements are independent, eliminating interference.
- Mounting cost and area can be cut in half.
- Pb-free lead plating and halogen-free package.

Equivalent Circuit



Outline



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		TR1 (NPN)	TR2 (PNP)	
Collector-Base Voltage	V_{CBO}	60	-60	V
Collector-Emitter Voltage	V_{CEO}	50	-50	V
Emitter-Base Voltage	V_{EBO}	7	-6	V
Collector Current	I_C	150	-150	mA
Power Dissipation	Pd	150(total) *1		mW
Junction Temperature	Tj	150		°C
Storage Temperature	Tstg	-55~+150		°C

Note: *1 120mW per element must not be exceeded.

Characteristics (Ta=25°C)

- **TR1 (NPN)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	60	-	-	V	I_C=100μA
BV_{CEO}	50	-	-	V	I_C=1mA
BV_{EBO}	7	-	-	V	I_E=50μA
I_{CBO}	-	-	0.1	μA	V_{CB}=60V
I_{EBO}	-	-	0.1	μA	V_{EB}=7V
*$V_{CE(sat)}$	-	0.2	0.4	V	I_C=50mA, I_B=5mA
*h_{FE}	200	-	600		V_{CE}=6V, I_C=1mA
f_T	80	180	-	MHz	V_{CE}=12V, I_C=2mA, f=100MHz
Cob	-	2	3.5	pF	V_{CB}=12V, f=1MHz

*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

- **TR2 (PNP)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	-60	-	-	V	I_C=-50μA
BV_{CEO}	-50	-	-	V	I_C=-1mA
BV_{EBO}	-6	-	-	V	I_E=-50μA
I_{CBO}	-	-	-0.1	μA	V_{CB}=-60V
I_{EBO}	-	-	-0.1	μA	V_{EB}=-6V
*$V_{CE(sat)}$	-	-0.25	-0.5	V	I_C=-50mA, I_B=-5mA
*h_{FE}	200	-	600		V_{CE}=-6V, I_C=-1mA
f_T	60	140	-	MHz	V_{CE}=-12V, I_C=-2mA, f=100MHz
Cob	-	4	5	pF	V_{CB}=-12V, f=1MHz

*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

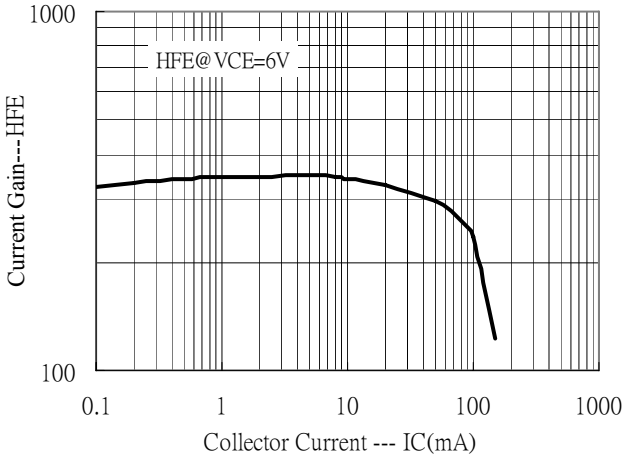
Ordering Information

Device	Package	Shipping
HBNP45C6-0-T1-G	SOT-363 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel

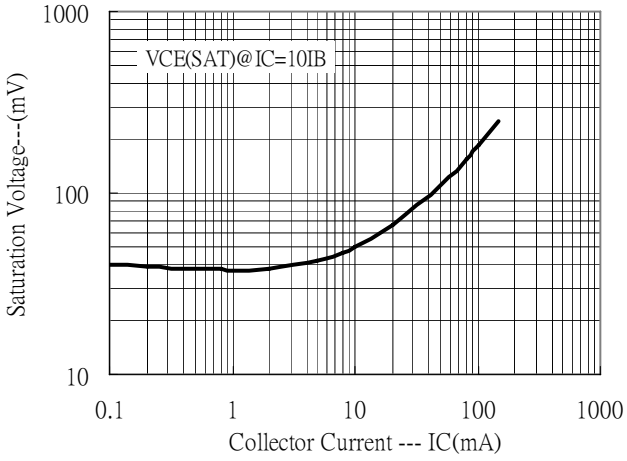
Characteristic curves

- **TR1 (NPN)**

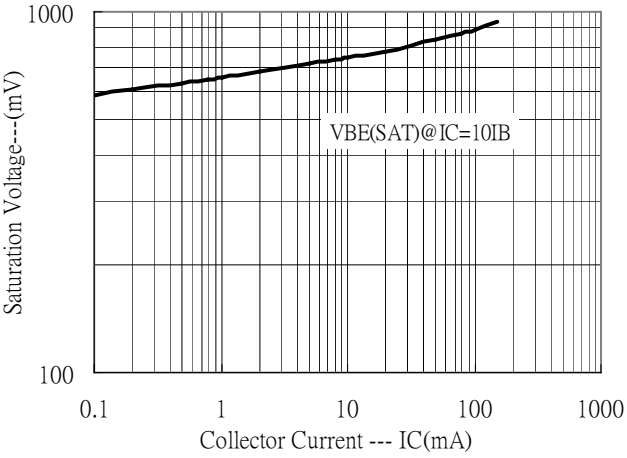
Current Gain vs Collector Current



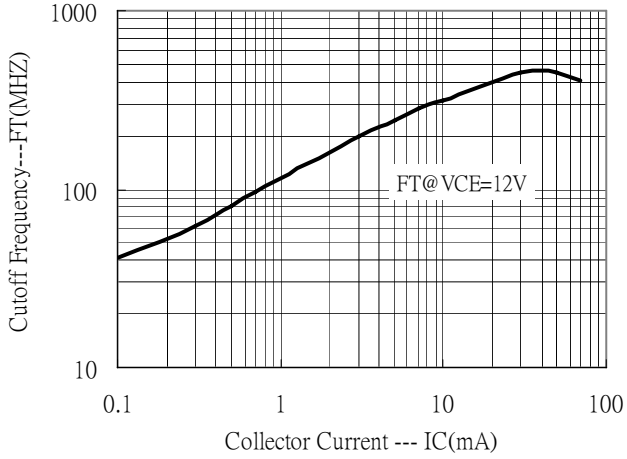
Saturation Voltage vs Collector Current



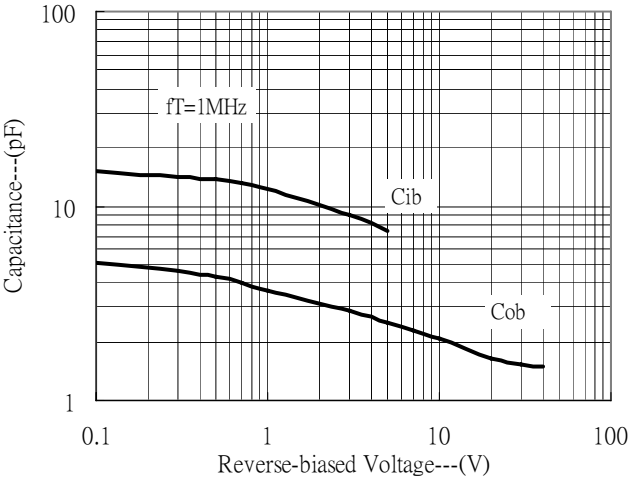
Saturation Voltage vs Collector Current



Cutoff Frequency vs Collector Current

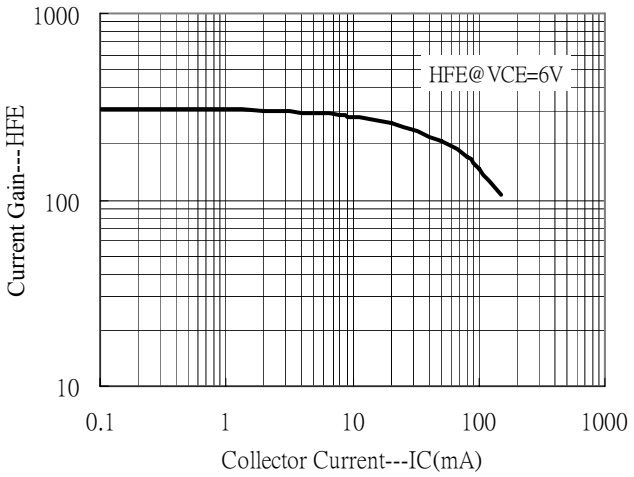


Capacitance Characteristics

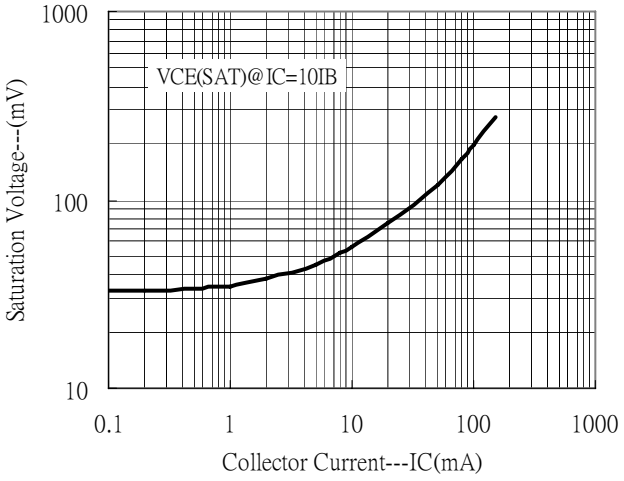


• TR2 (PNP)

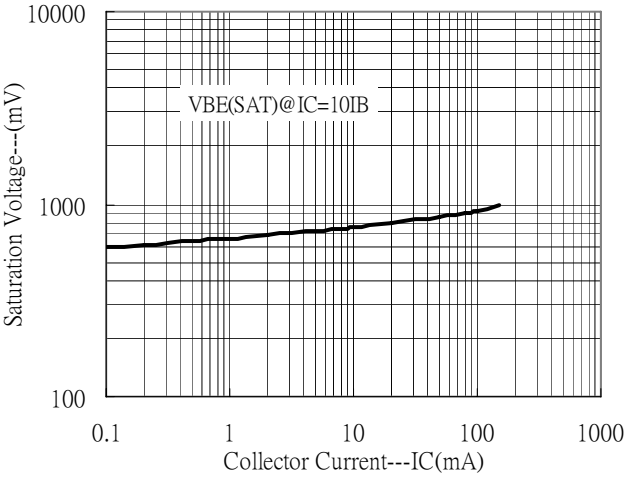
Current Gain vs Collector Current



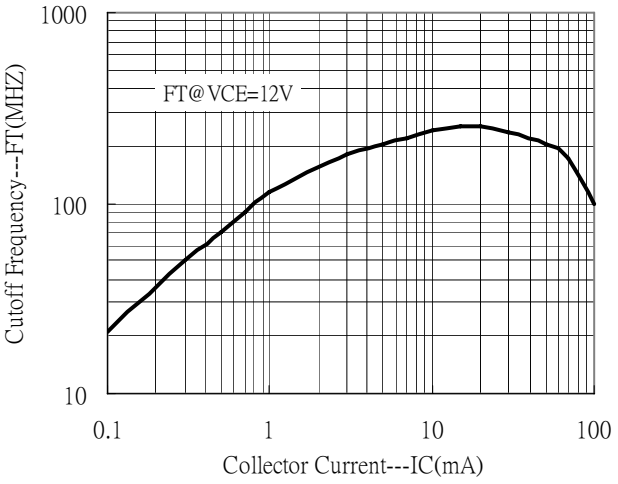
Saturation Voltage vs Collector Current



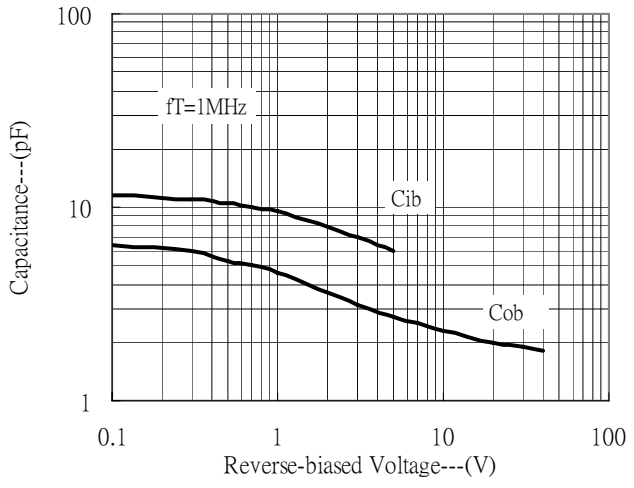
Saturation Voltage vs Collector Current



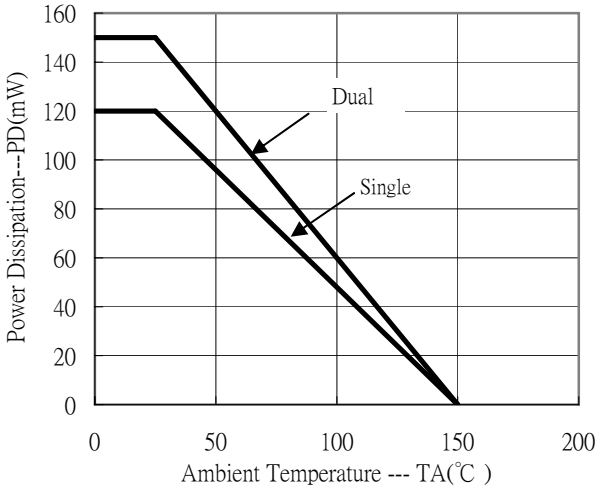
Cutoff Frequency vs Collector Current



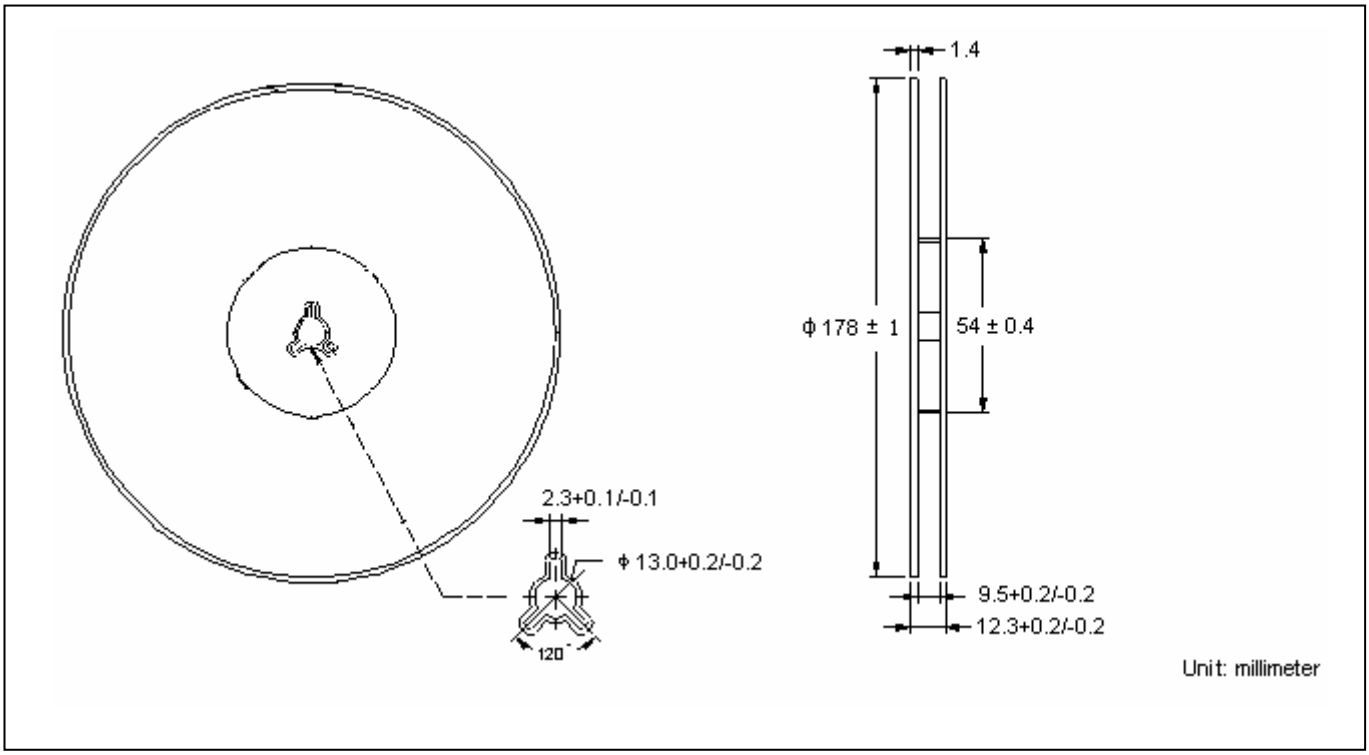
Capacitance Characteristics



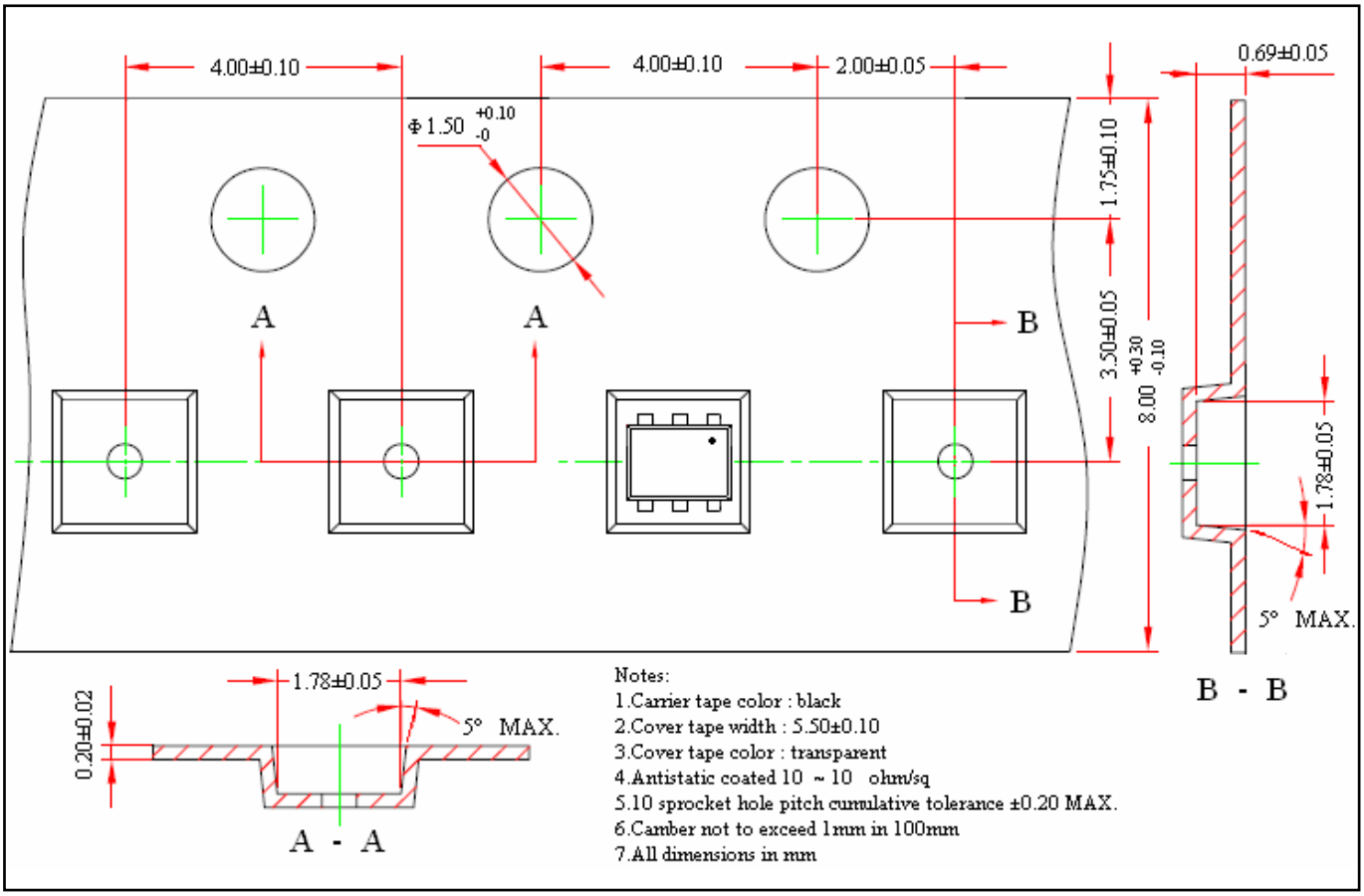
Power Derating Curves



Reel Dimension



Carrier Tape Dimension

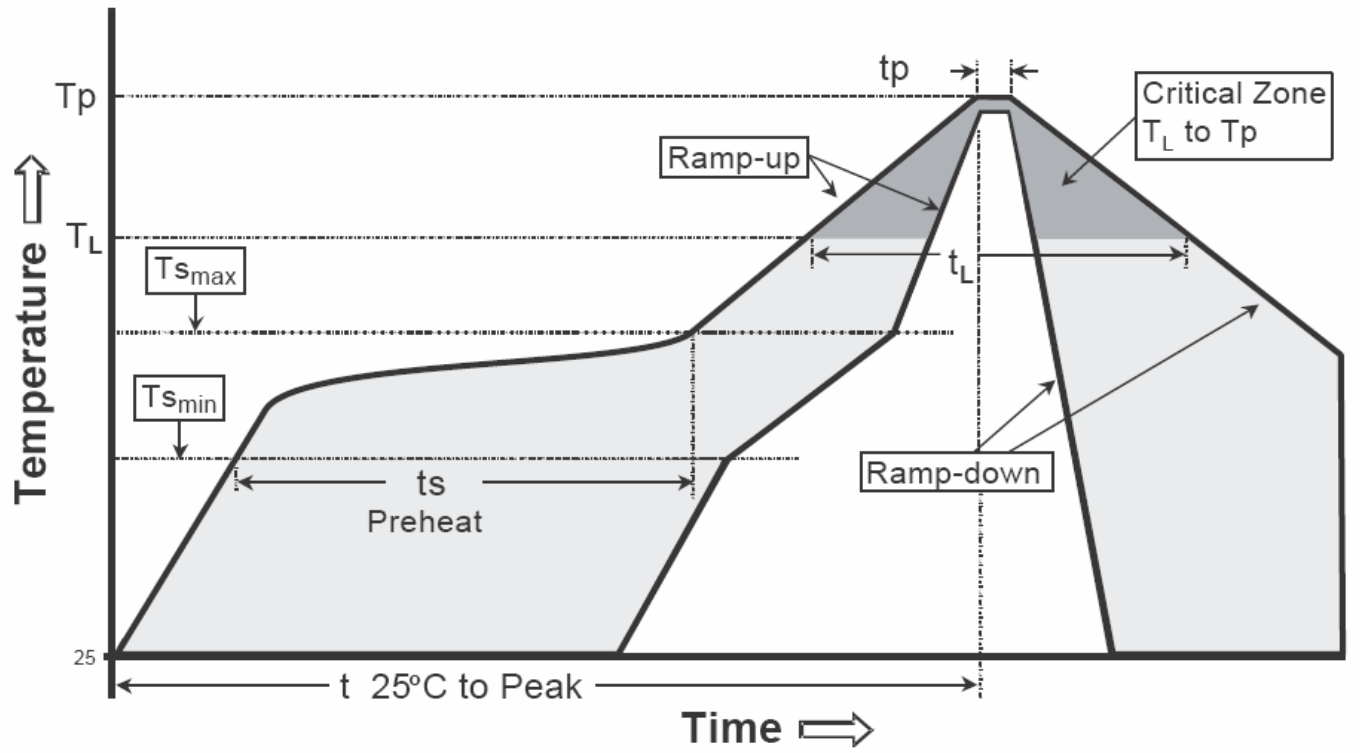


Notes:
1.Carrier tape color : black
2.Cover tape width : 5.50±0.10
3.Cover tape color : transparent
4.Antistatic coated 10 ~ 10 ohm/sq
5.10 sprocket hole pitch cumulative tolerance ±0.20 MAX.
6.Camber not to exceed 1mm in 100mm
7.All dimensions in mm

Recommended wave soldering condition

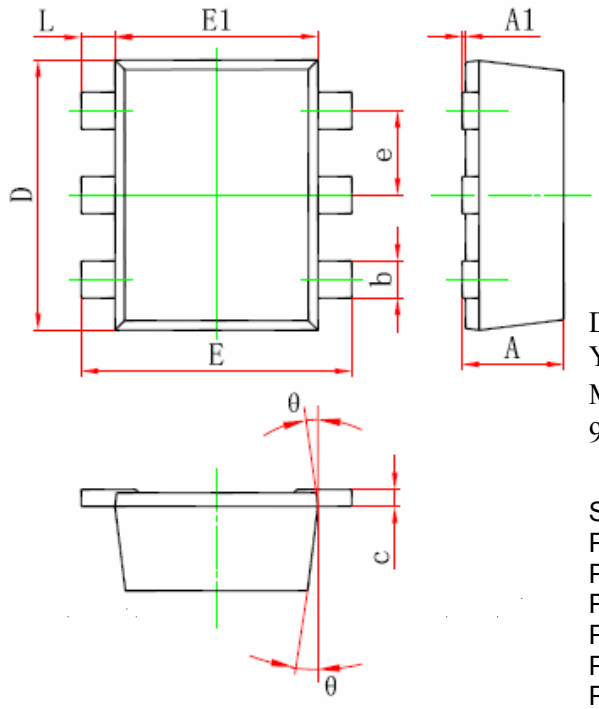
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow

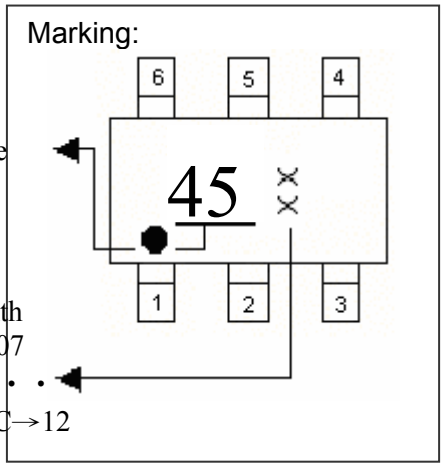


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(Ts min) −Temperature Max(Ts max) −Time(ts min to ts max)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

SOT-563 Dimension



Marking:



Product Code

Date Code: Year+Month
Year: 6→2006, 7→2007
Month: 1→1, 2→2, • • •
9→9, A→10, B→11, C→12

Style:
Pin 1. Emitter1 (E1)
Pin 2. Base1 (B1)
Pin 3. Collector2 (C2)
Pin 4. Emitter2 (E2)
Pin 5. Base2 (B2)
Pin 6. Collector1 (C1)

6-Lead SOT-563 Plastic
Surface Mounted Package
CYStek Package Code: C6

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.021	0.024	0.525	0.600	b	0.007	0.011	0.170	0.270
A1	0.000	0.002	0.000	0.050	E1	0.043	0.051	1.100	1.300
e	0.018	0.022	0.450	0.550	E	0.059	0.067	1.500	1.700
c	0.004	0.006	0.090	0.160	L	0.004	0.012	0.100	0.300
D	0.059	0.067	1.500	1.700	θ	7° REF		7° REF	

Notes : 1.Controlling dimension : millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.