Low Vcesat PNP Epitaxial Planar Transistor

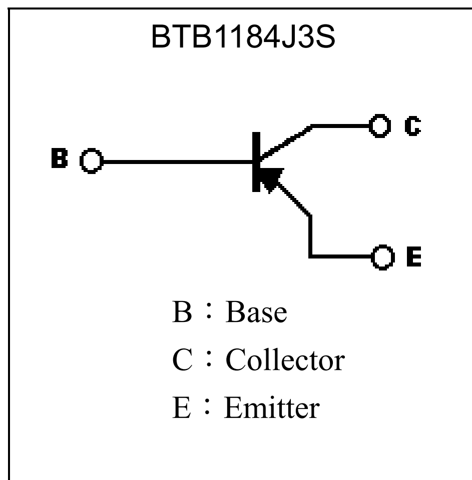
BTB1184J3S

BV_{CEO}	-50V
I_C	-3A
R_{CESAT}	130mΩ

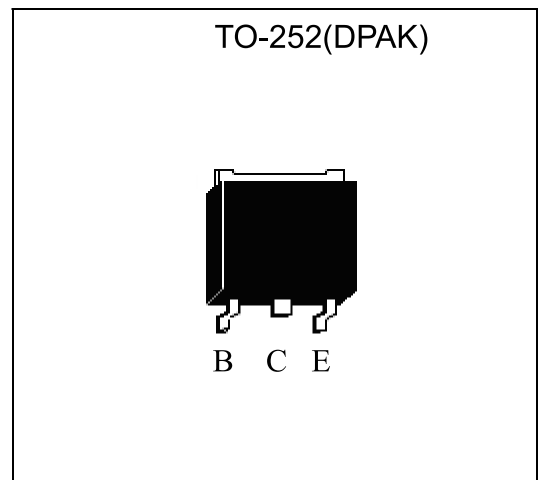
Features

- Low V_{CE}(sat)
- Excellent current gain characteristics
- RoHS compliant and halogen-free package

Symbol

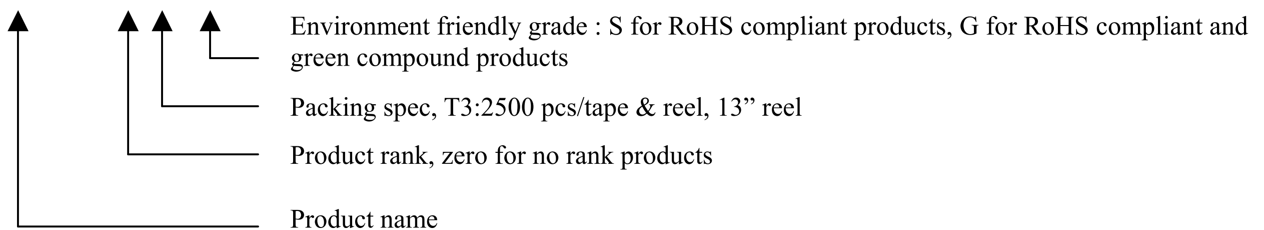


Outline



Ordering Information

Device	Package	Shipping
BTB1184J3S-S-T3-G	TO-252 (RoHS compliant and halogen-free package)	2500 pcs / Tape & Reel



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-60	V
Collector-Emitter Voltage	V_{CEO}	-50	V
Emitter-Base Voltage	V_{EBO}	-6	V
Collector Current(DC)	I_C	-3	A
Collector Current(Pulse)	I_{CP}	-7 *1	A
Power Dissipation (T_A=25℃)	Pd(T_A=25℃)	1	W
Power Dissipation (T_C=25℃)	Pd(T_C=25℃)	15 *2	W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33 *2	°C/W
Operating Junction and Storage Temperature Range	Tj,Tstg	-55~+150	°C

Note : *1. Single Pulse Pw=10ms

*2 . Printed circuit board, 1.7mm thick, collector copper plating 10mm*10mm or larger.

Characteristics (Ta=25°C)

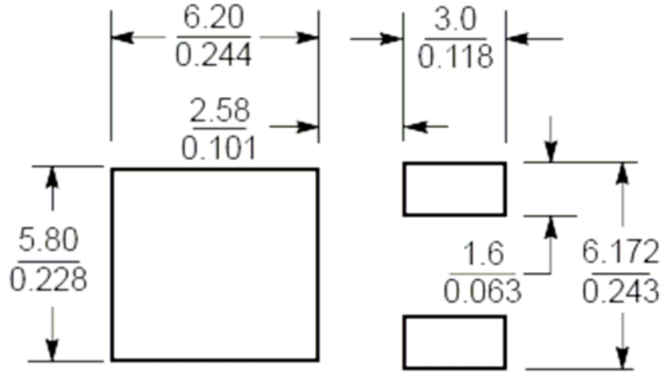
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	-60	-	-	V	I_C=-50μA, I_E=0
BV_{CEO}	-50	-	-	V	I_C=-1mA, I_B=0
BV_{EBO}	-6	-	-	V	I_E=-50μA, I_C=0
I_{CBO}	-	-	-1	μA	V_{CB}=-40V, I_E=0
I_{EBO}	-	-	-1	μA	V_{EB}=-4V, I_C=0
*$V_{CE(sat)}$	-	-0.26	-0.5	V	I_C=-2A, I_B=-0.1A
*$R_{CE(sat)}$	-	130	250	mΩ	I_C=-2A, I_B=-0.1A
*$V_{BE(sat)}$	-	-0.96	-1.2	V	I_C=-2A, I_B=-0.1A
*$h_{FE}1$	200	-	-	-	V_{CE}=-2V, I_C=-20mA
*$h_{FE}2$	270	-	560	-	V_{CE}=-3V, I_C=-500mA
*$h_{FE}3$	80	-	-	-	V_{CE}=-2V, I_C=-1A
f_T	-	80	-	MHz	V_{CE}=-5V, I_C=-0.1A, f=100MHz
Cob	-	35	-	pF	V_{CB}=-10V, f=1MHz

*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

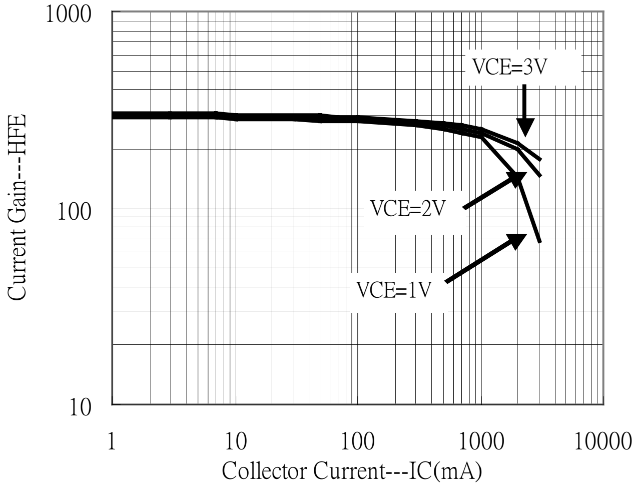
Classification Of $h_{FE}2$

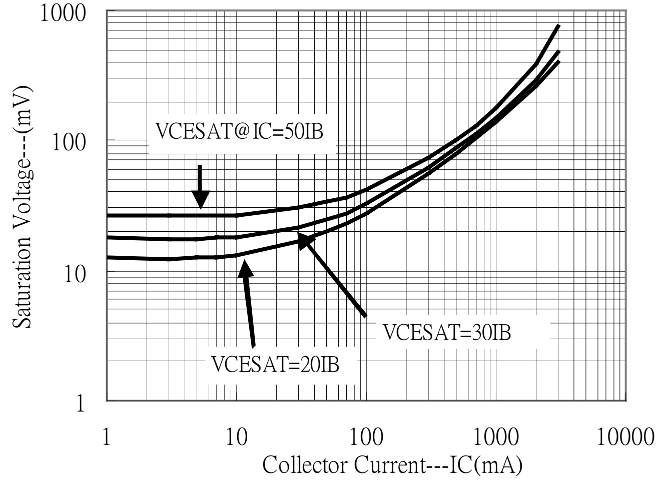
Rank	S
Range	270~560

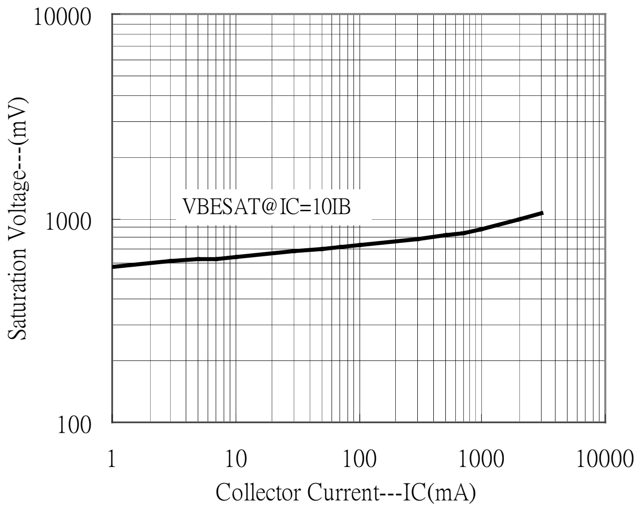
Recommended soldering footprint

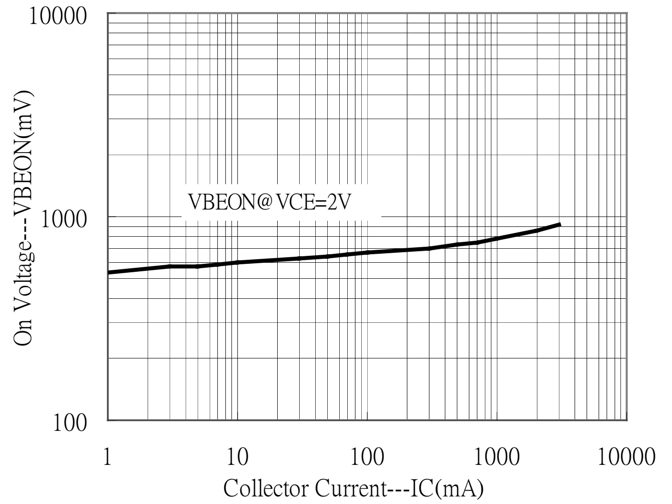


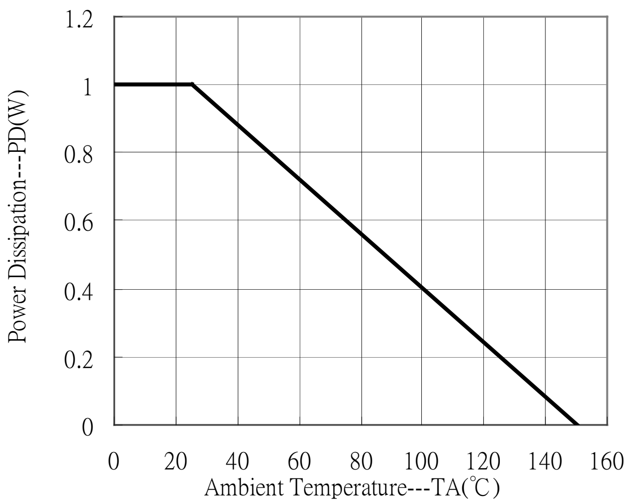
Typical Characteristics

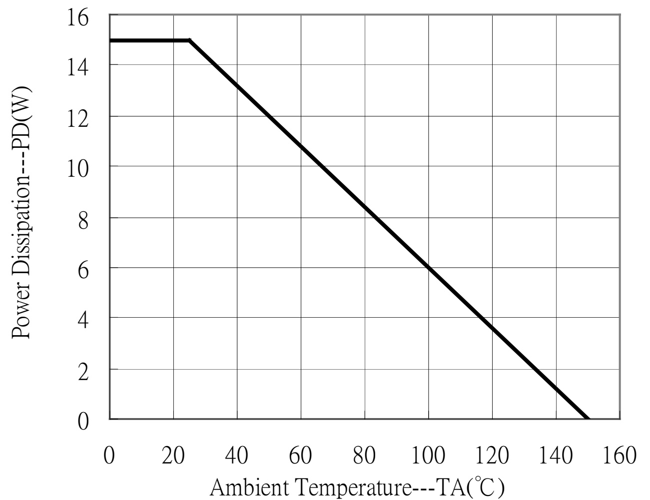












Reel Dimension

Carrier Tape Dimension

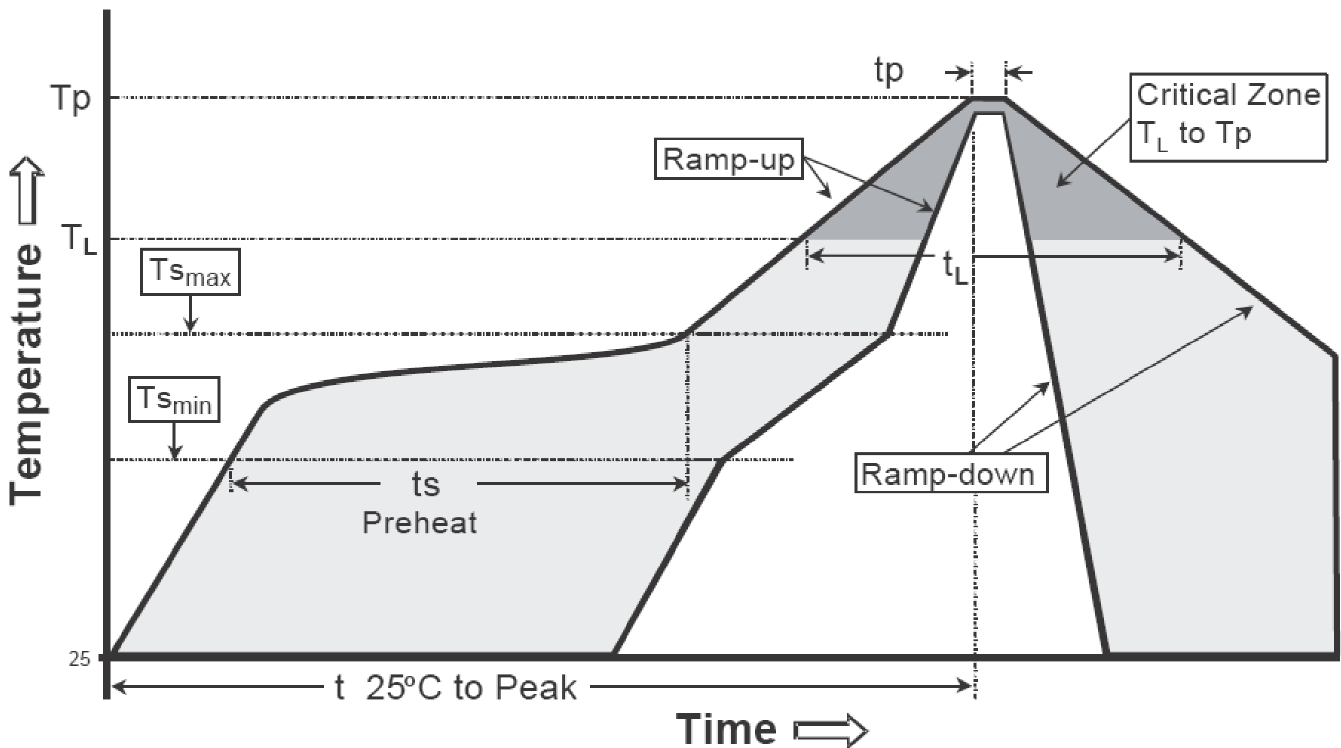
Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material: conductive black polystyrene, antistatic coated : 10^{5} Ω/□~ 10^{11} Ω/□

unit : mm

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

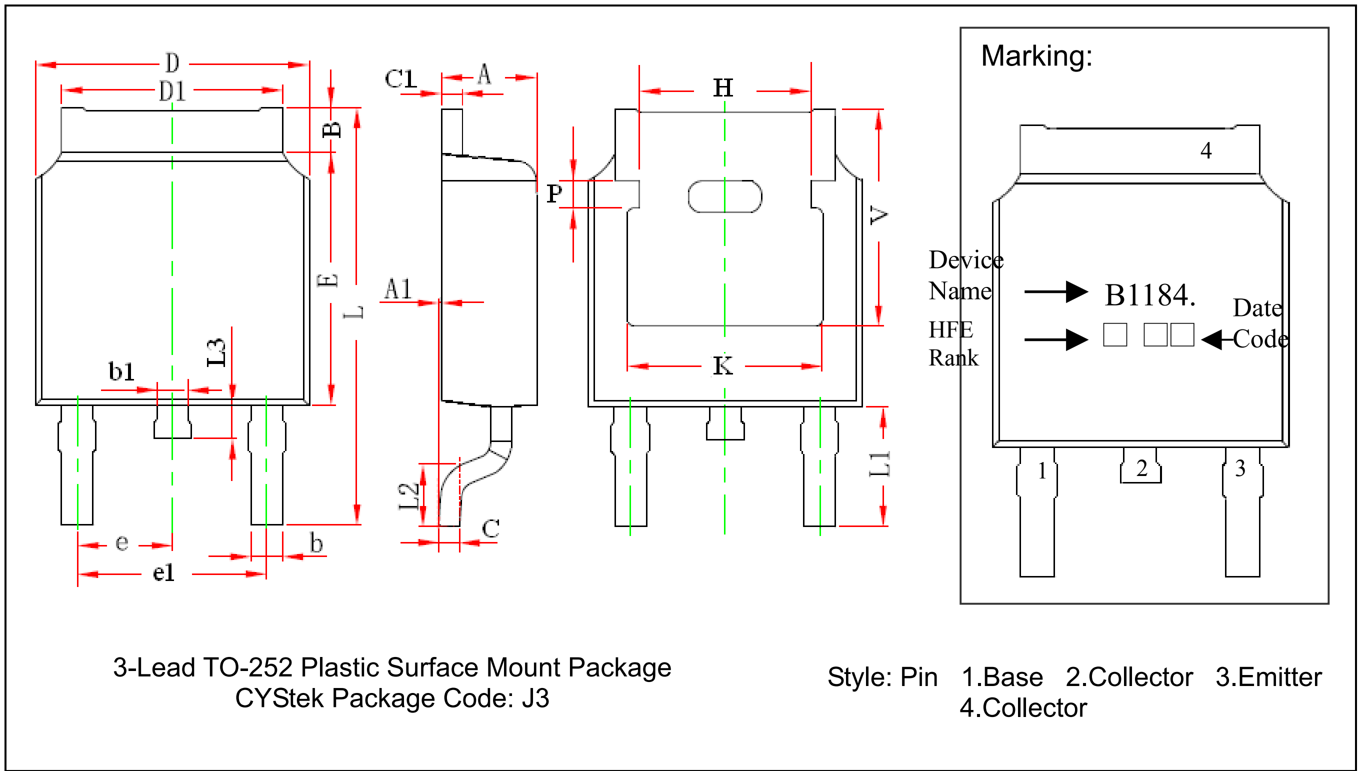
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(Ts min) −Temperature Max(Ts max) −Time(ts min to ts max)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-252 Dimension



3-Lead TO-252 Plastic Surface Mount Package
CYStek Package Code: J3

Style: Pin 1.Base 2.Collector 3.Emitter 4.Collector

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	e	0.086	0.094	2.186	2.386
A1	0.000	0.005	0.000	0.127	e1	0.172	0.188	4.372	4.772
B	0.039	0.048	0.990	1.210	H	0.163	REF	4.140	REF
b	0.026	0.034	0.660	0.860	K	0.190	REF	4.830	REF
b1	0.026	0.034	0.660	0.860	L	0.386	0.409	9.800	10.400
C	0.018	0.023	0.460	0.580	L1	0.114	REF	2.900	REF
C1	0.018	0.023	0.460	0.580	L2	0.055	0.067	1.400	1.700
D	0.256	0.264	6.500	6.700	L3	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	P	0.026	REF	0.650	REF
E	0.236	0.244	6.000	6.200	V	0.211	REF	5.350	REF

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek ***semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.***
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.