

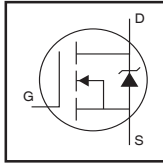
Features

- Advanced Process Technology
- Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

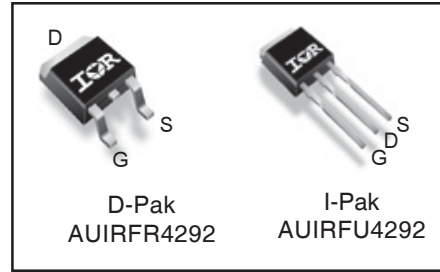
Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

HEXFET® Power MOSFET



V_{(BR)DSS}	250V
R_{DS(on)} typ.	275mΩ
max.	345mΩ
I_D	9.3A



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number	Note
		Form	Quantity		
AUIRFR4292	DPak	Tube	75	AUIRFR4292	
		Tape and Reel	2000	AUIRFR4292TR	
		Tape and Reel Left	3000	AUIRFR4292TRL	
		Tape and Reel Right	3000	AUIRFR4292TRR	EOL notice # 530
AUIRFU4292	IPak	Tube	75	AUIRFU4292	

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	9.3	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	6.6	
I _{DM}	Pulsed Drain Current ①	40	
P _D @ T _C = 25°C	Power Dissipation	100	W
	Linear Derating Factor	0.67	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	130	mJ
E _{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑥	97	
I _{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E _{AR}	Repetitive Avalanche Energy ③		mJ
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ④	—	1.5	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mount) ⑦	—	50	
R _{θJA}	Junction-to-Ambient	—	110	

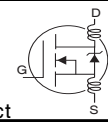
HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

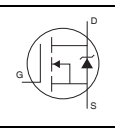
Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.31	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	275	345	mΩ	V _{GS} = 10V, I _D = 5.6A ③
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 50μA
g _{fs}	Forward Transconductance	6.2	—	—	V	V _{DS} = 50V, I _D = 5.6A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 250V, V _{GS} = 0V
		—	—	250		V _{DS} = 250V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V

Dynamic Electrical @ T_J = 25°C (unless otherwise specified)

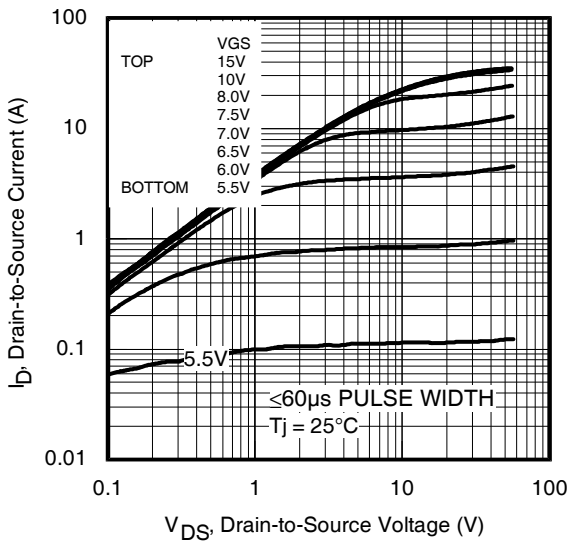
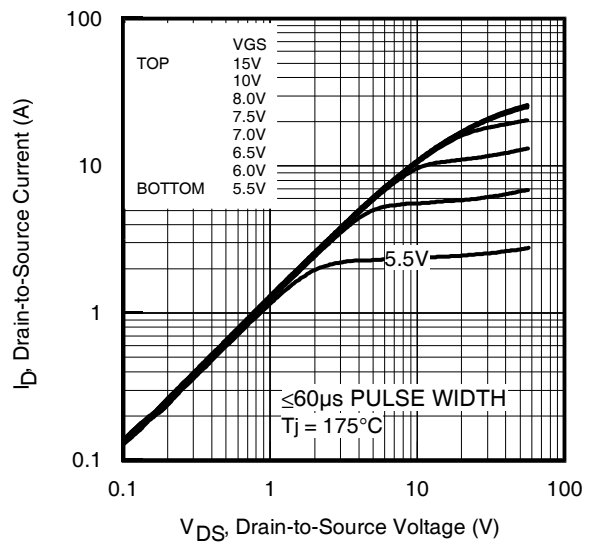
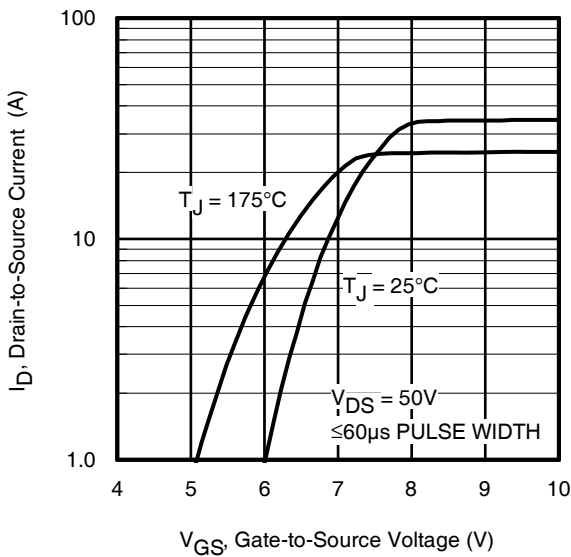
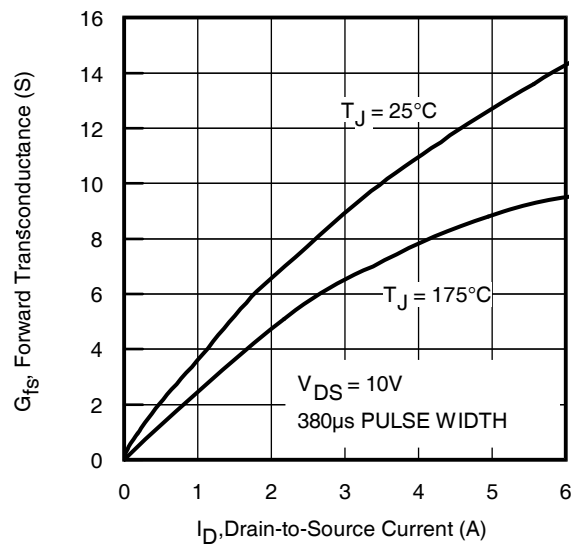
	Parameter	Min.	Typ.	Max.	Units	Conditions
Q _g	Total Gate Charge	—	13	20	nC	I _D = 5.6A
Q _{gs}	Gate-to-Source Charge	—	4.7	—		V _{DS} = 125V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	4.8	—		V _{GS} = 10V ③
t _{d(on)}	Turn-On Delay Time	—	11	—	ns	V _{DD} = 250V
t _r	Rise Time	—	15	—		I _D = 5.6A
t _{d(off)}	Turn-Off Delay Time	—	16	—		R _G = 15Ω
t _f	Fall Time	—	8.4	—		V _{GS} = 10V ③
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	705	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	71	—		V _{DS} = 25V
C _{iss}	Reverse Transfer Capacitance	—	20	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	600	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	26	—		V _{GS} = 0V, V _{DS} = 200V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	65	—		V _{GS} = 0V, V _{DS} = 0V to 200V ④

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	9.3	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	40		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 5.6A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	110	165	ns	T _J = 25°C, I _F = 5.6A, V _{DD} = 125V
Q _{rr}	Reverse Recovery Charge	—	390	585	nC	di/dt = 100A/μs ③
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 8.1mH, R_G = 50Ω, I_{AS} = 5.6A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ④ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑤ Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value is determined from sample failure population, starting T_J = 25°C, L = 8.1mH, R_G = 50Ω, I_{AS} = 5.6A, V_{GS} = 10V.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J approximately 90°C.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Typical Forward Transconductance vs. Drain Current

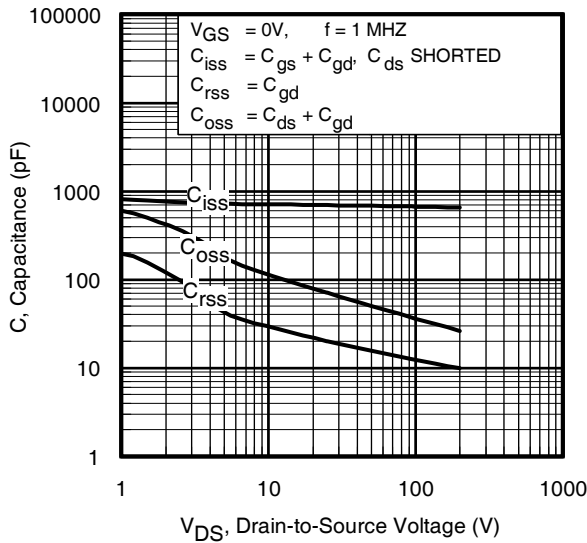


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

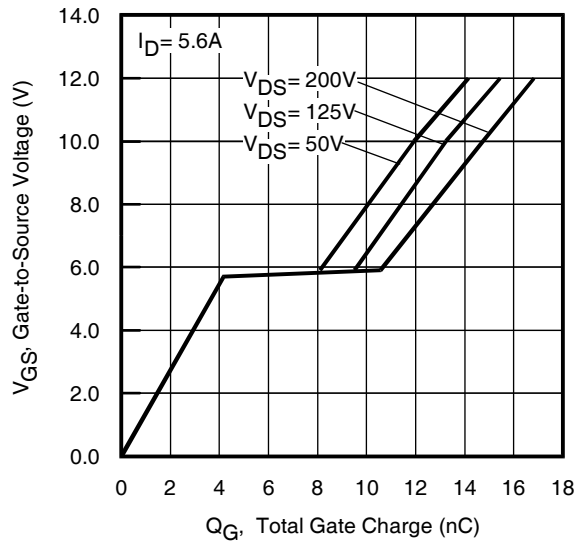


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

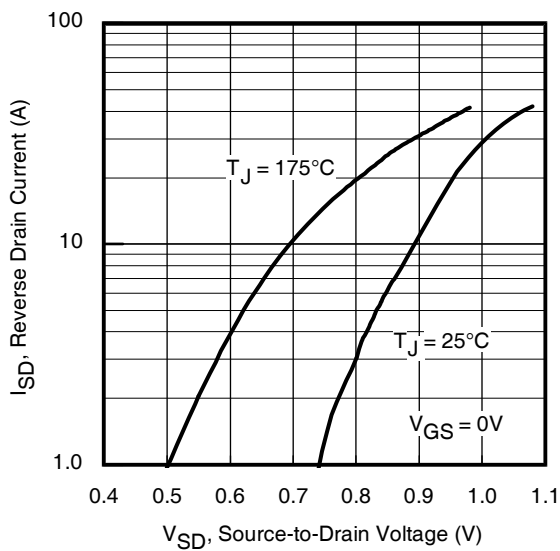


Fig 7. Typical Source-Drain Diode Forward Voltage

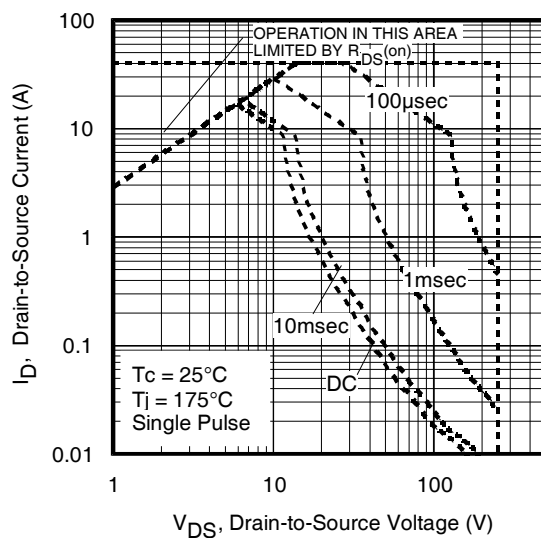


Fig 8. Maximum Safe Operating Area

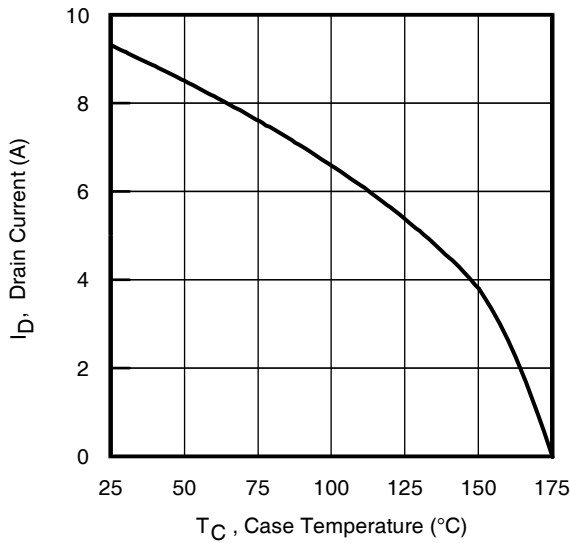


Fig 9. Maximum Drain Current vs. Case Temperature

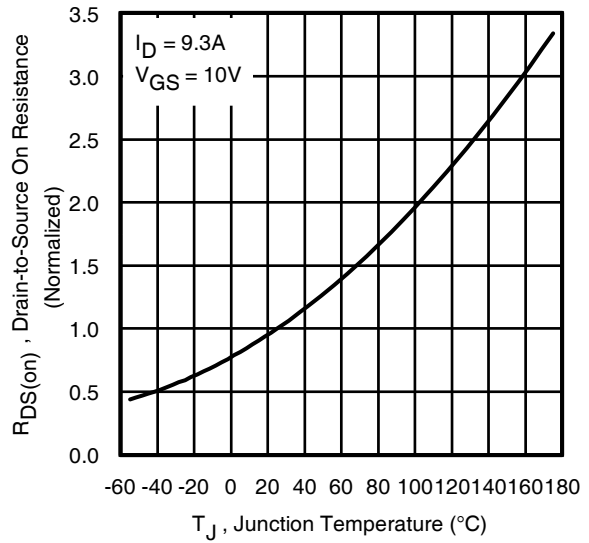


Fig 10. Normalized On-Resistance vs. Temperature

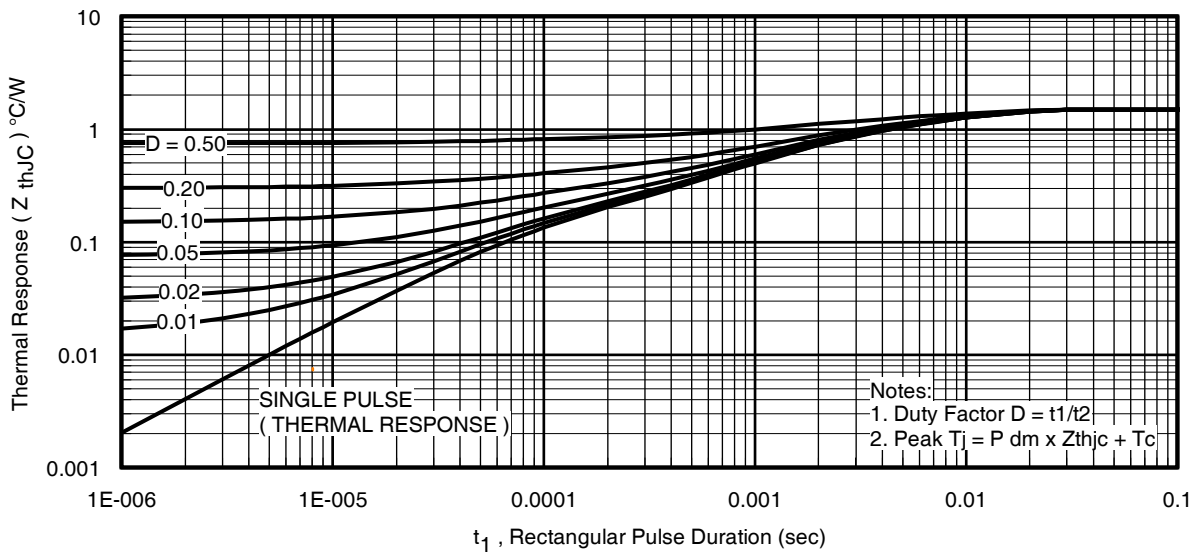
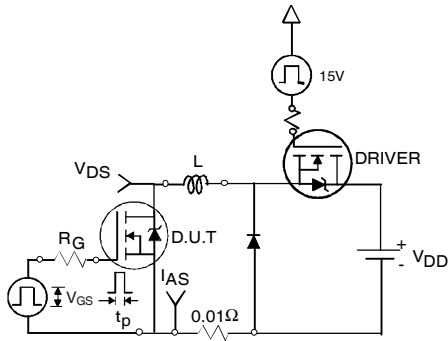
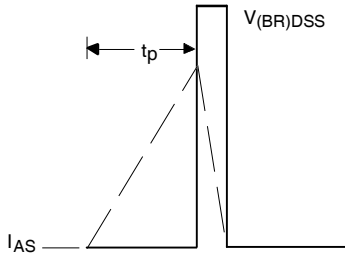
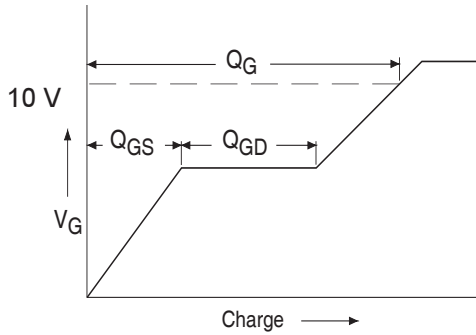
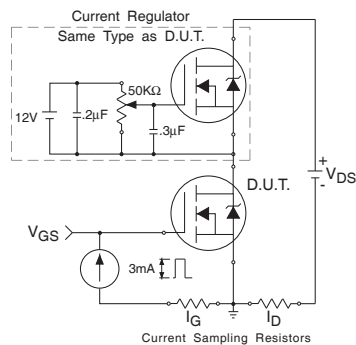
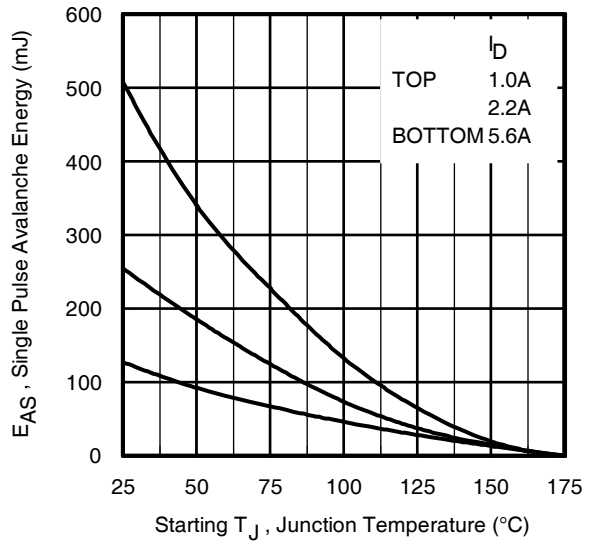
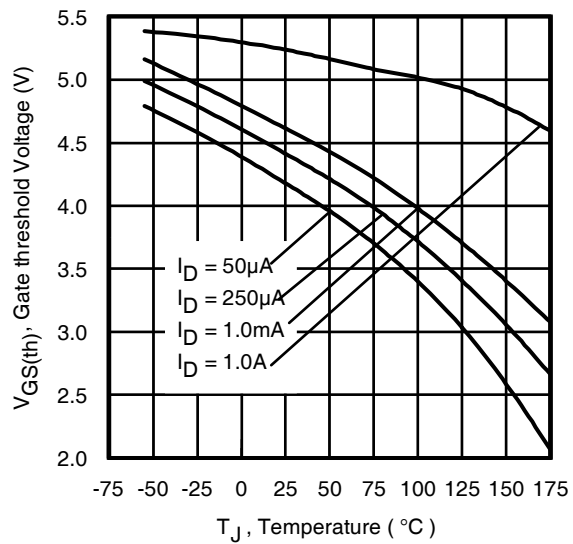
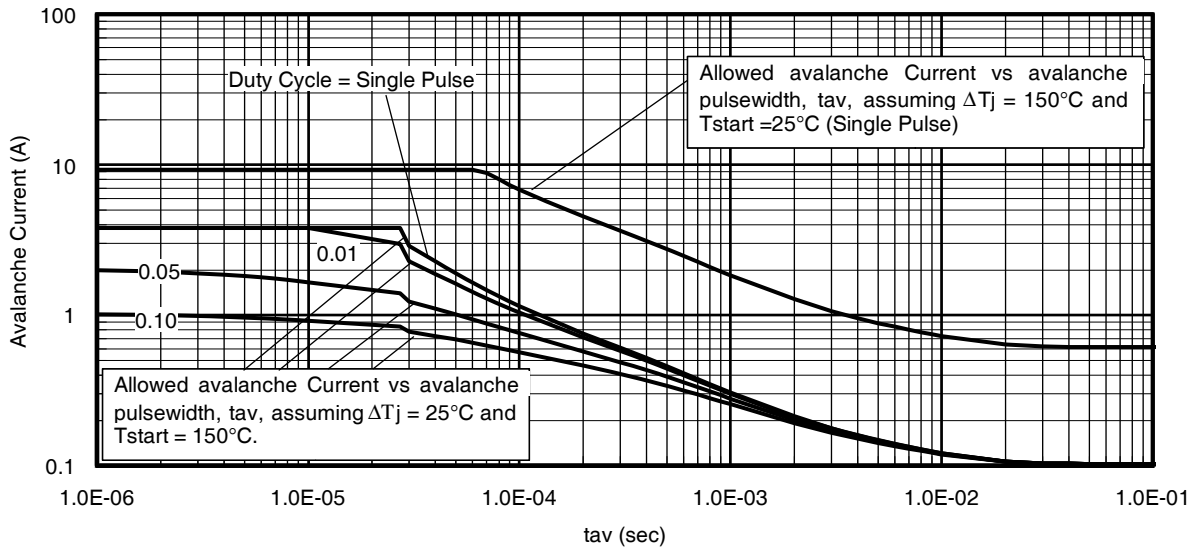
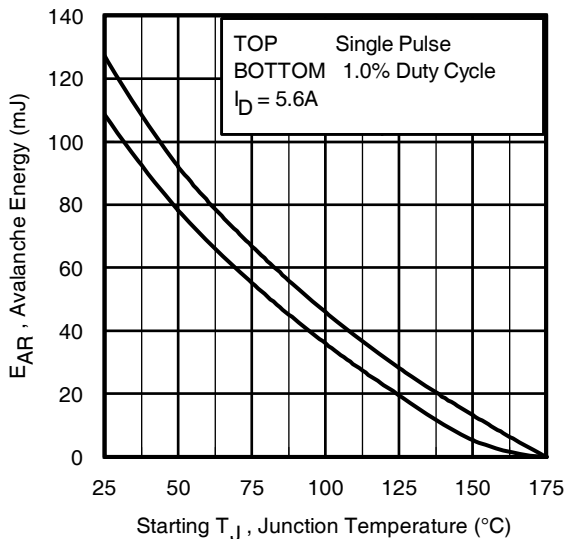


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 14. Threshold Voltage vs. Temperature


Fig 15. Typical Avalanche Current vs. Pulsewidth

Fig 16. Maximum Avalanche Energy vs. Temperature
**Notes on Repetitive Avalanche Curves, Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

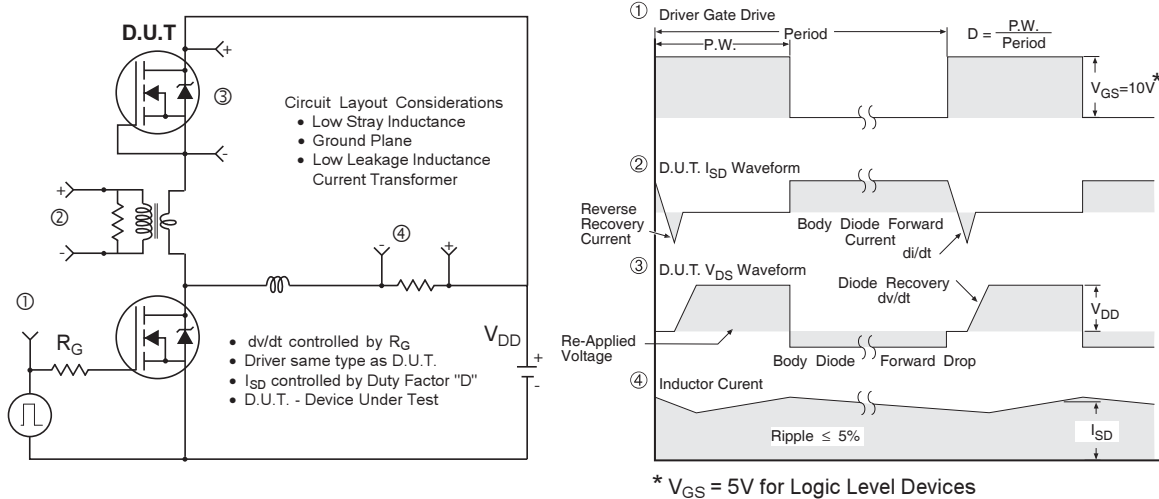


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

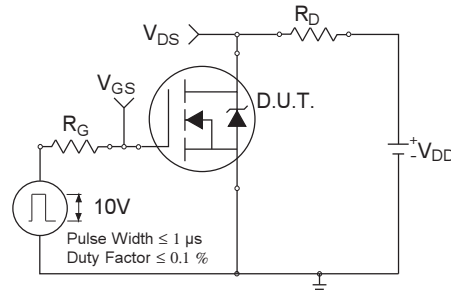


Fig 18a. Switching Time Test Circuit

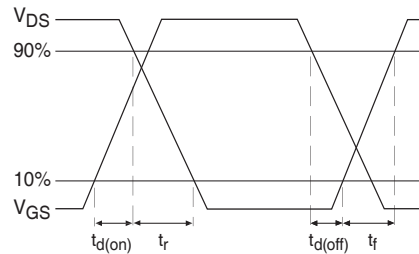
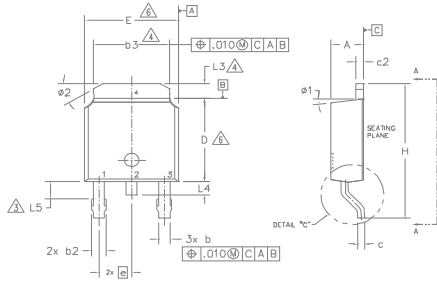


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
phi	0"	10"	0"	10"	
phi1	0"	15"	0"	15"	
phi2	25"	35"	25"	35"	

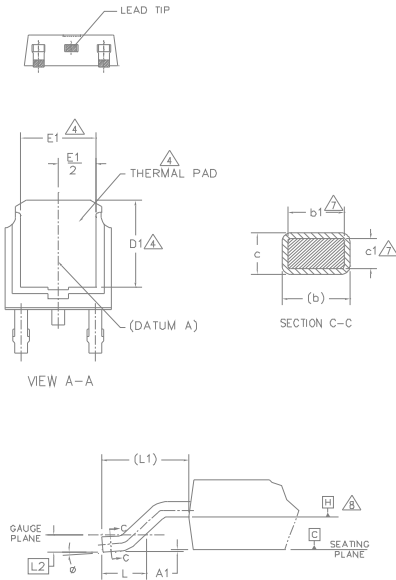
LEAD ASSIGNMENTS

HEXFET

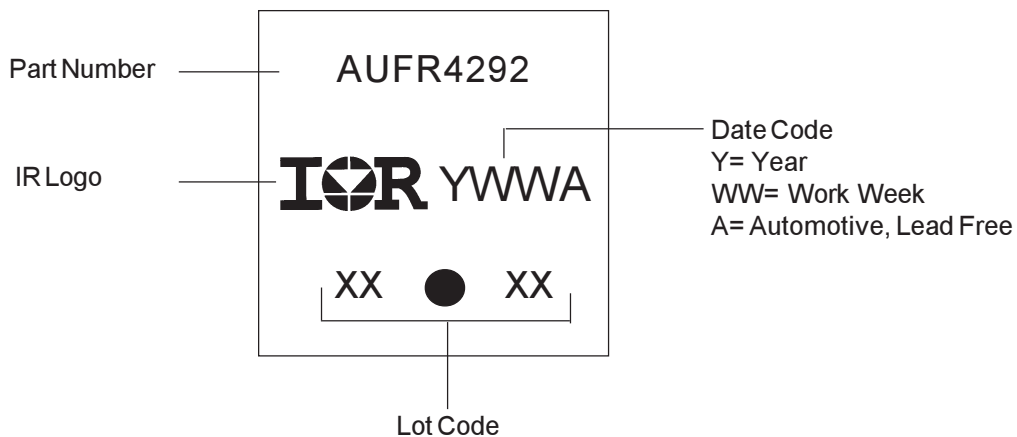
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR



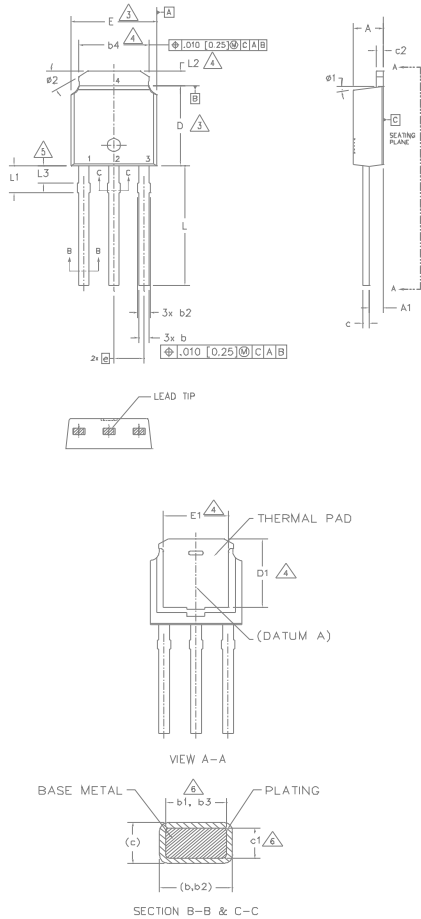
D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



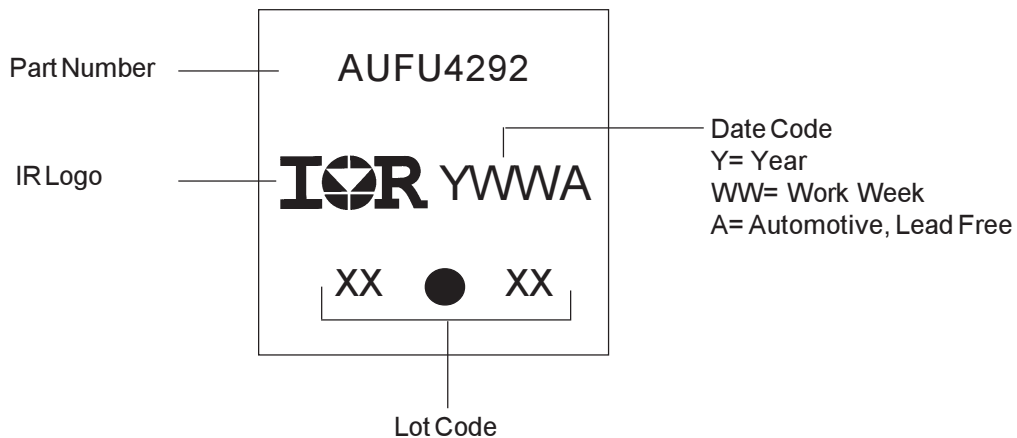
- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 - 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
 5. LEAD DIMENSION UNCONTROLLED IN L3.
 6. DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
 - 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
 - 8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	0.89	1.52	.035	.060	5
phi1	0'	15'	0'	15'	
phi2	25'	35'	25'	35'	

LEAD ASSIGNMENTS

- HEXFET**
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
 - 4.- DRAIN

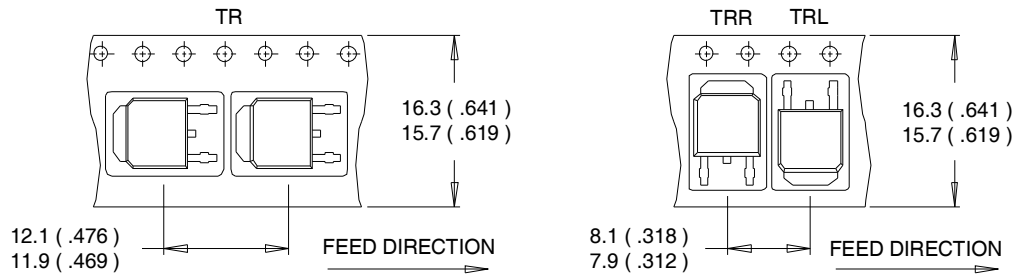
I-Pak (TO-251AA) Part Marking Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

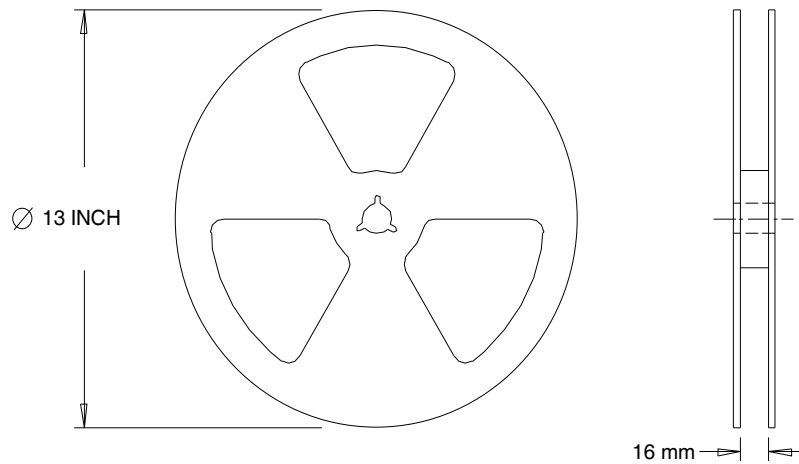
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D-PAK	MSL1
		I-PAK	
ESD	Machine Model	Class M1B (+/- 100) ^{††} AEC-Q101-002	
	Human Body Model	Class H1A (+/- 500) ^{††} AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000) ^{††} AEC-Q101-005	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

†† Highest passing voltage.

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IR warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with IR's standard warranty. Testing and other quality control techniques are used to the extent IR deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

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Revision History

Date	Comments
9/2/2014	<ul style="list-style-type: none"> • Updated datasheet with IR corporate template. • Updated SOA curve Fig 8 from "50V" VDS to "250V" on page 4. • Updated Package outline on page 9 & 10 • Updated ordering information to reflect the End-Of-life (EOL) of the option (EOL notice #530)