

DATA SHEET

BF901; BF901R Silicon n-channel dual gate MOS-FETs

Product specification
File under Discrete Semiconductors, SC07

November 1992

Silicon n-channel dual gate MOS-FETs

BF901; BF901R

FEATURES

- Intended for low voltage operation
- Short channel transistor with high ratio $|Y_{fs}| : C_{is}$
- Low noise gain-controlled amplifier to 1 GHz
- BF901R has reverse pinning.

DESCRIPTION

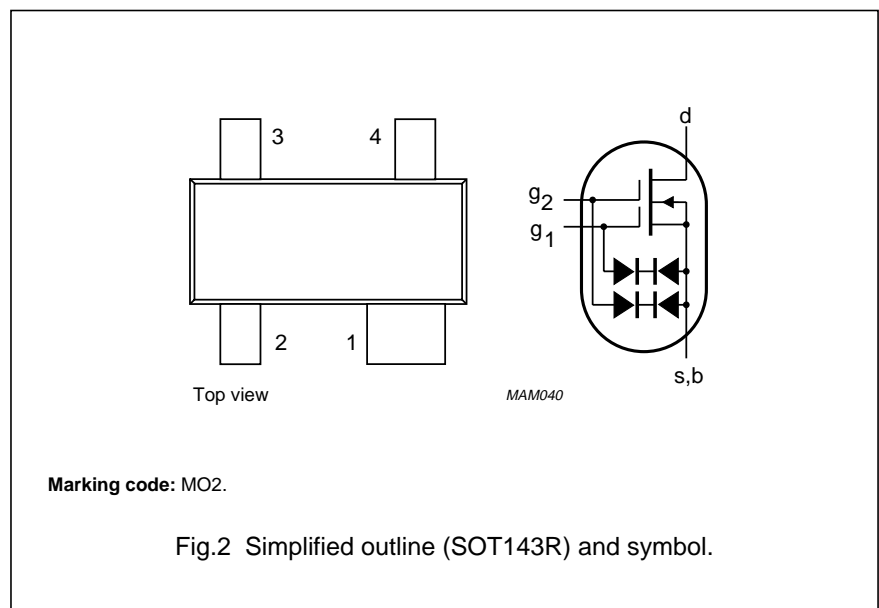
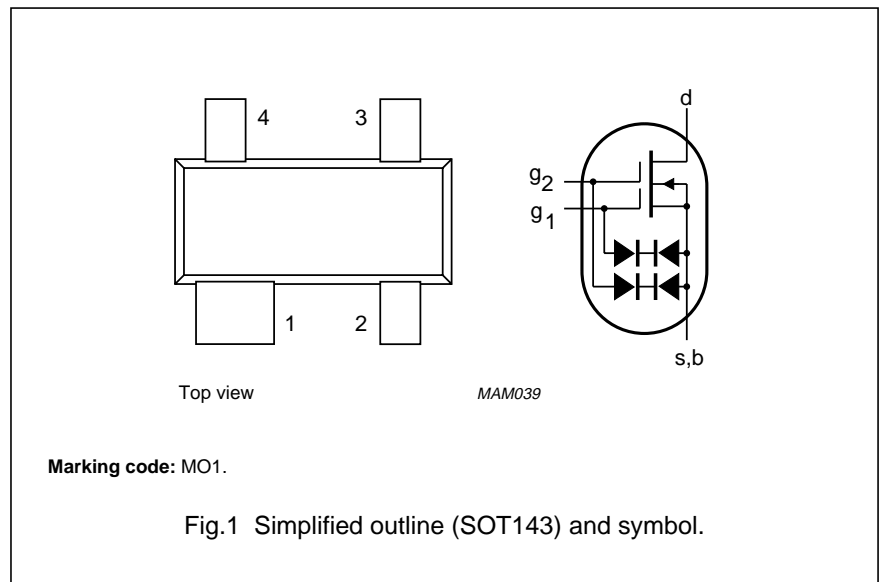
Enhancement type field-effect transistors in plastic microminiature SOT143 and SOT143R envelopes, with source and substrate interconnected. They are intended for UHF and VHF applications, such as television tuners and professional communications equipment especially suited for low voltage operation. These MOS-FET tetrodes are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	–	12	V
I_D	drain current	–	30	mA
P_{tot}	total power dissipation	–	200	mW
T_j	junction temperature	–	150	°C
$ Y_{fs} $	transfer admittance	28	35	mS
C_{ig1-s}	input capacitance at gate 1	2.35	2.75	pF
C_{rs}	feedback capacitance	25	–	fF
F	noise figure at 800 MHz	1.7	–	dB



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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
V_{D-G2}	drain-gate 2 voltage		–	6	V
I_D	DC drain current		–	30	mA
$\pm I_{G1-S}$	gate 1-source current		–	10	mA
$\pm I_{G2-S}$	gate 2-source current		–	10	mA
P_{tot}	total power dissipation BF901 BF901R	up to $T_{amb} = 50\text{ }^\circ\text{C}$ (note 1) up to $T_{amb} = 40\text{ }^\circ\text{C}$ (note 1)	–	200 200	mW mW
T_{stg}	storage temperature		–65	150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	thermal resistance from junction to ambient (note 1) BF901 BF901R	500 K/W 550 K/W

Note

1. Device mounted on an FR4 printboard.

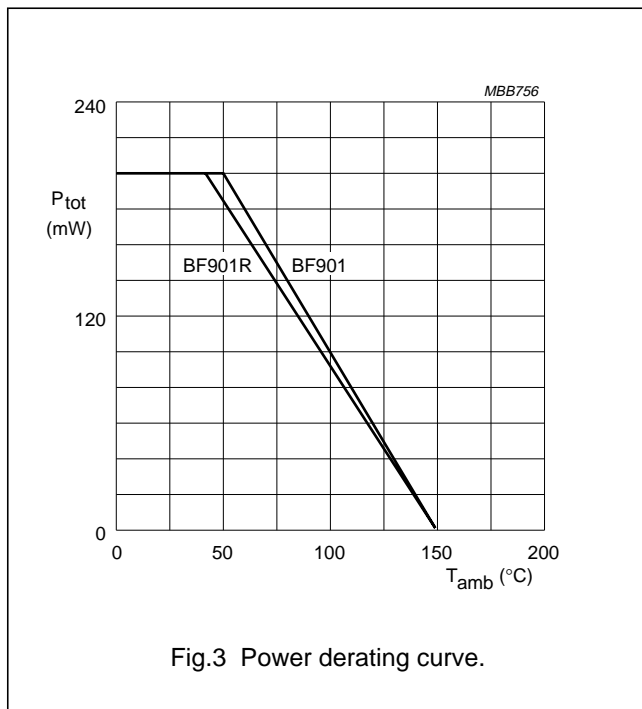


Fig.3 Power derating curve.

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STATIC CHARACTERISTICS $T_j = 25\text{ }^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1-SS}$	gate 1 cut-off current	$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$	–	50	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$	–	50	nA
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	6	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	6	20	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$I_D = 20\text{ }\mu\text{A}; V_{DS} = 8\text{ V}; V_{G2-S} = 4\text{ V}$	0	0.7	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$I_D = 20\text{ }\mu\text{A}; V_{DS} = 8\text{ V}; V_{G1-S} = 0$	0.3	1	V
I_{DSX}	drain-source current	$V_{DS} = 4\text{ V}; V_{G1-S} = 1.1\text{ V}; V_{G2-S} = 3.4\text{ V}$	2	18	mA

DYNAMIC CHARACTERISTICSMeasuring conditions (common source): $I_D = 14\text{ mA}; V_{DS} = 5\text{ V}; V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ Y_{fs} $	transfer admittance	pulsed; $T_j = 25\text{ }^\circ\text{C}$	25	28	35	mS
C_{ig1-s}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	2.35	2.75	pF
C_{ig2-s}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	1.2	–	pF
C_{os}	output capacitance	$f = 1\text{ MHz}$	–	1.4	–	pF
C_{rs}	feedback capacitance	$f = 1\text{ MHz}$	–	25	–	fF
F	noise figure	$f = 200\text{ MHz}; G_s = 2\text{ mS}; B_s = B_{s\text{opt}}$	–	0.7	–	dB
		$f = 800\text{ MHz}; G_s = 3.3\text{ mS}; B_s = B_{s\text{opt}}$	–	1.7	–	dB

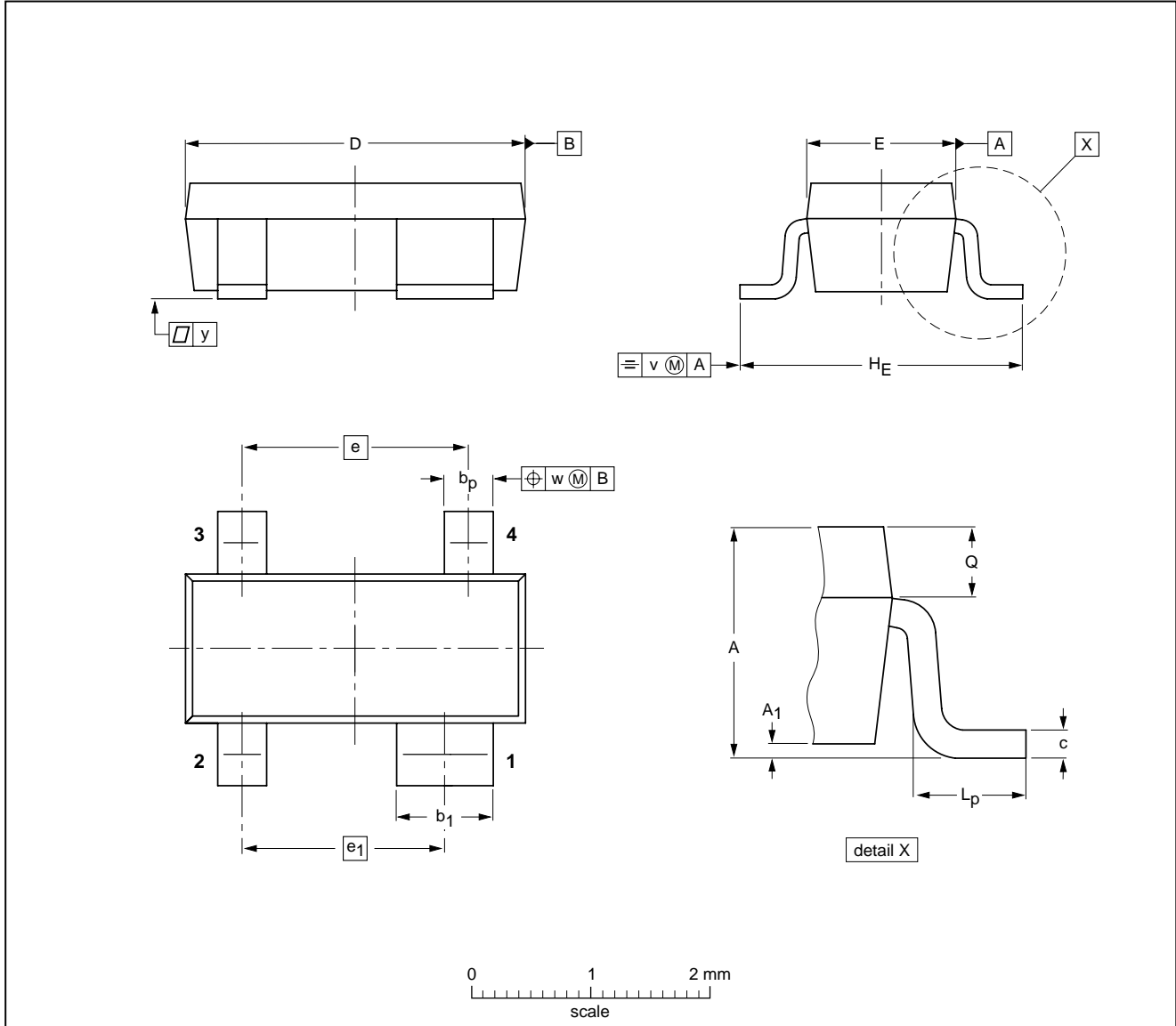
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PACKAGE OUTLINE

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

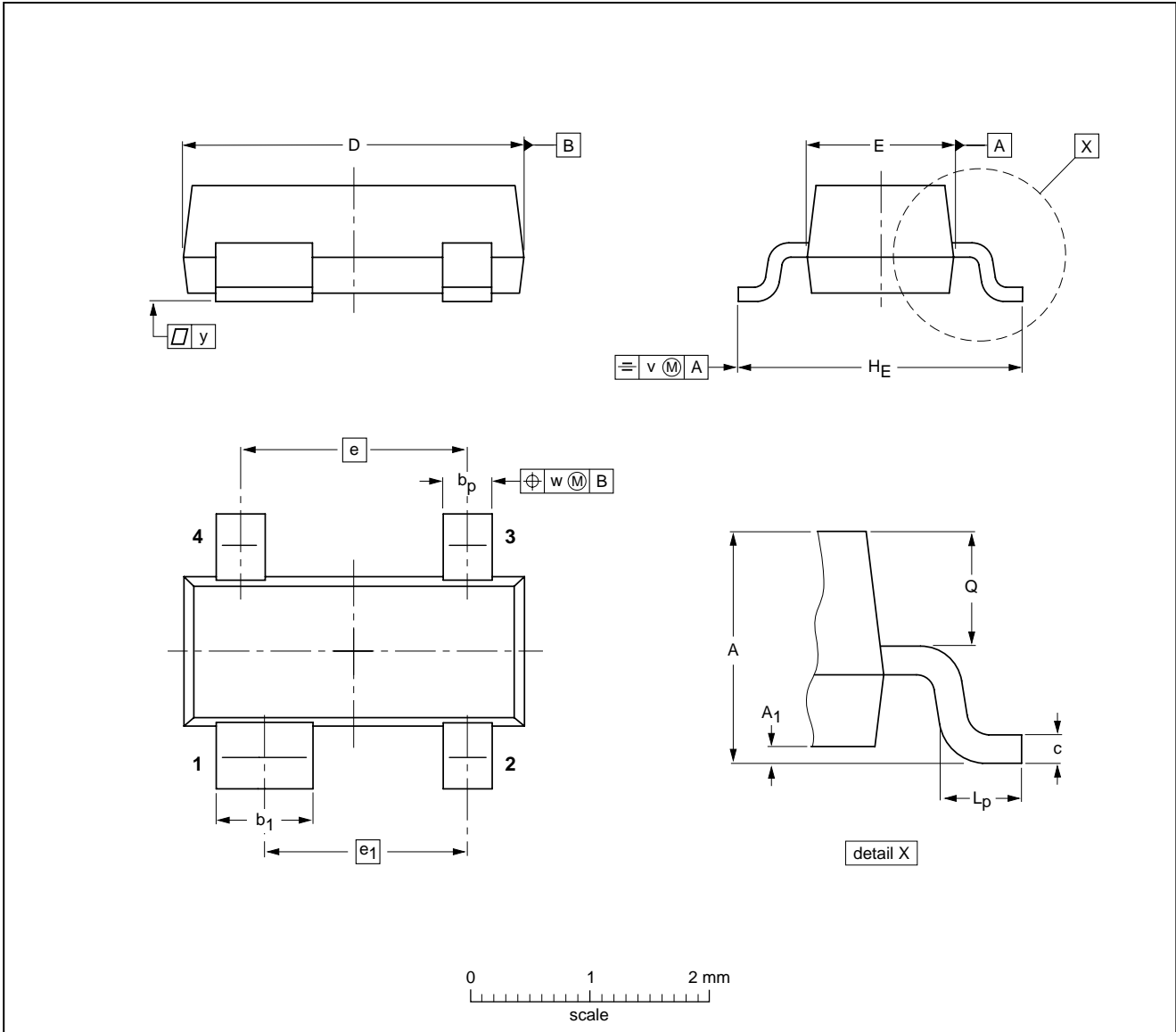
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143R						97-03-10

Silicon n-channel dual gate MOS-FETs

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Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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