

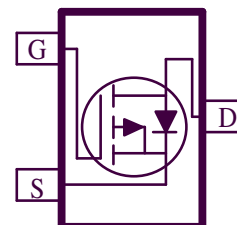
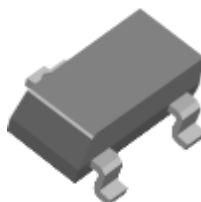
P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology



RoHS
COMPLIANT
HALOGEN
FREE



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
-20	0.100 @ $V_{GS} = -4.5V$	-2.9
	0.160 @ $V_{GS} = -2.5V$	-2.3
	0.290 @ $V_{GS} = -1.8V$	-1.7

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ^a	I_D	$T_A=25^\circ C$	-2.9
		$T_A=70^\circ C$	-2.4
Pulsed Drain Current ^b	I_{DM}	-10	A
Continuous Source Current (Diode Conduction) ^a	I_S	± 1.6	A
Power Dissipation ^a	P_D	$T_A=25^\circ C$	1.25
		$T_A=70^\circ C$	0.8
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	R_{THJA}	t <= 5 sec	100
		Steady-State	166

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25 ^o C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 uA	-0.4			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +/-12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	uA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55 ^o C			-10	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-3			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -2.9 A			0.100	Ω
		V _{GS} = -2.5 V, I _D = -2.3 A			0.160	
		V _{GS} = -1.8 V, I _D = -1.7 A			0.290	
Forward Transconductance ^A	g _{fs}	V _{DS} = -5 V, I _D = -2.8 A		3		S
Diode Forward Voltage	V _{SD}	I _S = -1.6 A, V _{GS} = 0 V		-0.7		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -5 V, V _{GS} = -4.5 V, I _D = -2.6 A		6		nC
Gate-Source Charge	Q _{gs}			0.3		
Gate-Drain Charge	Q _{gd}			1.3		
Input Capacitance	C _{iss}	P-Channel V _{DS} =-15V, V _{GS} =0V, f=1MHz		395		pF
Output Capacitance	C _{oss}			130		
Reverse Transfer Capacitance	C _{rss}			33		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -5 V, R _L = 5 OHM, V _{GEN} = -4.5 V, R _G = 6 OHM		6.5		ns
Rise Time	t _r			3		
Turn-Off Delay Time	t _{d(off)}			31		
Fall-Time	t _f			4		

Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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Typical Electrical Characteristics

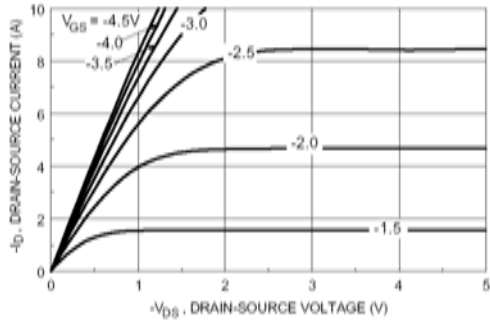


Figure 1. On-Region Characteristics.

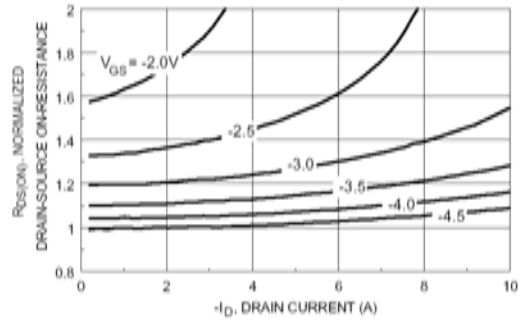


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

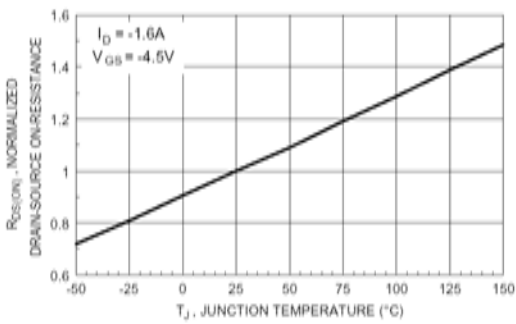


Figure 3. On-Resistance Variation with Temperature.

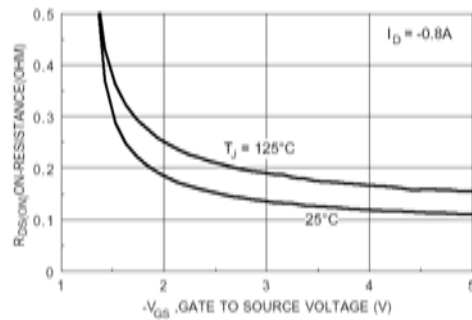


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

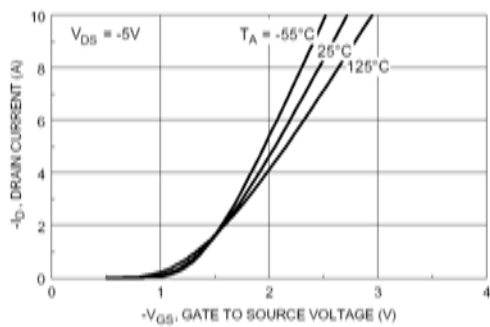


Figure 5. Transfer Characteristics.

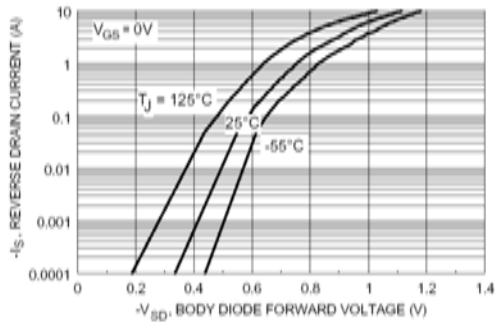


Figure 6 . Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics

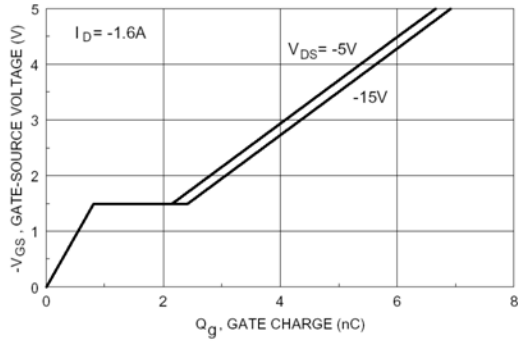


Figure 7. Gate Charge Characteristics.

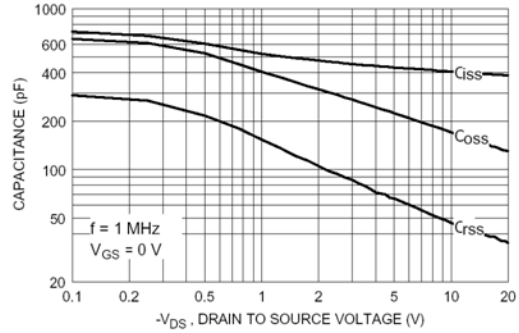


Figure 8. Capacitance Characteristics.

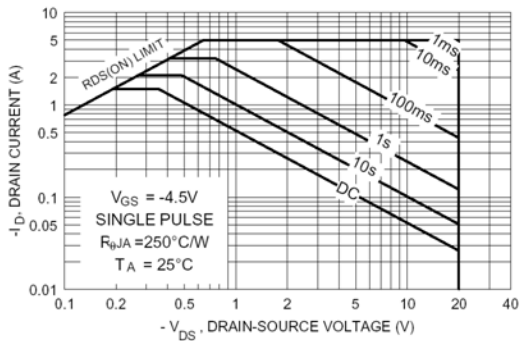


Figure 9. Maximum Safe Operating Area.

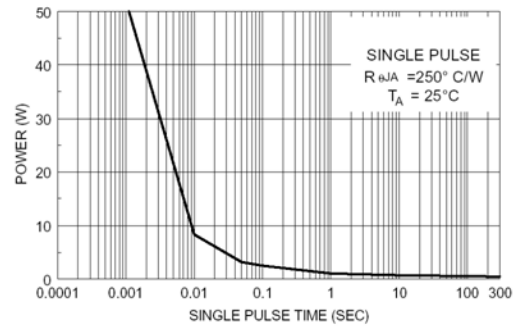


Figure 10. Single Pulse Maximum Power Dissipation.

Normalized Thermal Transient Junction to Ambient

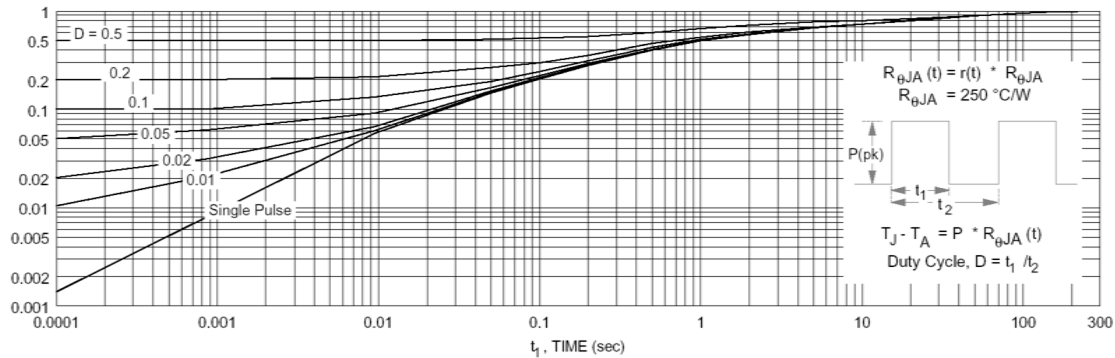
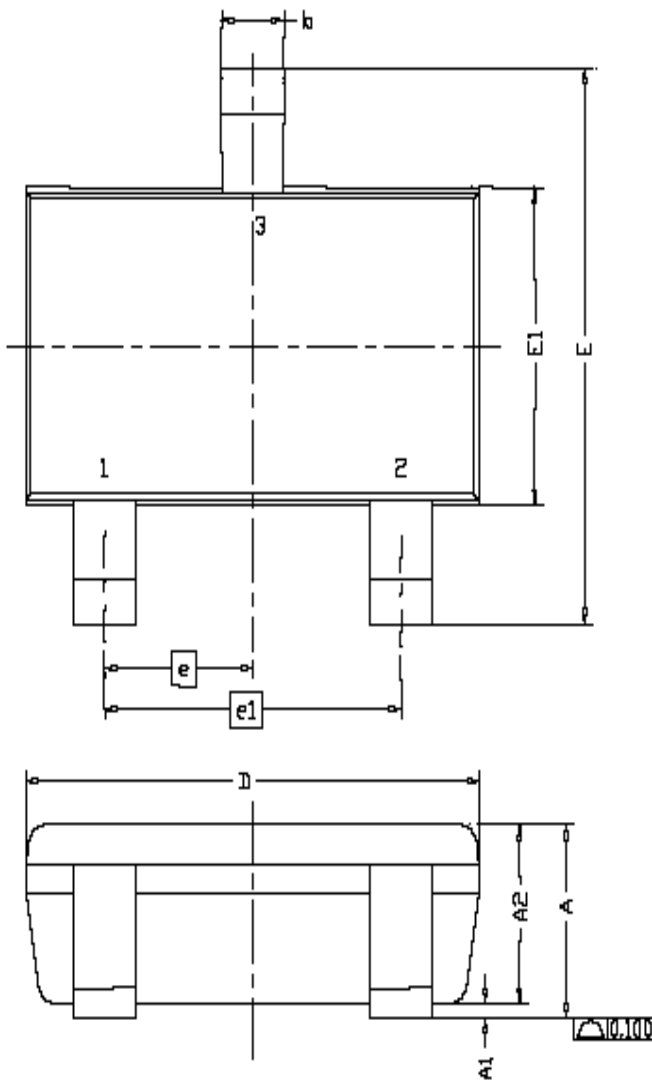


Figure 11. Transient Thermal Response Curve.

Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
$\theta1$	7°NOM		

