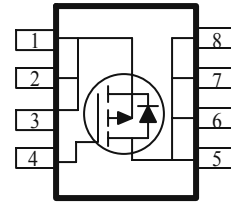


P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-20	20 @ $V_{GS} = -4.5V$	10.2
	29 @ $V_{GS} = -2.5V$	8.5
	54 @ $V_{GS} = -1.8V$	6.2



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ^a	I_D	$T_A = 25^\circ C$	10.2
		$T_A = 70^\circ C$	8.2
Pulsed Drain Current ^b	I_{DM}	± 30	A
Continuous Source Current (Diode Conduction) ^a	I_S	-2.3	A
Power Dissipation ^a	P_D	$T_A = 25^\circ C$	3.1
		$T_A = 70^\circ C$	2
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	t \leq 10 sec	50
		Steady State	92

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -350 uA	-0.7			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	uA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55°C			-10	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-20			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -10.2 A			20	mΩ
		V _{GS} = -2.5 V, I _D = -8.5 A			29	
		V _{GS} = -1.8 V, I _D = -6.2 A			54	
Forward Transconductance ^A	g _{fs}	V _{DS} = -10 V, I _D = -10.2 A		36		S
Diode Forward Voltage	V _{SD}	I _S = -2.3 A, V _{GS} = 0 V		-0.8		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -5 V, I _D = -10.2 A		30		nC
Gate-Source Charge	Q _{gs}			4		
Gate-Drain Charge	Q _{gd}			6		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 15 Ω, I _D = -1 A, V _{GEN} = -5 V, R _G = 6Ω		25		nS
Rise Time	t _r			45		
Turn-Off Delay Time	t _{d(off)}			150		
Fall-Time	t _f			70		

Notes

- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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Typical Electrical Characteristics

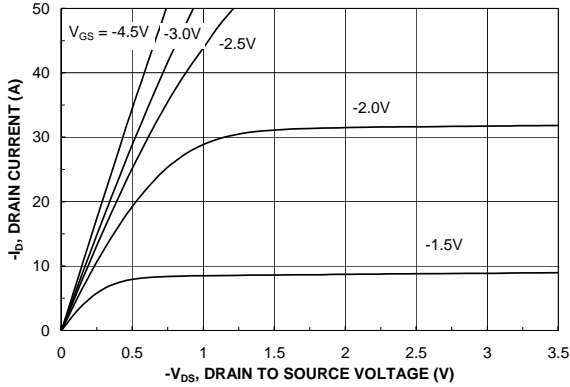


Figure 1. Output Characteristics

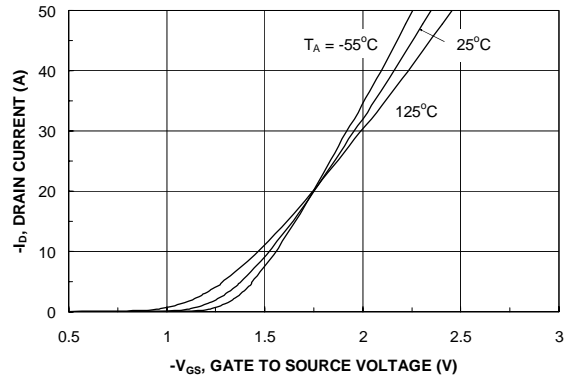


Figure 2. Transfer Characteristics

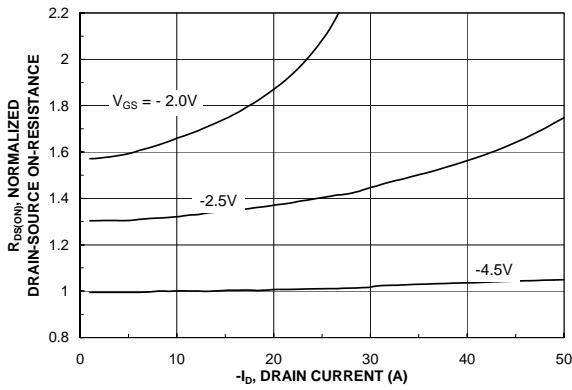


Figure 3. On Resistance vs. Drain Current

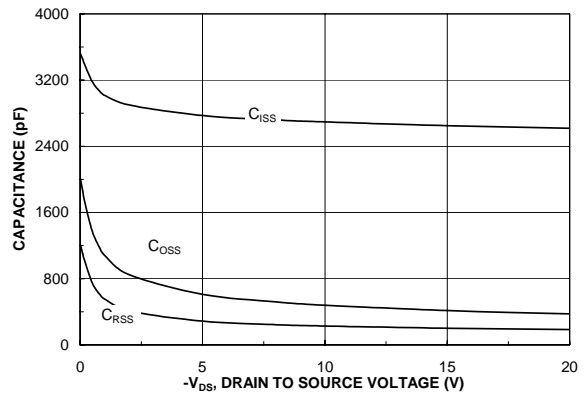


Figure 4. Capacitance

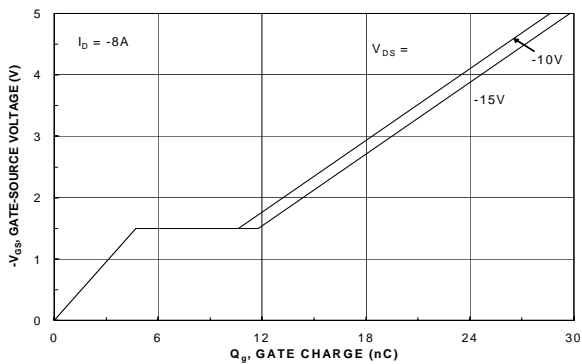


Figure 5. Gate Charge

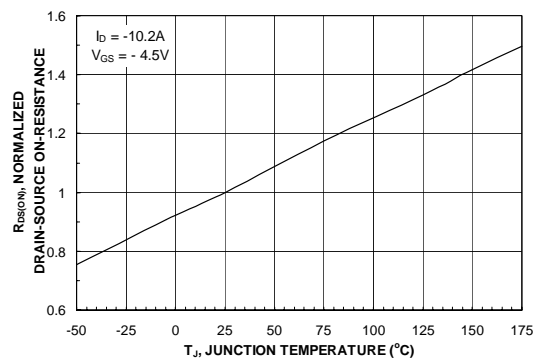


Figure 6. On-Resistance vs. Junction Temperature

Typical Electrical Characteristics

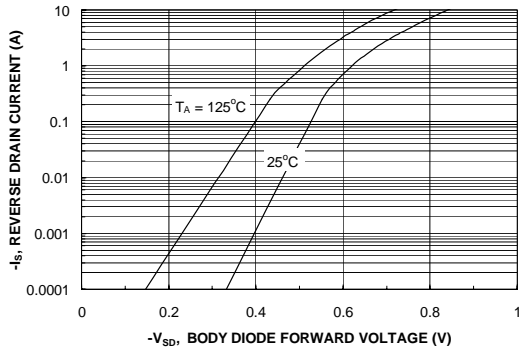


Figure 7. Source-Drain Diode Forward Voltage

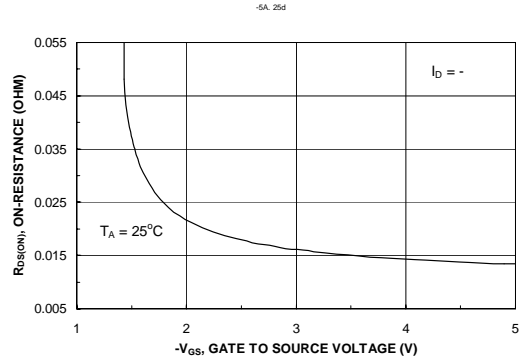


Figure 8. On-Resistance vs. Gate-to-Source Voltage

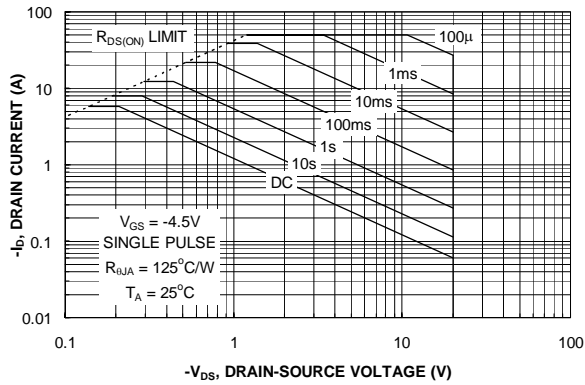


Figure 9. Safe Operating Area

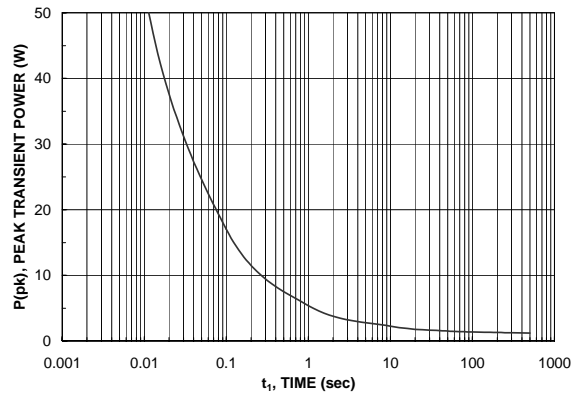


Figure 10. Single Pulse Power, Junction-to-Ambient

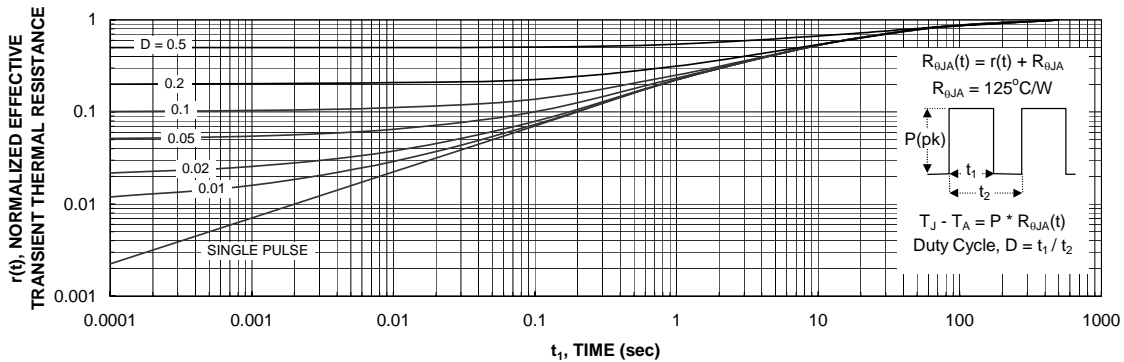
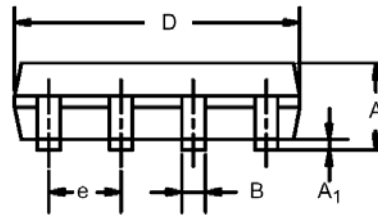
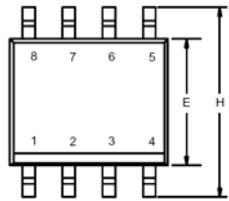


Figure 11. Normalized Thermal Transient Impedance, Junction-to-Ambient

Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

