

P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-30	9 @ $V_{GS} = -10V$	-15
	13 @ $V_{GS} = -4.5V$	-11

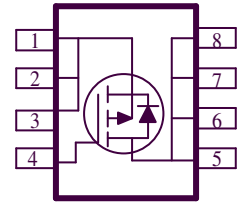
- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology



RoHS
COMPLIANT
HALOGEN
FREE
Available



Protected



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	$T_A=25^\circ C$	-15
		$T_A=70^\circ C$	-11
Pulsed Drain Current ^b	I_{DM}	± 50	A
Continuous Source Current (Diode Conduction) ^a	I_S	-2.1	A
Power Dissipation ^a	P_D	$T_A=25^\circ C$	3.1
		$T_A=70^\circ C$	2.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Case ^a	$R_{\theta JC}$	25	$^\circ C/W$
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±10	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -24 V, V _{GS} = 0 V, T _J = 55°C			-5	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-50			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -10 V, I _D = -1 A			9	mΩ
		V _{GS} = -4.5 V, I _D = -1 A			13	
Forward Transconductance ^A	g _{fs}	V _{DS} = -5 V, I _D = -1 A		44		S
Diode Forward Voltage	V _{SD}	I _S = 1 A, V _{GS} = 0 V		-0.7		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -4.5 V, I _D = -1 A		50		nC
Gate-Source Charge	Q _{gs}			10		
Gate-Drain Charge	Q _{gd}			20		
Switching						
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 6 Ω, I _D = -1 A, V _{GEN} = -10 V		10		nS
Rise Time	t _r			30		
Turn-Off Delay Time	t _{d(off)}			100		
Fall-Time	t _f			50		

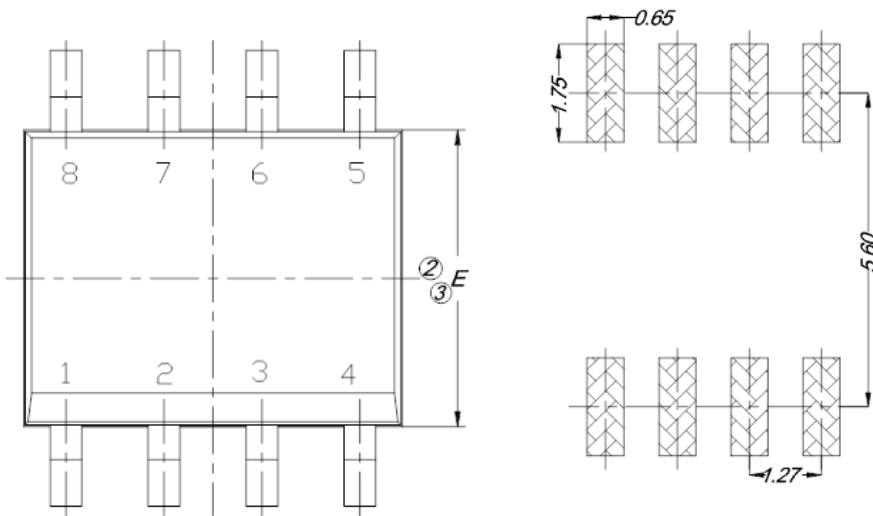
Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

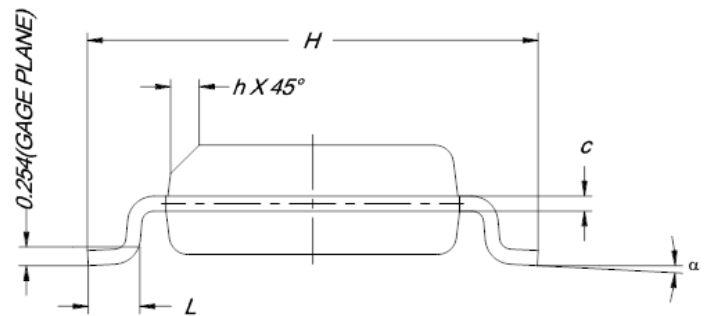
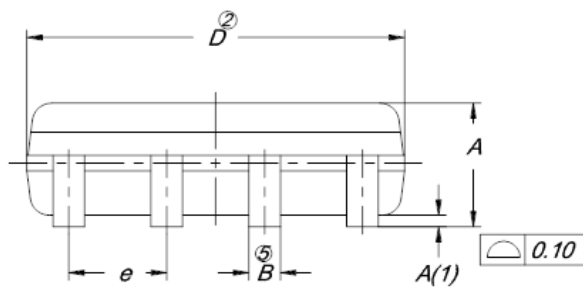
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Package Information

Land Pattern
(Only for Reference)



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A(1)	0.10	0.18	0.25
B	0.38	0.45	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
H	5.80	6.00	6.20
L	0.50	0.72	0.93
α	0°	4°	8°
h	0.25	0.38	0.50



Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.
5. Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.