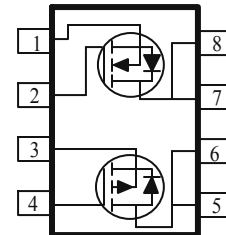
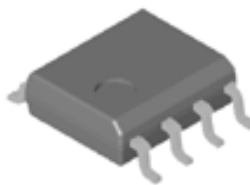


P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	28 @ $V_{GS} = 4.5V$	7.2
	18 @ $V_{GS} = 10V$	8.5
-20	250 @ $V_{GS} = -2.5V$	-2.6
	170 @ $V_{GS} = -4.5V$	-3.2



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	N-Channel	P-Channel	Units	
Drain-Source Voltage	V_{DS}	30	-20	V	
Gate-Source Voltage	V_{GS}	20	-12		
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	10	-3.5	A
	$T_A = 70^\circ C$		7	-2.3	
Pulsed Drain Current ^b	I_{DM}	± 50	± 50		
Continuous Source Current (Diode Conduction) ^a	I_S	2.3	-2.1	A	
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	2.1	2.1	W
	$T_A = 70^\circ C$		1.3	1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}		-55 to 150	$^\circ C$	

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Case ^a	$t \leq 5$ sec	$R_{\theta JC}$	40	$^\circ C/W$
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	$R_{\theta JA}$	60	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	1			V
		V _{GS} = -12 V, V _{DS} = 0 V	P	-0.7			
Gate-Body Leakage	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V	N			±100	nA
		V _{GS} = -12 V, V _{DS} = 0 V	P			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V	P			-1	uA
		V _{DS} = 24 V, V _{GS} = 0 V	N			1	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N	30			A
		V _{DS} = -5 V, V _{GS} = -10 V	P	-10			
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 8.5 A	N			18	mΩ
		V _{GS} = 4.5 V, I _D = 7.2 A				28	
		V _{GS} = -4.5 V, I _D = -3.2 A	P			170	
		V _{GS} = -2.5 V, I _D = -2.6 A				250	
Forward Transconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 10 A	N		40		S
		V _{DS} = -15 V, I _D = -9.5 A	P		31		
Dynamic							
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =10V, I _D =10A P-Channel V _{DS} =-15V, V _{GS} =-10V, I _D =-5A	N		20		nC
			P		4		
Gate-Source Charge	Q _{gs}		N		7		
			P		0.8		
Gate-Drain Charge	Q _{gd}		N		7		
			P		1		
Turn-On Delay Time	t _{d(on)}	N-Chaneel V _{DD} =15V, V _{GS} =10V, I _D =1A , R _{GEN} =25Ω, P-Channel V _{DD} =-15V, V _{GS} =-10V, I _D =-1A R _{GEN} =15Ω	N		20		nS
			P		5		
Rise Time	t _r		N		9		
			P		4		
Turn-Off Delay Time	t _{d(off)}		N		70		
			P		31		
Fall-Time	t _f		N		20		
			P		28		

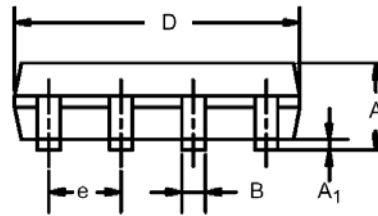
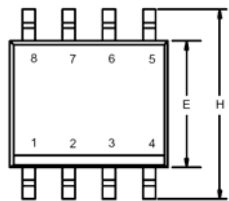
Notes

- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

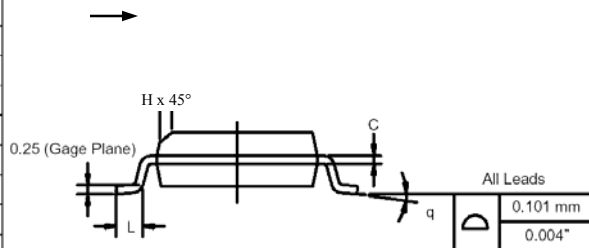
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Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°



Ordering information

- AM4528C-T1-XX
 - A: Analog Power
 - M: MOSFET
 - 4528: Part number
 - C: Complementary
 - T1: Tape & reel
 - XX: Blank: Standard
PF: Leadfree