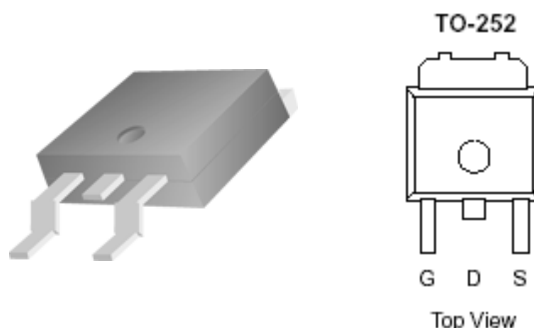


### P-Channel 32-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
-32	59 @ $V_{GS} = -10V$	24
	95 @ $V_{GS} = -4.5V$	19



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		$V_{DS}$	-32	V
Gate-Source Voltage		$V_{GS}$	$\pm 25$	
Continuous Drain Current <sup>a</sup>	$T_A=25\text{ }^\circ\text{C}$	$I_D$	24	A
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	$\pm 40$	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	-30	A
Power Dissipation <sup>a</sup>	$T_A=25\text{ }^\circ\text{C}$	$P_D$	50	W
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

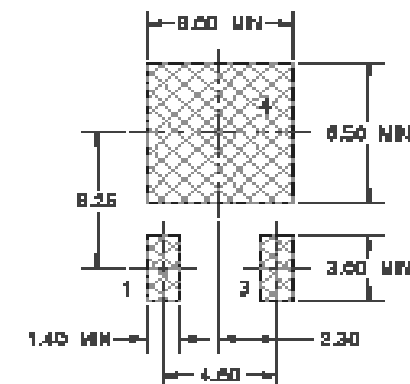
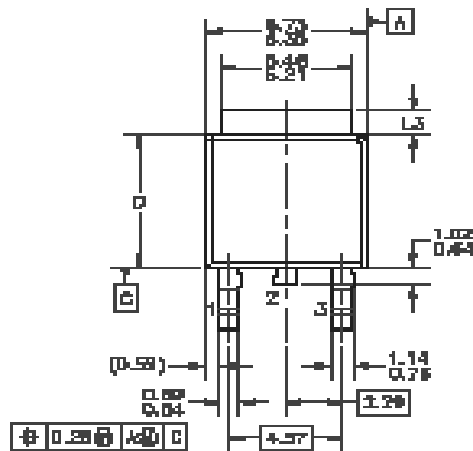
SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 uA	-1			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V			-1	uA
		V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			-5	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -10 V	-41			A
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -24 A			59	mΩ
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -19 A			95	
Forward Transconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -24 A		31		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = -41 A, V <sub>GS</sub> = 0 V		-0.7		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -24 A		6.4		nC
Gate-Source Charge	Q <sub>gs</sub>			1.9		
Gate-Drain Charge	Q <sub>gd</sub>			2.5		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz		520		pF
Output Capacitance	C <sub>oss</sub>			130		
Reverse Transfer Capacitance	C <sub>rss</sub>			70		
<b>Switching</b>						
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, R <sub>L</sub> = 15 Ω , I <sub>D</sub> = -24 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6Ω		10		nS
Rise Time	t <sub>r</sub>			2.8		
Turn-Off Delay Time	t <sub>d(off)</sub>			53.6		
Fall-Time	t <sub>f</sub>			46		

Notes

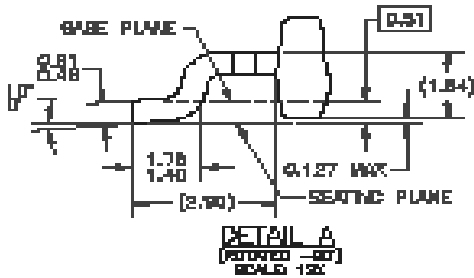
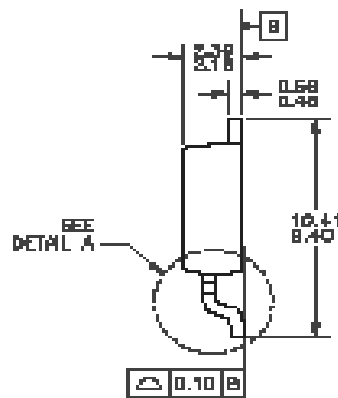
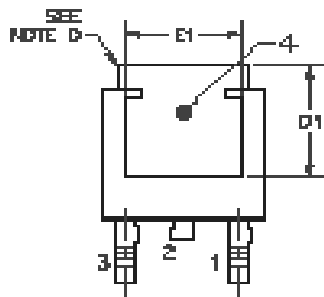
- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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# Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 30 DE, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.04M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION A1	OPTION A2
L3	0.68-1.27	1.62-2.52
D	0.92-0.92	0.92-0.92
E1	4.32 MIN	3.81 MIN
D1	3.41 MIN	4.37 MIN