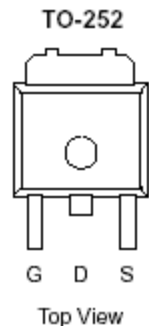
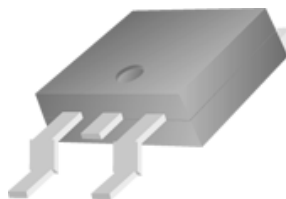


P-Channel 40-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-40	10 @ $V_{GS} = -10V$	58
	13 @ $V_{GS} = -4.5V$	51

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ C$ I_D	58	A
Pulsed Drain Current ^b	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	-30	A
Power Dissipation ^a	$T_A = 25^\circ C$ P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ C$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

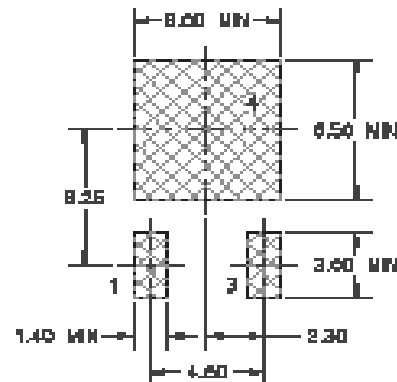
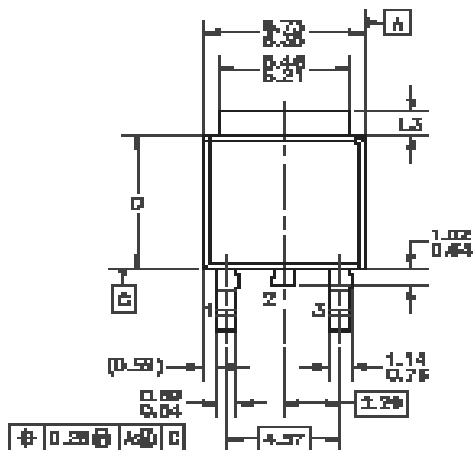
SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 25\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24\ \text{V}, V_{GS} = 0\ \text{V}$			-1	uA
		$V_{DS} = -24\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -10\ \text{V}$	-41			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -36\ \text{A}$			10	m Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -29\ \text{A}$			13	
Forward Transconductance ^A	g_s	$V_{DS} = -15\ \text{V}, I_D = -36\ \text{A}$		31		S
Diode Forward Voltage	V_{SD}	$I_S = -41\ \text{A}, V_{GS} = 0\ \text{V}$		-0.7		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15\ \text{V}, V_{GS} = -4.5\ \text{V},$ $I_D = -36\ \text{A}$		15.3		nC
Gate-Source Charge	Q_{gs}			5.2		
Gate-Drain Charge	Q_{gd}			5.8		
Switching						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ \text{V}, R_L = 15\ \Omega, I_D = -41\ \text{A},$ $V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		15		nS
Rise Time	t_r			12		
Turn-Off Delay Time	$t_{d(off)}$			62		
Fall-Time	t_f			46		

Notes

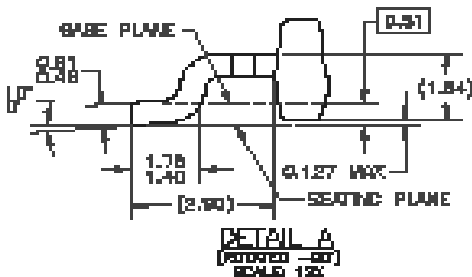
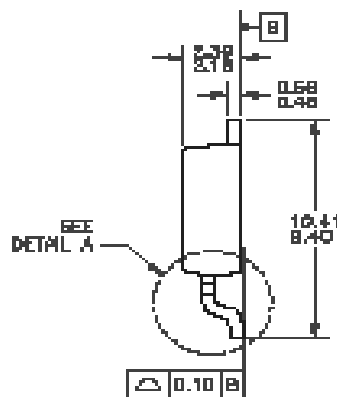
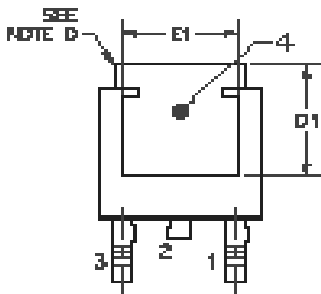
- Pulse test: $PW \leq 300\ \mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 31 DEJ, DATED NOV. 1989.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.004-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3, D, E1 & D1 TABLE:

	SECTION AA	SECTION AB
L3	0.68-1.27	1.62-2.54
D	0.97-0.99	0.93-0.99
E1	4.32 MIN	3.81 MIN
D1	3.81 MIN	4.37 MIN