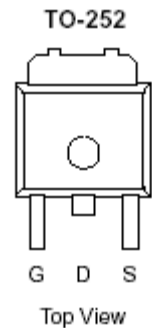
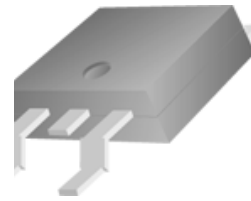


## N-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, and cordless telephones.

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
100	13 @ $V_{GS} = 10V$	51
	14 @ $V_{GS} = 5.5V$	49

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$T_C=25^\circ\text{C}$ $I_D$	51	A
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	100	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	30	A
Power Dissipation <sup>a</sup>	$T_C=25^\circ\text{C}$ $P_D$	50	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	34			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 1 \text{ A}$			13	m $\Omega$
		$V_{GS} = 5.5 \text{ V}, I_D = 1 \text{ A}$			14	
Forward Transconductance <sup>A</sup>	$g_{fs}$	$V_{DS} = 40 \text{ V}, I_D = 1 \text{ A}$		4.4		S
Diode Forward Voltage	$V_{SD}$	$I_S = 1 \text{ A}, V_{GS} = 0 \text{ V}$		1.1		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 25 \text{ V}, V_{GS} = 10 \text{ V},$ $I_D = 1 \text{ A}$		60		nC
Gate-Source Charge	$Q_{gs}$			20		
Gate-Drain Charge	$Q_{gd}$			10		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100 \text{ V}, R_L = 25 \Omega, I_D = 9 \text{ A},$ $V_{GEN} = 10 \text{ V}$		20		nS
Rise Time	$t_r$			10		
Turn-Off Delay Time	$t_{d(off)}$			190		
Fall-Time	$t_f$			40		

## Notes

- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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