

## N-Channel 100-V (D-S) MOSFET

### Key Features:

- Low  $r_{DS(on)}$  trench technology
- Low thermal impedance
- Fast switching speed

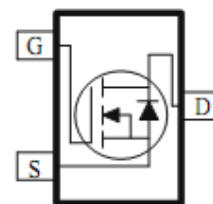
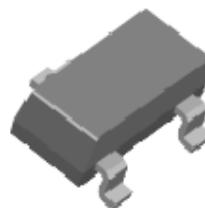
### Typical Applications:

- PoE Power Sourcing Equipment
- PoE Powered Devices
- Telecom DC/DC converters
- White LED boost converters

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
100	280 @ $V_{GS} = 10V$	1.5
	355 @ $V_{GS} = 4.5V$	1.3



RoHS  
COMPLIANT  
HALOGEN  
FREE



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	1.5
		$T_A = 70^\circ\text{C}$	1.2
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	10	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.6	A
Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	1.3
		$T_A = 70^\circ\text{C}$	0.8
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	t $\leq$ 10 sec	100
		Steady State	166

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

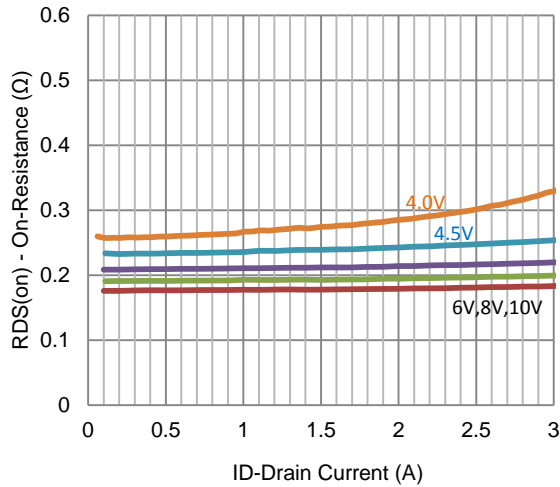
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = 20 V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80 V, V_{GS} = 0 V$			1	uA
		$V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55^\circ C$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = 5 V, V_{GS} = 10 V$	4			A
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 10 V, I_D = 1.2 A$			280	m $\Omega$
		$V_{GS} = 4.5 V, I_D = 1.0 A$			355	
Forward Transconductance	$g_{fs}$	$V_{DS} = 15 V, I_D = 1.2 A$		5		S
Diode Forward Voltage	$V_{SD}$	$I_S = 0.8 A, V_{GS} = 0 V$		0.75		V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 1.2 A$		3.9		nC
Gate-Source Charge	$Q_{gs}$			1.3		
Gate-Drain Charge	$Q_{gd}$			2.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50 V, R_L = 41.7 \Omega, I_D = 1.2 A,$ $V_{GEN} = 10 V, R_{GEN} = 6 \Omega$		4.8		nS
Rise Time	$t_r$			3.9		
Turn-Off Delay Time	$t_{d(off)}$			12.7		
Fall-Time	$t_f$			3.2		
Input Capacitance	$C_{iss}$	$V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz$		332		pF
Output Capacitance	$C_{oss}$			40		
Reverse Transfer Capacitance	$C_{rss}$			29		
Gate Resistance	$R_g$	$f = 1 MHz$		0.3		$\Omega$

## Notes

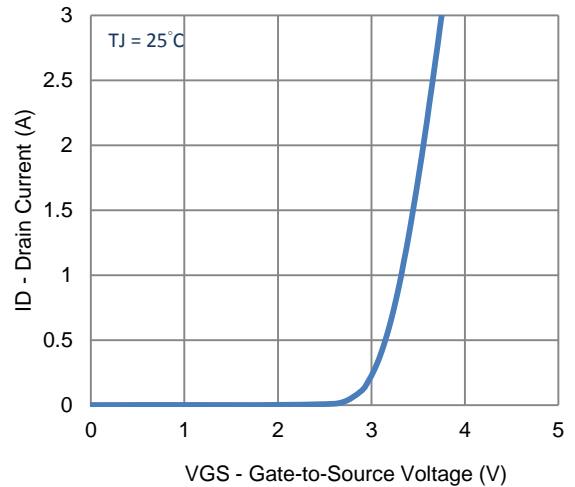
- Pulse test: PW  $\leq$  300us duty cycle  $\leq$  2%.
- Guaranteed by design, not subject to production testing.

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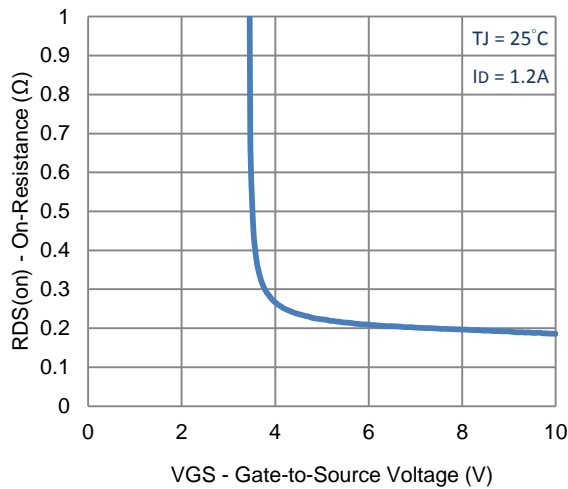
### Typical Electrical Characteristics



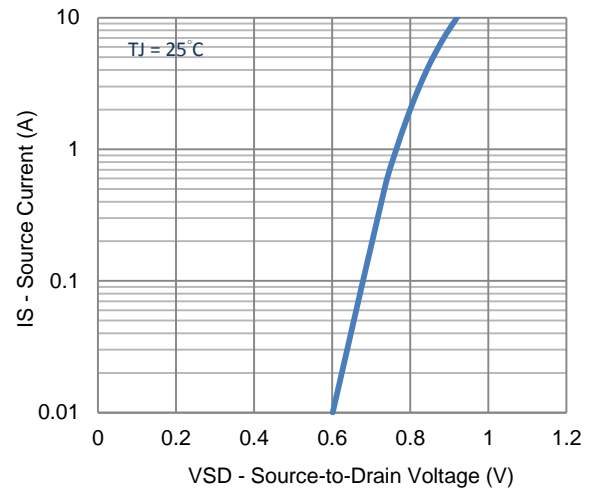
1. On-Resistance vs. Drain Current



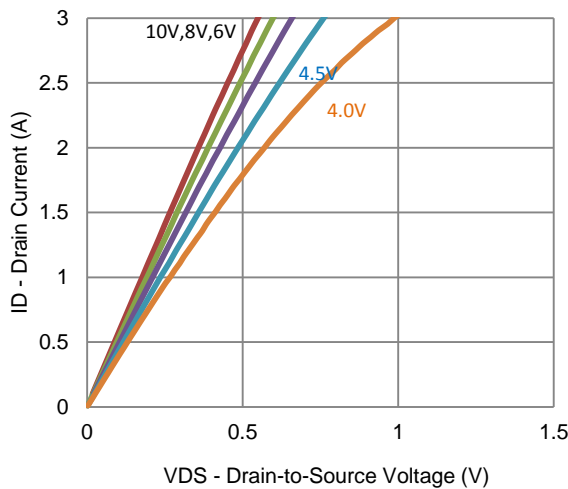
2. Transfer Characteristics



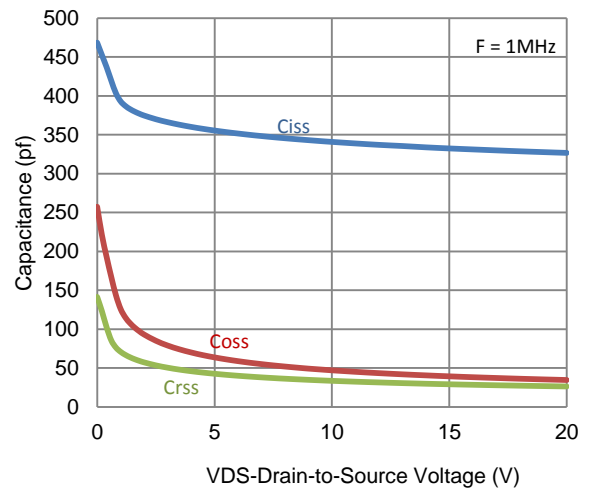
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

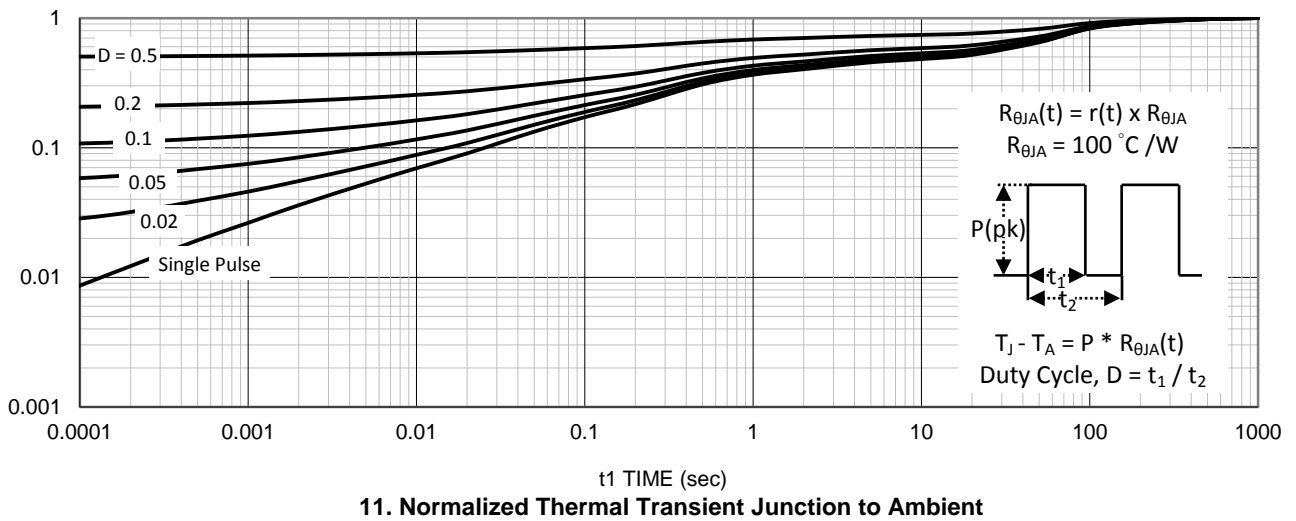
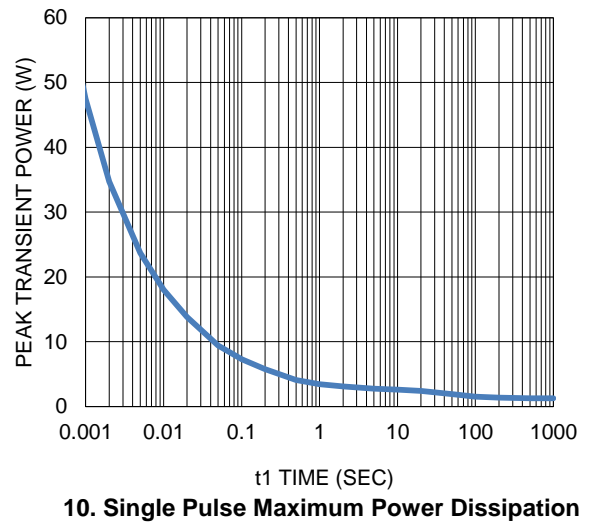
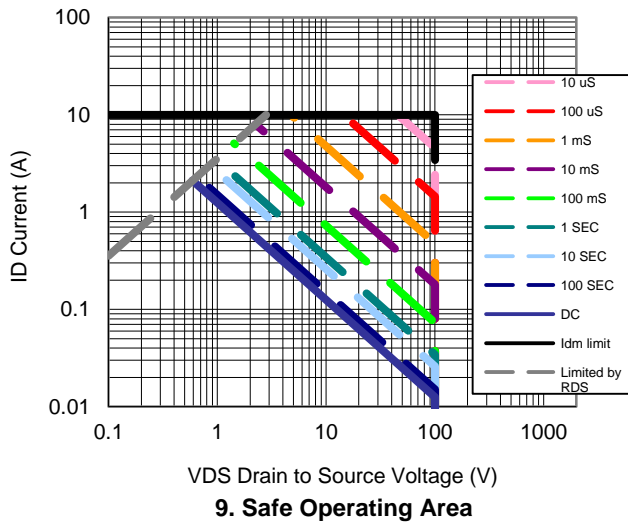
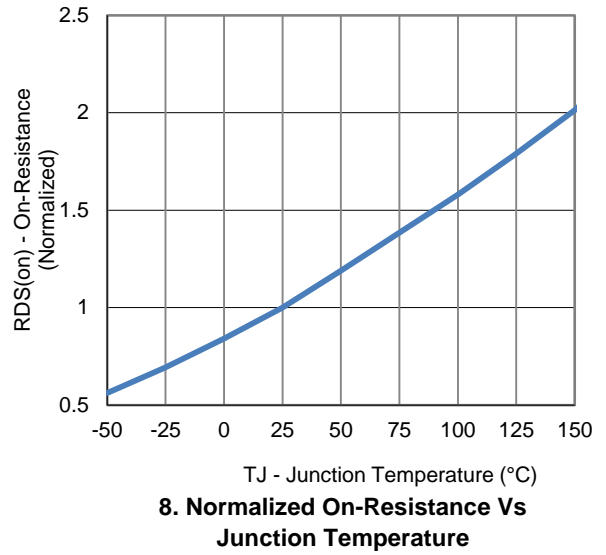
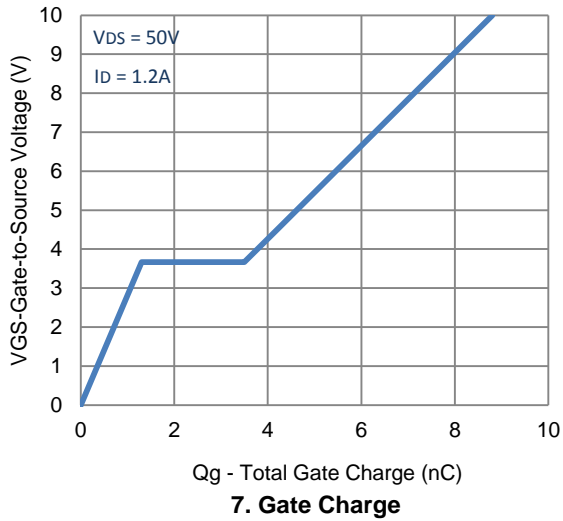


5. Output Characteristics

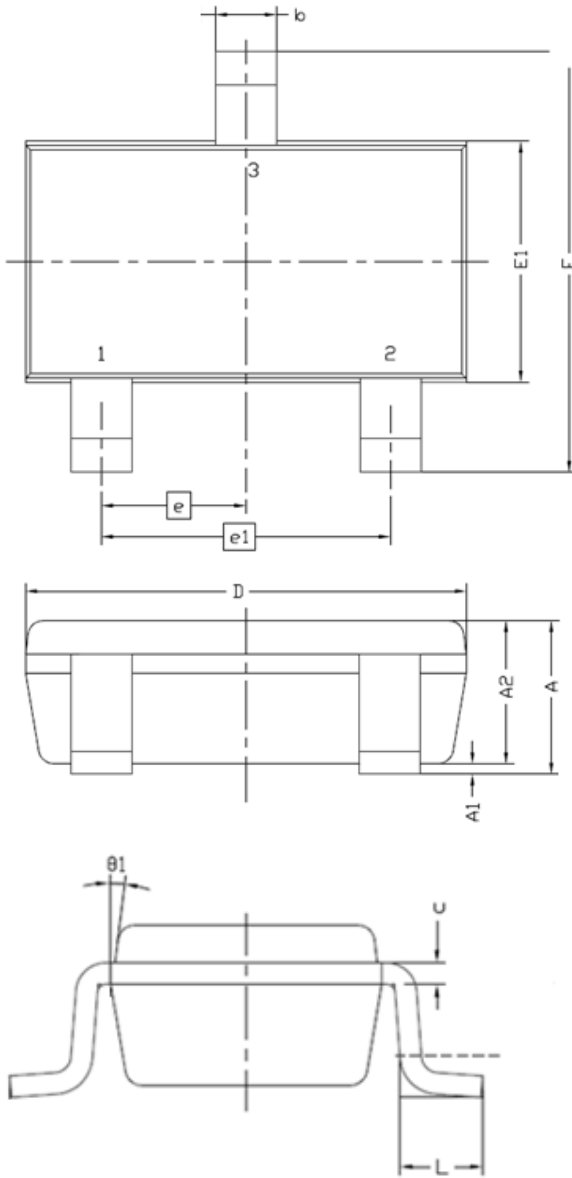


6. Capacitance

Typical Electrical Characteristics



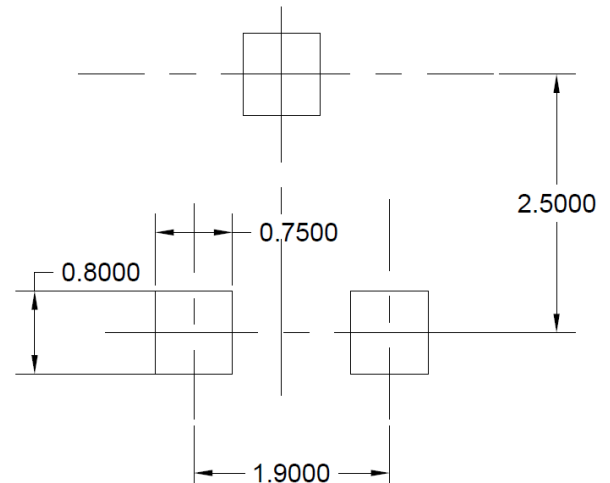
Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
theta1	7° NOM	

Recommended Pad Layout

Note: Drain opening is recommended to be solder mask defined in a copper fill to provide improved thermal performance



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