

### N-Channel 60-V (D-S) MOSFET

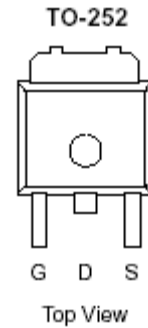
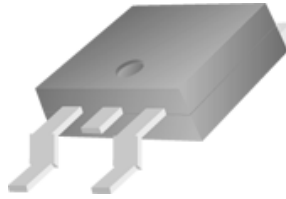
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
60	28 @ $V_{GS} = 10V$	35
	30 @ $V_{GS} = 4.5V$	34

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$T_C=25^\circ C$ $I_D$	35	A
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	140	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	35	A
Power Dissipation <sup>a</sup>	$T_C=25^\circ C$ $P_D$	50	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

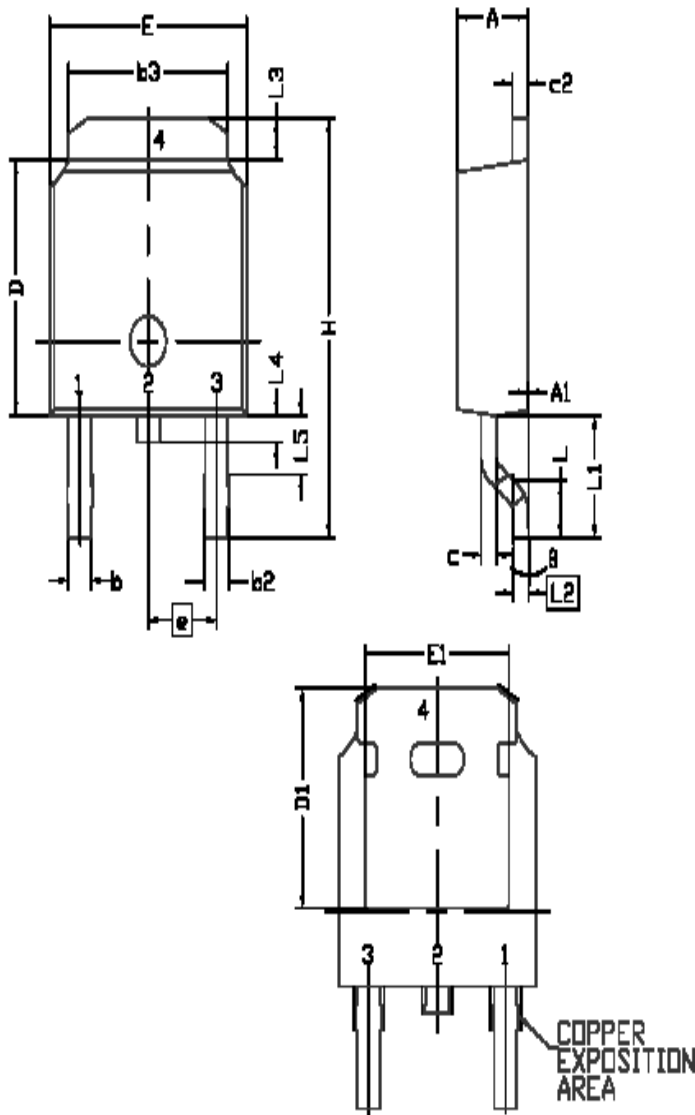
SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	35			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$			28	mΩ
		$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$			30	
Forward Transconductance <sup>A</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 3 \text{ A}$		25		S
Diode Forward Voltage	$V_{SD}$	$I_S = 2 \text{ A}, V_{GS} = 0 \text{ V}$		1.1		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 30 \text{ A}$		26		nC
Gate-Source Charge	$Q_{gs}$			5		
Gate-Drain Charge	$Q_{gd}$			13		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25 \text{ V}, R_L = 25 \Omega, I_D = 30 \text{ A},$ $V_{GEN} = 10 \text{ V}$		6		nS
Rise Time	$t_r$			6		
Turn-Off Delay Time	$t_{d(off)}$			50		
Fall-Time	$t_f$			20		

## Notes

- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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# Package Information



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	—	1.27
L4	0.64	—	1.01
L5	—	—	—
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	3.21	3.34	3.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	—	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.30	—	—
E1	4.40	—	—
θ	0°	—	10°