

N-Channel 55V (D-S) MOSFET

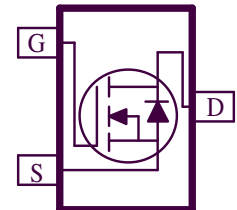
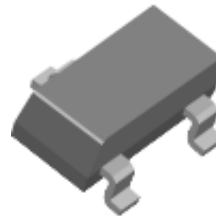
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
55	0.160 @ $V_{GS} = 4.5$ V	2.4
	0.200 @ $V_{GS} = 2.5$ V	2.1

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology



RoHS
COMPLIANT
HALOGEN
FREE
Available



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	55	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ^a	I_D	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Pulsed Drain Current ^b	I_{DM}	± 10	
Continuous Source Current (Diode Conduction) ^a	I_S	1	A
Power Dissipation ^a	P_D	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	R_{THJA}	$t \leq 5$ sec	$^\circ\text{C}/\text{W}$
		Steady-State	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

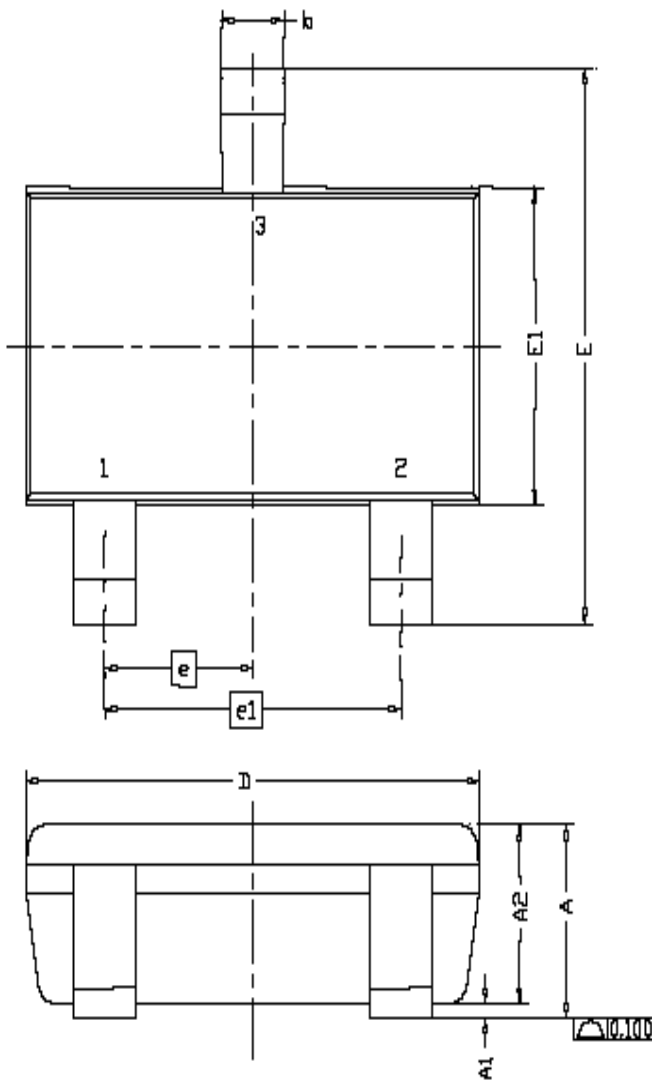
SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 44 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 44 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			50	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	10			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 2.4 \text{ A}$			160	m Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 2.1 \text{ A}$			200	
Forward Transconductance ^A	g_s	$V_{DS} = 4.5 \text{ V}, I_D = 2.4 \text{ A}$		8		S
Diode Forward Voltage	V_{SD}	$I_S = 1.7 \text{ A}, V_{GS} = 0 \text{ V}$		1.10		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 30 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 2.4 \text{ A}$		3.6		nC
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}, R_L = 30 \Omega, I_D = 1 \text{ A},$ $V_{GEN} = 10 \text{ V}$		10		ns
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			20		
Fall-Time	t_f			10		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7°NOM		

