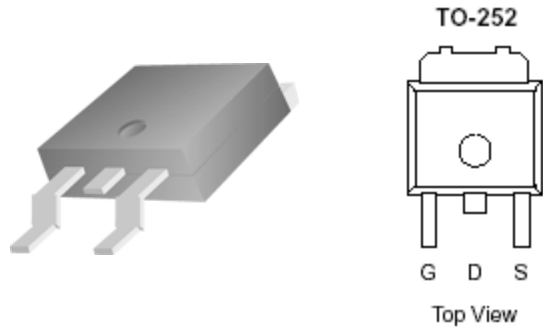


**N-Channel 60-V (D-S) MOSFET**

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low  $r_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> m(Ω)	I <sub>D</sub> (A)
60	94 @ V <sub>GS</sub> = 10V	19
	109 @ V <sub>GS</sub> = 4.5V	18



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	±20	
Continuous Drain Current <sup>a</sup>	T <sub>C</sub> =25°C I <sub>D</sub>	19	A
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	40	
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	30	A
Power Dissipation <sup>a</sup>	T <sub>C</sub> =25°C P <sub>D</sub>	50	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>θJA</sub>	50	°C/W
Maximum Junction-to-Case	R <sub>θJC</sub>	3.0	°C/W

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

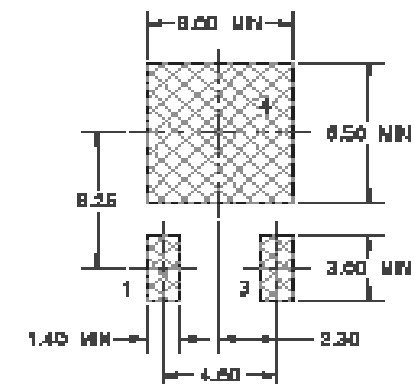
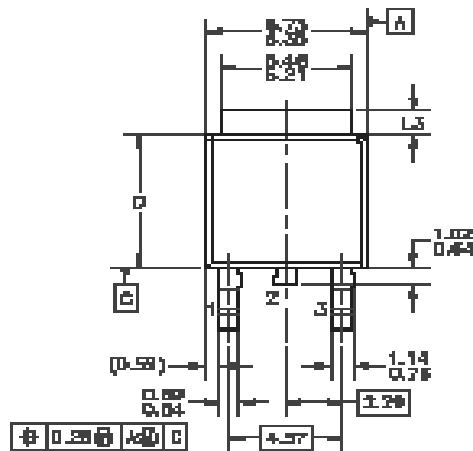
SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 uA	1.0			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V			1	uA
		V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			25	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	34			A
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 19 A			94	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 18 A			109	
Forward Transconductance <sup>A</sup>	g <sub>f</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 19 A		22		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 24 A, V <sub>GS</sub> = 0 V		1.1		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 19 A		4.0		nC
Gate-Source Charge	Q <sub>gs</sub>			1.1		
Gate-Drain Charge	Q <sub>gd</sub>			1.4		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 25 V, R <sub>L</sub> = 25 Ω, I <sub>D</sub> = 24 A, V <sub>GEN</sub> = 10 V		16		nS
Rise Time	t <sub>r</sub>			5		
Turn-Off Delay Time	t <sub>d(off)</sub>			23		
Fall-Time	t <sub>f</sub>			3		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		I <sub>F</sub> = 24 A, Di/Dt = 100 A/uS		50	

## Notes

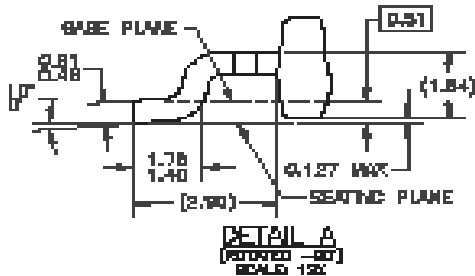
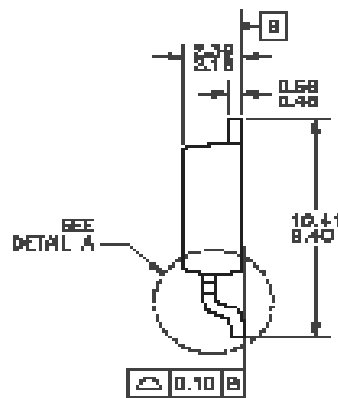
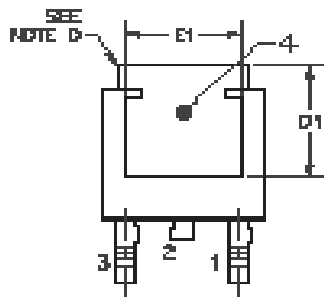
- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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# Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 30 DE, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.04M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.68-1.27	1.62-2.52
D	0.92-0.92	0.43-0.43
E1	4.32 MIN	3.81 MIN
D1	3.41 MIN	4.37 MIN