Elektronische Bauelemente

SSD80N03

80A , 30V , $R_{DS(ON)}$ 5.5mΩ

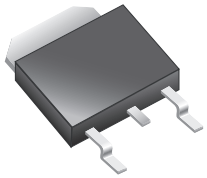
N-Ch Enhancement Mode Power MOSFET

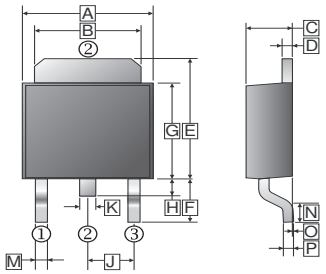
RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD80N03 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .

TO-252(D-Pack)



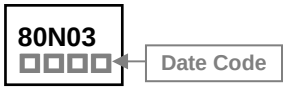


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	J	2.30 REF.	
B	5.20	5.50	K	0.64	0.90
C	2.15	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.65
E	6.8	7.5	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.25			
H	0.64	1.20			

FEATURES

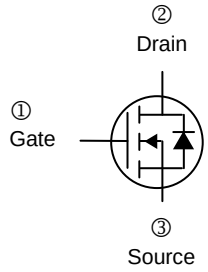
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	V_{GS}=10V, T_C=25℃	I_D	80	A
	V_{GS}=10V,T_C=100℃		57	A
Pulsed Drain Current [2]		I_{DM}	160	A
Total Power Dissipation [4]	T_C=25℃	P_D	59	W
Linear Derating Factor			0.5	W / ℃
Single Pulse Avalanche Energy [3]		E_{AS}	252	mJ
Single Pulse Avalanche Current		I_{AS}	48	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Rating				
Maximum Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	62	℃ / W
Maximum Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	2.1	℃ / W

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static							
Drain-Source Breakdown Voltage		BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	1.0	-	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transconductance		g_{fs}	-	43	-	S	V_{DS}=5V, I_D=30A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J =25℃	I_{DSS}	-	-	1	μA	V_{DS}=24V, V_{GS}=0
	T_J =55℃		-	-	5		V_{DS}=24V, V_{GS}=0
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	-	5.5	mΩ	V_{GS}=10V, I_D=30A
			-	-	8		V_{GS}=4.5V, I_D=15A
Total Gate Charge		Q_g	-	20	-	nC	I_D=15A V_{DS}=15V V_{GS}=4.5V
Gate-Source Charge		Q_{gs}	-	7.6	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	7.2	-		
Turn-on Delay Time		$T_{d(on)}$	-	7.8	-	nS	V_{DD}=15V I_D=15A V_{GS}=10V R_G=3.3 Ω
Rise Time		T_r	-	15	-		
Turn-off Delay Time		$T_{d(off)}$	-	37.3	-		
Fall Time		T_f	-	10.6	-		
Input Capacitance		C_{iss}	-	2295	-	pF	V_{GS} =0 V_{DS}=15V f =1.0MHz
Output Capacitance		C_{oss}	-	267	-		
Reverse Transfer Capacitance		C_{rss}	-	210	-		
Guaranteed Avalanche Characteristics							
Single Pulse Avalanche Energy [5]		EAS	63	-	-	mJ	V_{DD}=25V,L=0.1mH , I_{AS}=24A
Source-Drain Diode							
Diode Forward Voltage [2]		V_{SD}	-	-	1	V	I_S=1A, V_{GS}=0
Continuous Source Current [1,6]		I_S	-	-	80	A	V_D=V_G=0, Force Current
Pulsed Source Current [2,6]		I_{SM}	-	-	160	A	
Reverse Recovery Time		T_{RR}	-	14	-	nS	I_F=30A, dI/dt=100A/μS T_J =25℃
Reverse Recovery Charge		Q_{RR}	-	5	-	nC	

Notes:
1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width≦300μs , duty cycle≦2%
3. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=48A
4. The power dissipation is limited by 150℃ junct ion temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

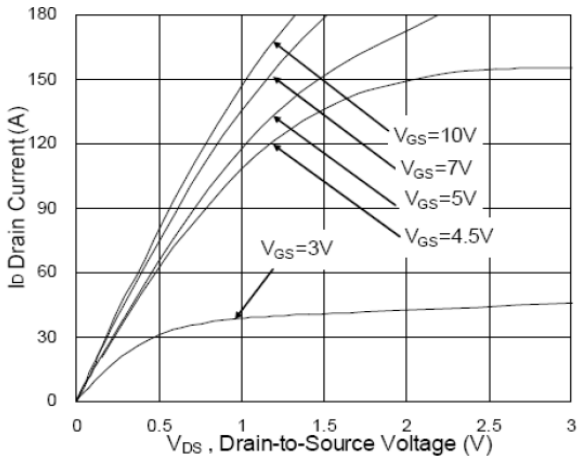


Fig.1 Typical Output Characteristics

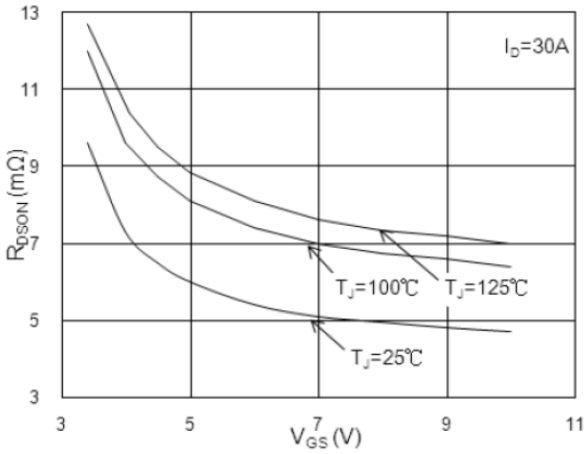


Fig.2 On-Resistance vs. G-S Voltage

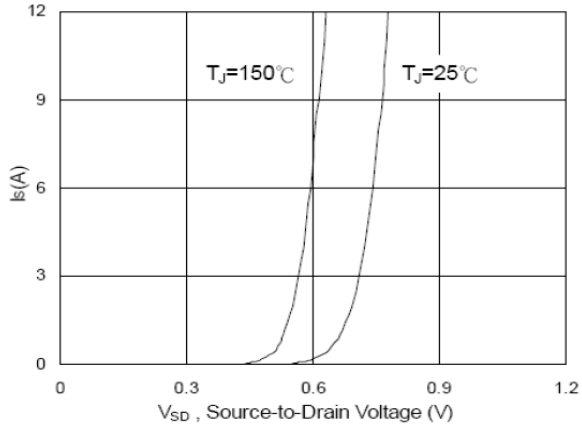


Fig.3 Forward Characteristics of Reverse

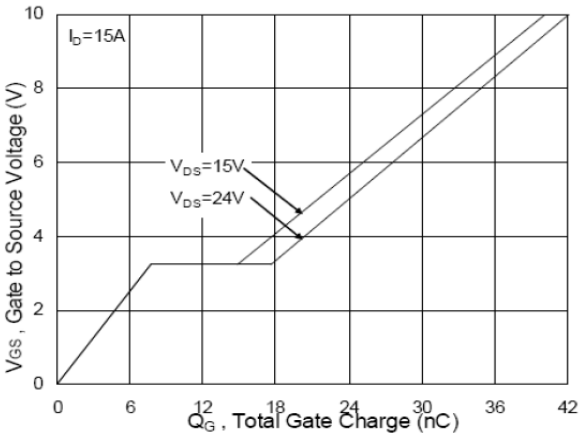


Fig.4 Gate-Charge Characteristics

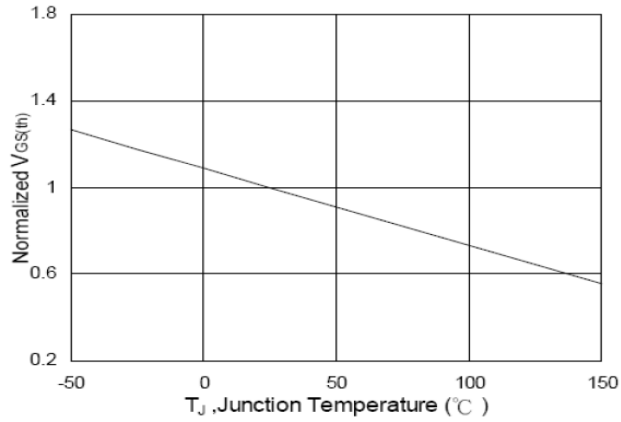


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

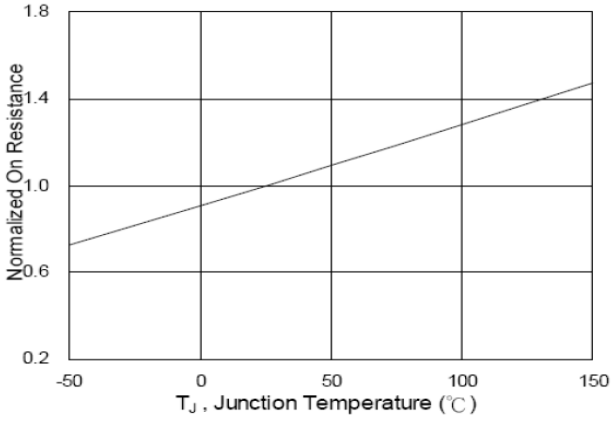


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVES

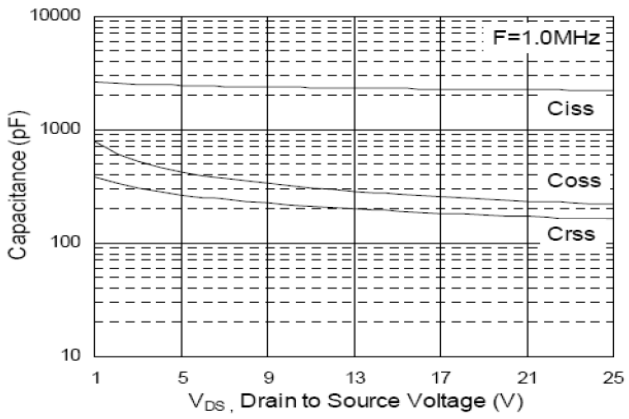


Fig.7 Capacitance

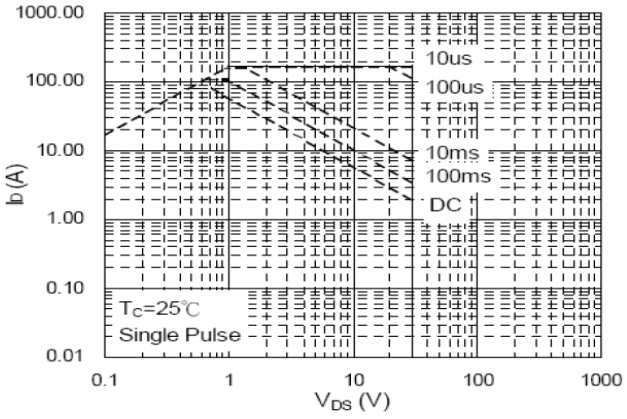


Fig.8 Safe Operating Area

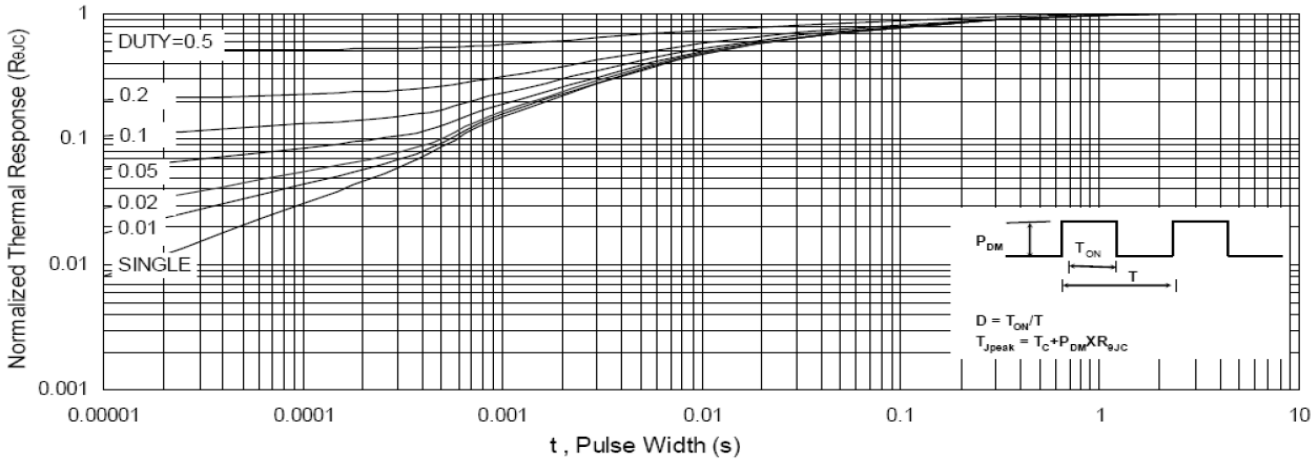


Fig.9 Normalized Maximum Transient Thermal Impedance

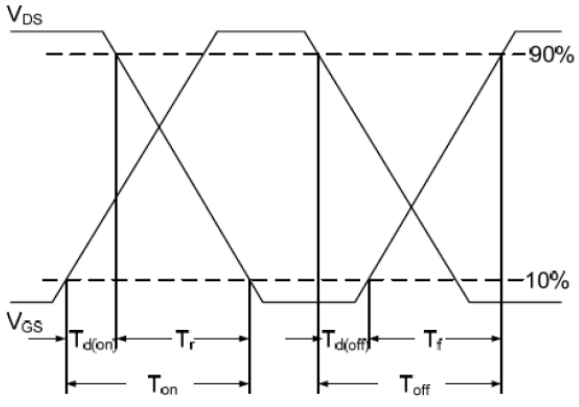


Fig.10 Switching Time Waveform

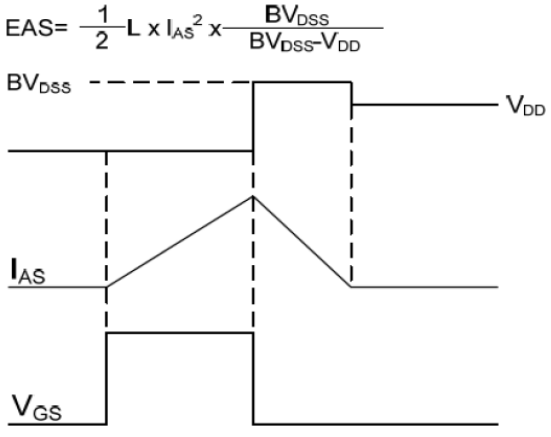


Fig.11 Unclamped Inductive Switching Waveform