

DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTORS 2SK2365/2SK2366

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2365, 2SK2365-Z/2SK2366, 2SK2366-Z is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-Resistance
2SK2365: $R_{DS(on)} = 0.5 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 5.0 \text{ A}$)
2SK2366: $R_{DS(on)} = 0.6 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 5.0 \text{ A}$)
- Low C_{iss} $C_{iss} = 1\ 600 \text{ pF TYP.}$
- High Avalanche Capability Ratings
- Isolate TO-220 Package

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$)

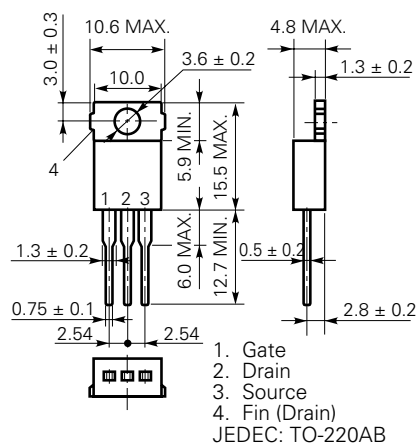
Drain to Source Voltage (2SK2365/2SK2366)	V_{DS}	450/500	V
Gate to Source Voltage	V_{GS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 10	A
Drain Current (pulse)*	$I_{D(pulse)}$	± 40	A
Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$)	P_{T1}	75	W
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$)	P_{T2}	1.5	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	I_{AS}	10	A
Single Avalanche Energy**	E_{AS}	143	mJ

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$

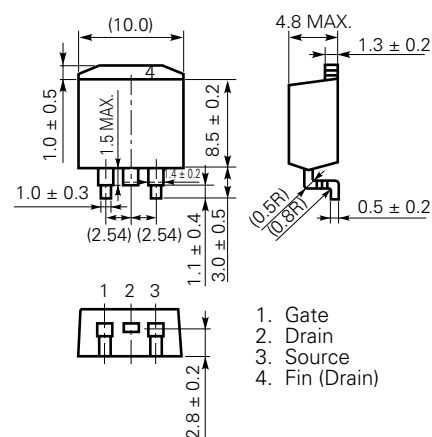
** Starting $T_{ch} = 25 \text{ }^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

PACKAGE DIMENSIONS

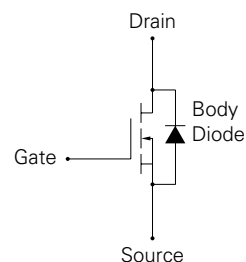
(in millimeters)



MP-25 (TO-220)



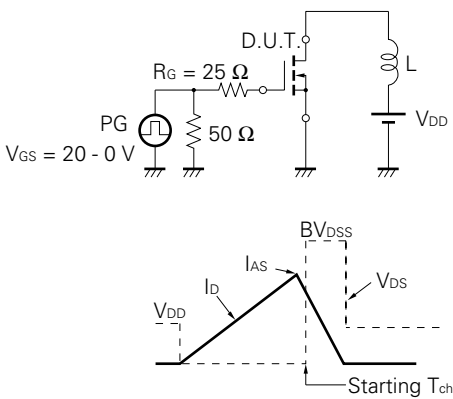
MP-25Z (SURFACE MOUNT TYPE)



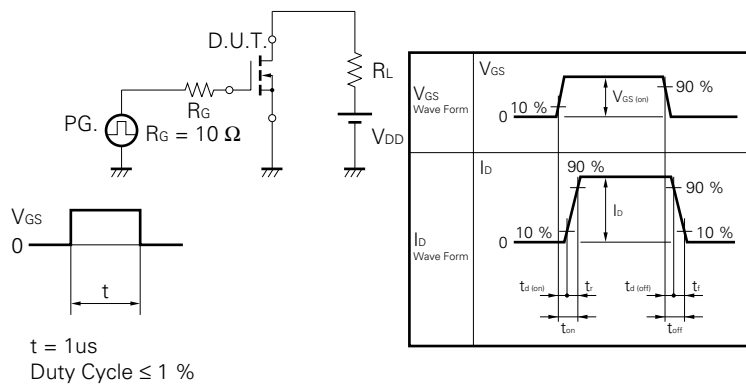
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-State Resistance	R _{DS(on)}		0.4	0.5	Ω	V _{GS} = 10 V
			0.5	0.6		I _D = 5.0 A
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	4.0			S	V _{DS} = 10 V, I _D = 5.0 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = V _{DSS} , V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		1 600		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		310		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		30		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		30		ns	I _D = 5.0 A
Rise Time	t _r		20		ns	V _{GS} = 10 V
Turn-Off Delay Time	t _{d(off)}		80		ns	V _{DD} = 150 V
Fall Time	t _f		20		ns	R _G = 10 Ω R _L = 30 Ω
Total Gate Charge	Q _G		42		nC	I _D = 10 A
Gate to Source Charge	Q _{GS}		10		nC	V _{DD} = 400 V
Gate to Drain Charge	Q _{GD}		20		nC	V _{GS} = 10 V
Body Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _F = 10 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		350		ns	I _F = 10 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		1.5		μC	di/dt = 50 A/μs

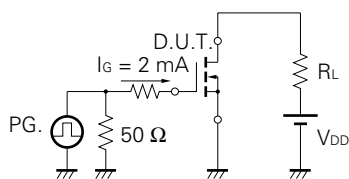
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time



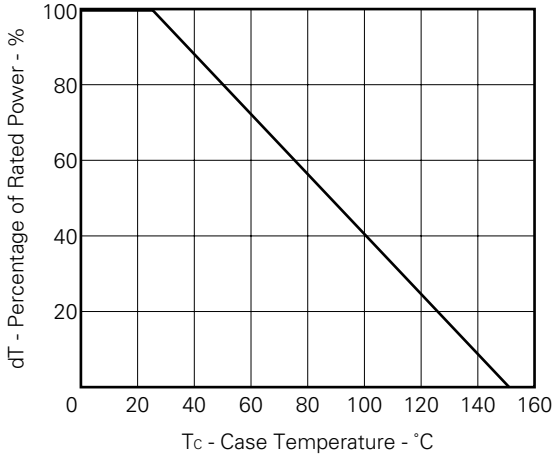
Test Circuit 3 Gate Charge



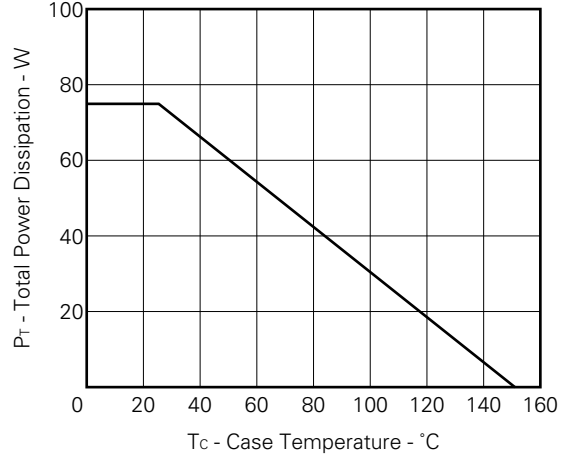
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS (T_A = 25 °C)

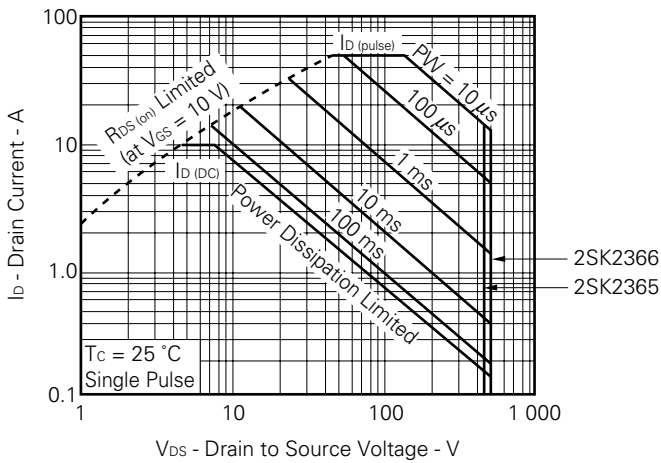
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



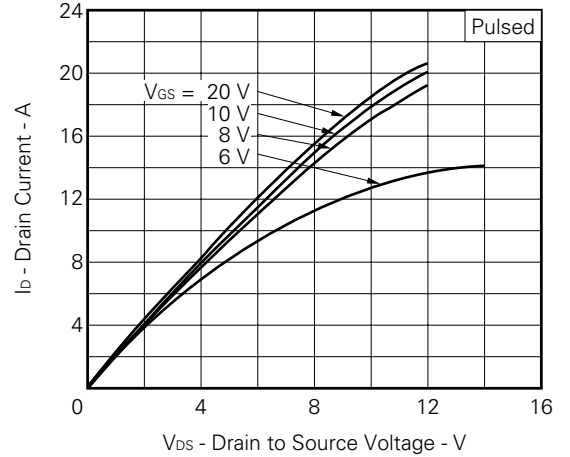
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



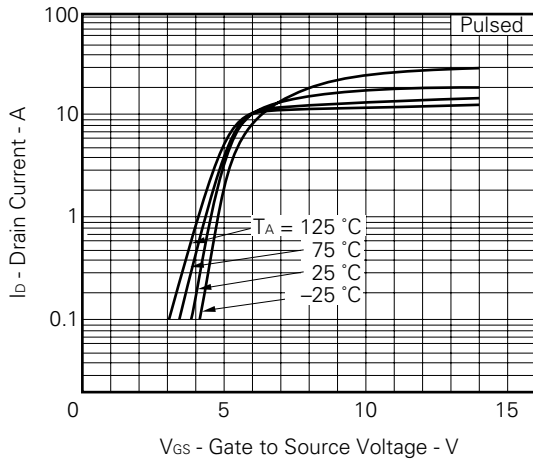
FORWARD BIAS SAFE OPERATING AREA

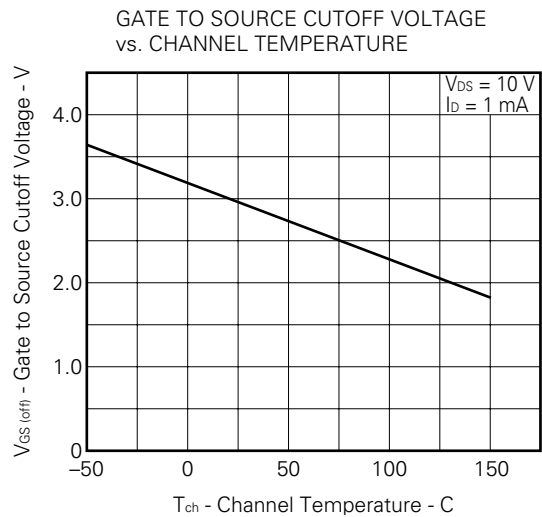
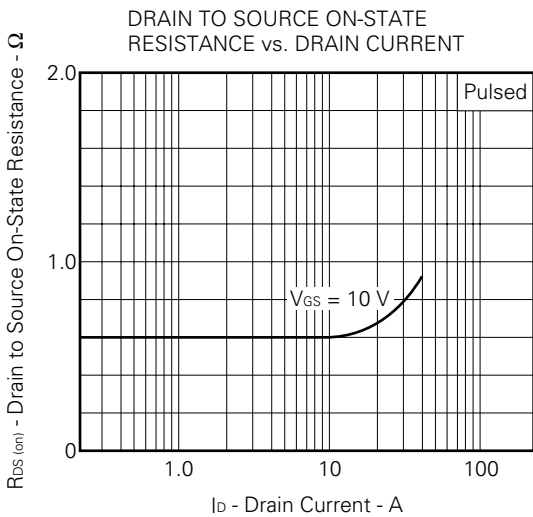
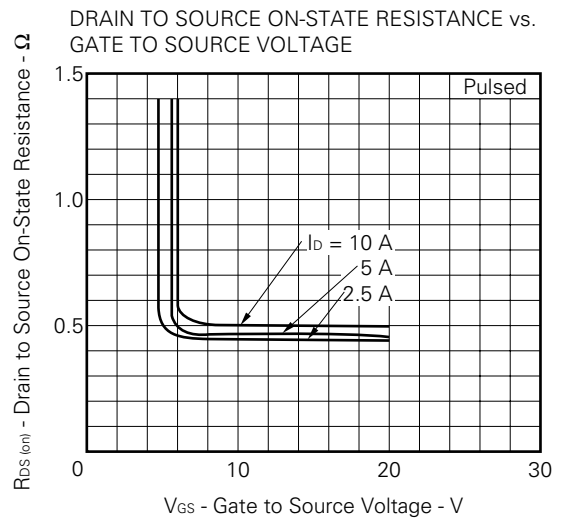
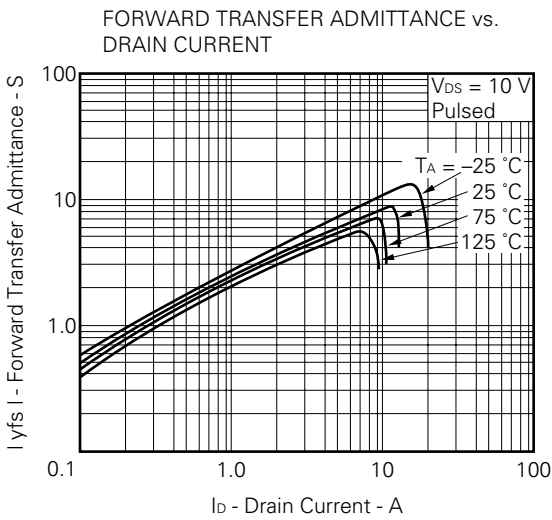
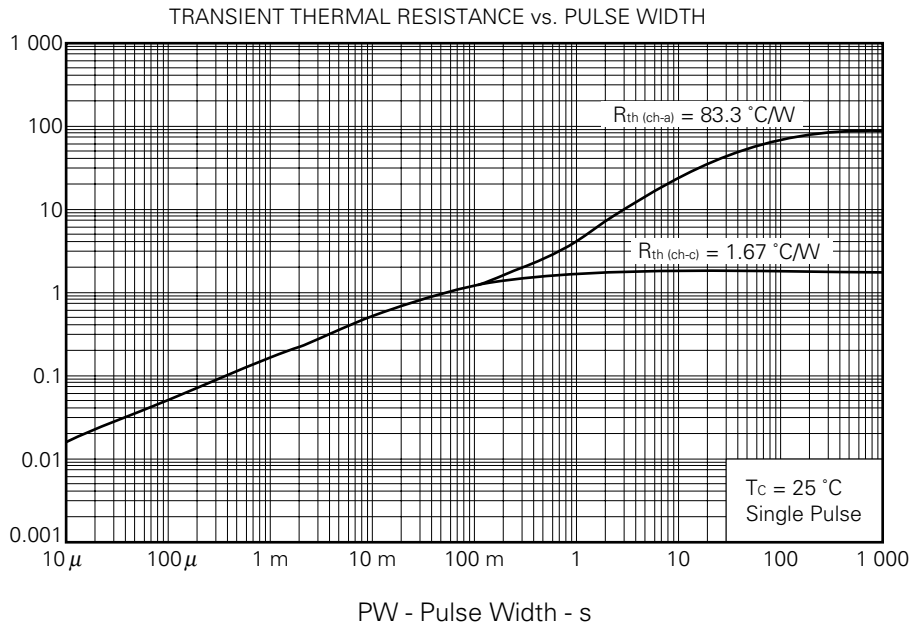


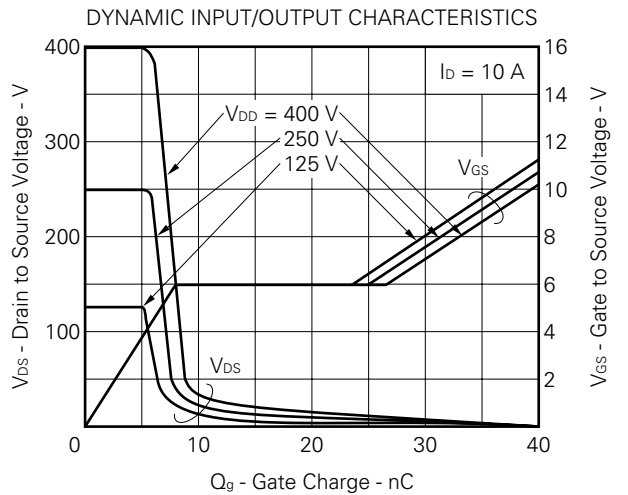
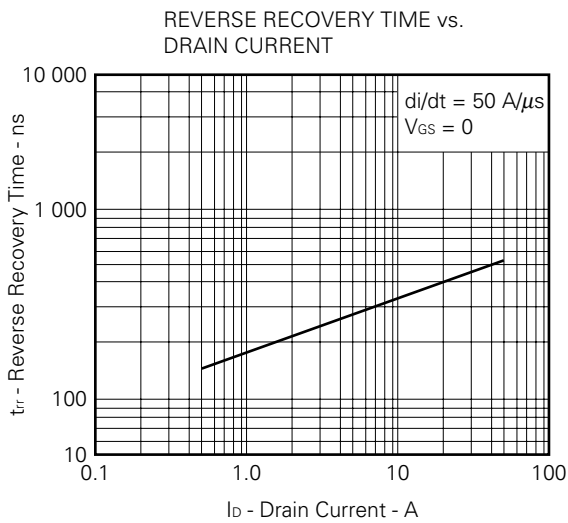
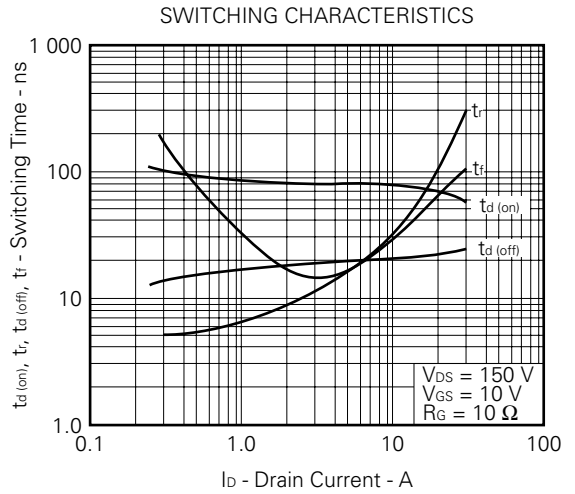
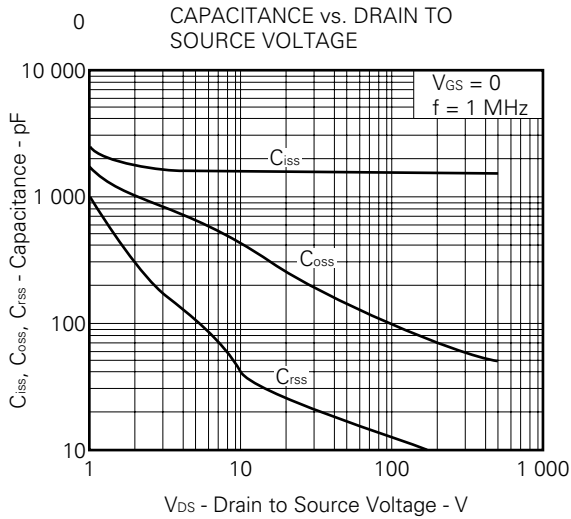
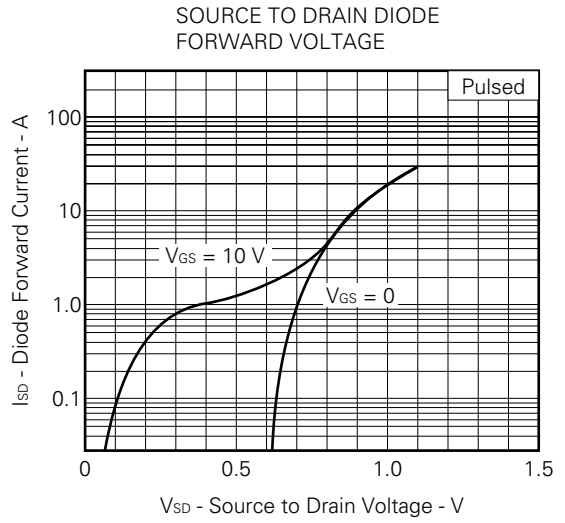
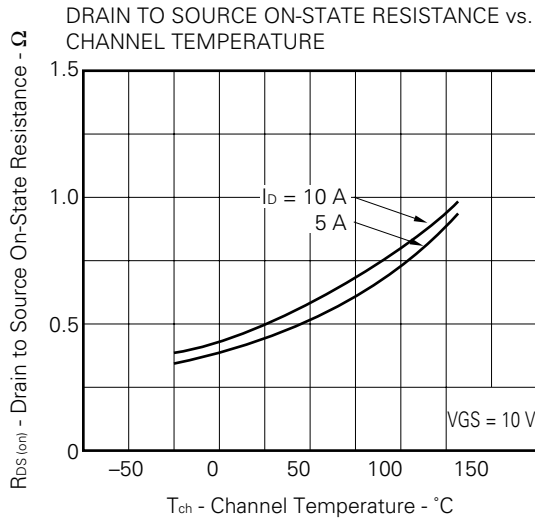
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



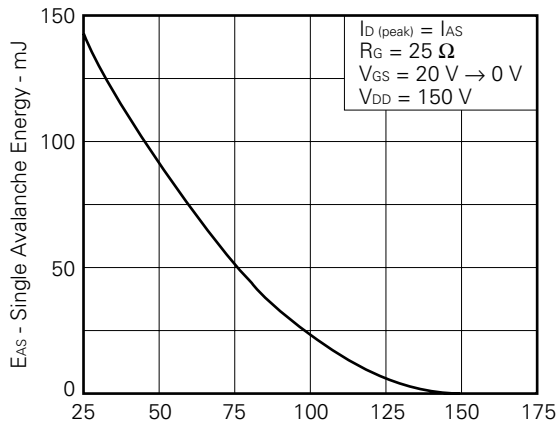
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



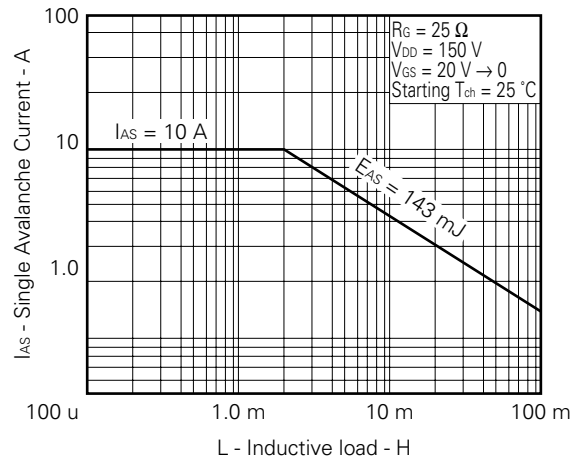




SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.

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