N-Channel MOSFETS

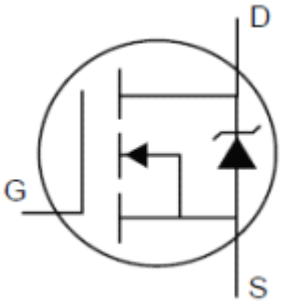
DESCRIPTION

The OGFD 20N50 is produced using advanced planar stripe DMOS technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

V_{DSS}	$R_{DS(ON)}$	I_D
500V	0.26Ω	20A

TO-3P



Features

- 20.0A,500V,$R_{DS(ON)}$=0.26 Ω@V_{GS}=10V
- Low gate charge (typical 70Nc)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

PART NUMBER	PACKAGE	BRAND
20N50	TO-3P	0GFD

Absolute Maximum Ratings (TC=25℃, unless otherwise noted)

Symbol	Parameter	20N50	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current	20	A
I_{DM}	Pulsed Drain Current@VG=10V	80	
P_D	Power Dissipation	280	W
	Derating Factor above 25℃	2.30	W/℃
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single PulseAvalanche Energy (L=1mH, IAS=40A)C	1110	mJ
dv/dt	Peak Diode Recovery dv/dt	4.5	V/ns
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	℃

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	--	--	0.44	℃/W	Water cooled heatsink, PD adjusted for a peak junction temperature of +175℃.
$R_{\theta CS}$	Case-to-Sink Typ	--	0.24	--		
$R_{\theta JA}$	Junction-to-Ambient	--	--	40		1 cubic foot chamber, free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
B_{VDSS}	Drain-to-Source Breakdown Voltage	500	--	--	V	V_{GS}=0, I_D=250uA
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	nA	V_{DS}=0V, V_{GS}=30V
I_{DSS}	Zero Gate Voltage Drain Current	--	--	1	uA	V_{DS}=500V, V_{GS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	0.21	0.26	Ω	V_{GS}=10V,I_D=10A
$V_{GS(TH)}$	Gate Threshold Voltage, Figure 12.	2.0	--	4.0	V	V_{DS}=10V, I_D=250uA

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	2700	--	pF	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ
C_{oss}	Output Capacitance	--	400	--		
C_{rss}	Reverse Transfer Capacitance	--	40	340		
Q_g	Total Gate Charge	--	70	--	nC	V_{DS}=400V, V_{GS}=10V, I_D=20A
Q_{gs}	Gate-to-Source Charge	--	18	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	35	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$T_{d(ON)}$	Turn-on Delay Time		100	--	ns	V_{DD}=250V, I_D= 20.0A R_G=25Ω
T_{rise}	Rise Time		400	--		
$T_{d(OFF)}$	Turn-Off Delay Time		100	--		
T_{fall}	Fall Time		100	--		

Typical Characteristics

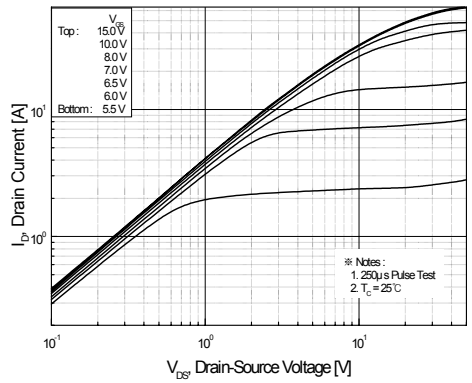


Figure 1. On-Region Characteristics

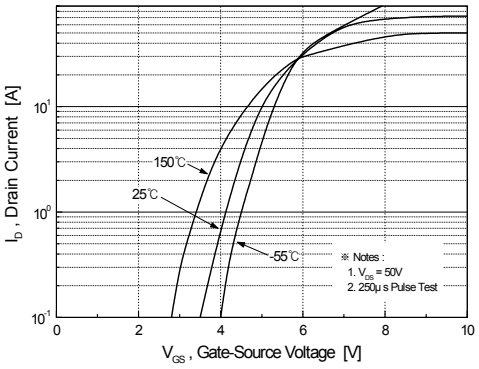


Figure 2. Transfer Characteristics

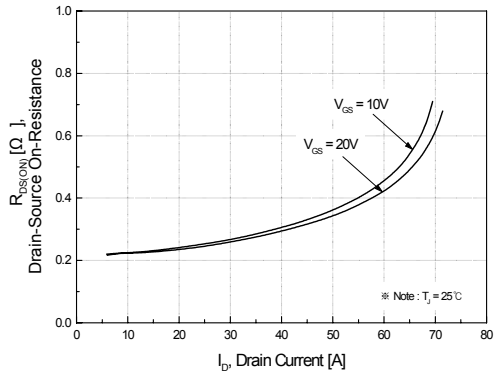


Figure 3. On-Resistance Variation vs

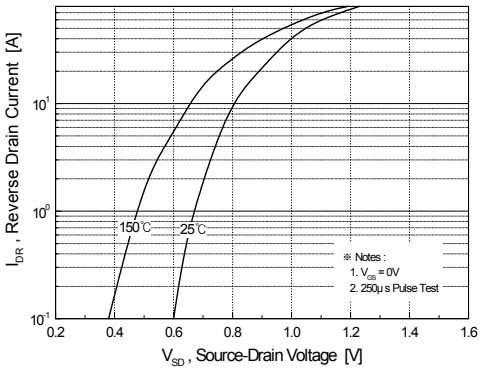


Figure 4. Body Diode Forward Voltage

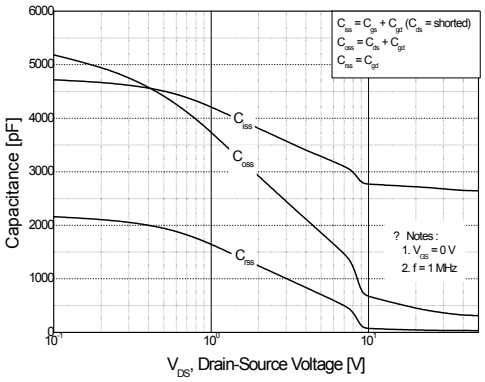


Figure 5. Capacitance Characteristics

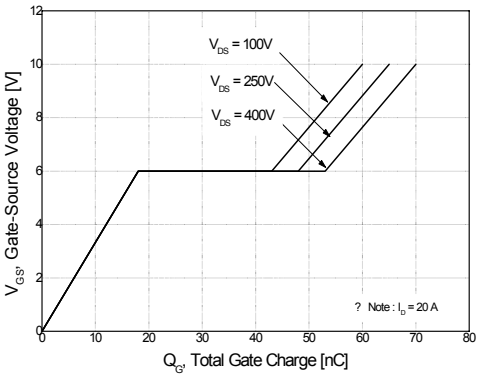


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

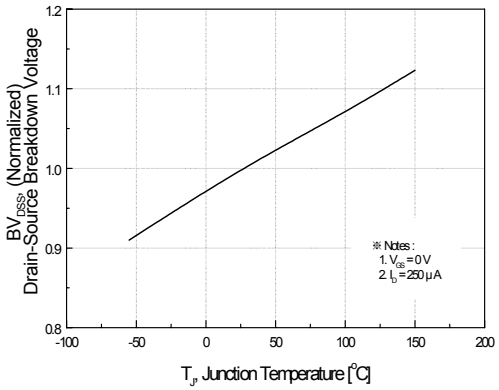


Figure 7. Breakdown Voltage Variation

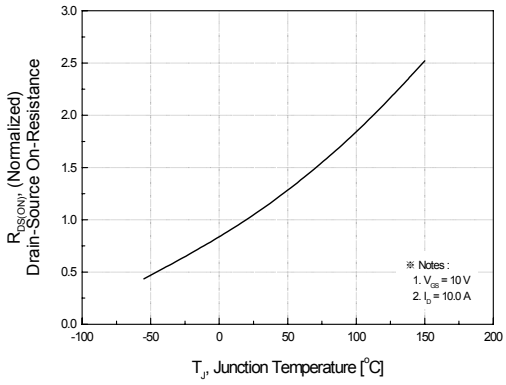


Figure 8. On-Resistance Variation

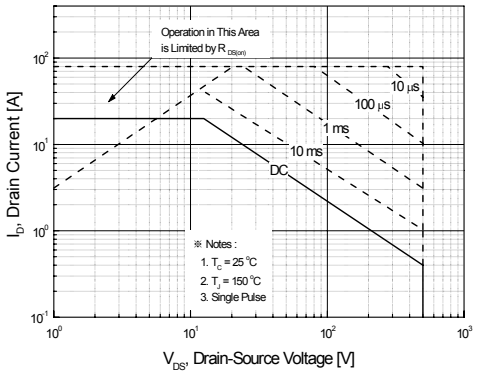


Figure 9. Maximum Safe Operating Area

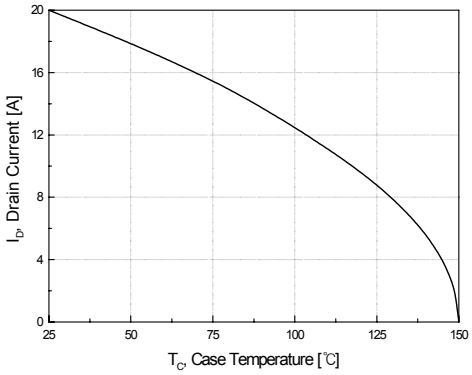


Figure 10. Maximum Drain Current vs Case Temperature

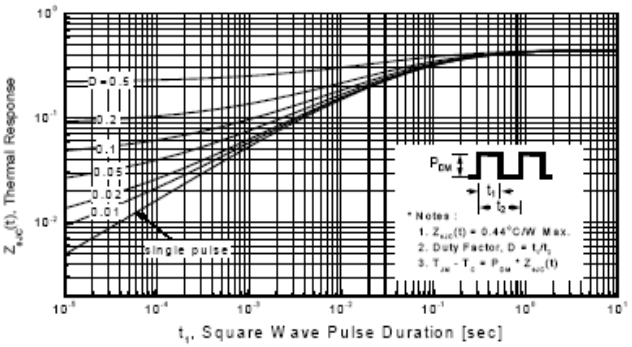
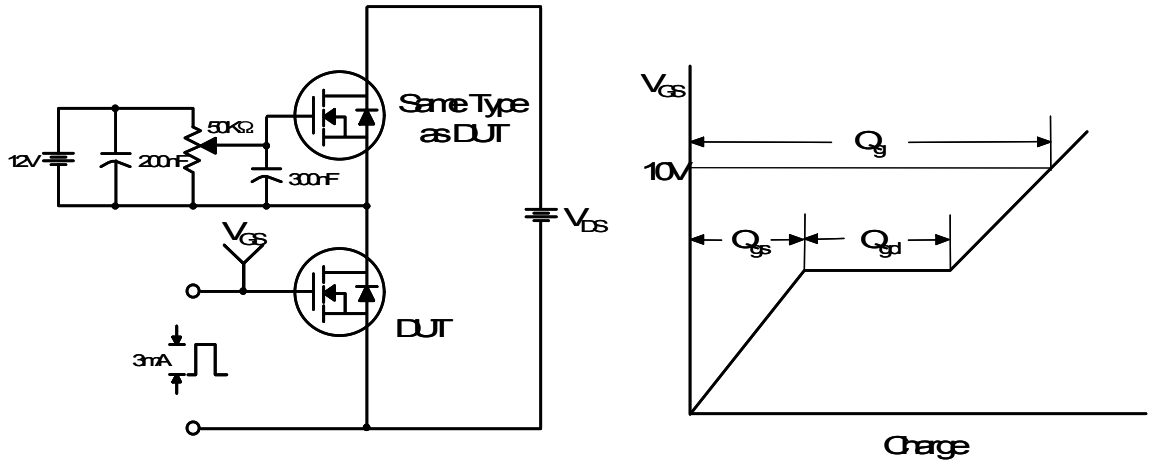
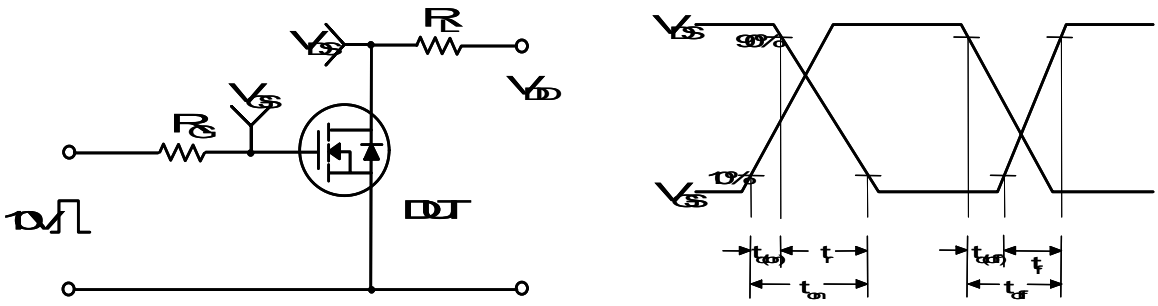


Figure 11. Transient Thermal Response Curve

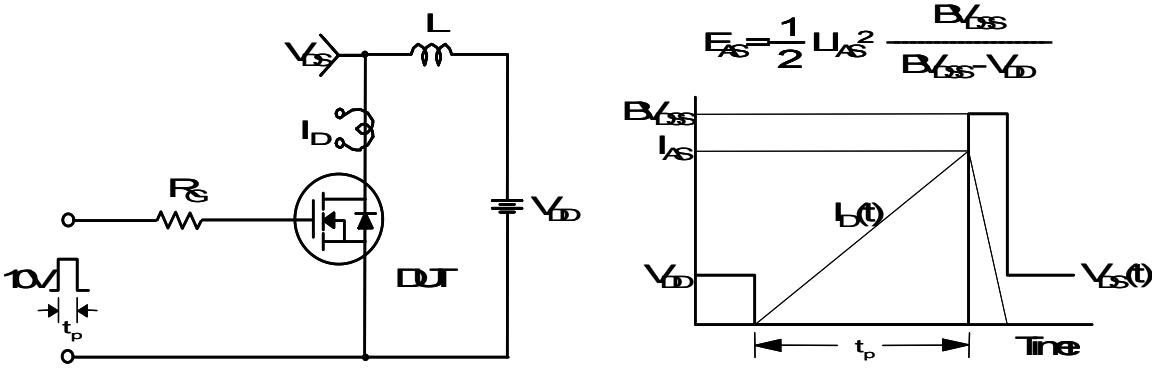
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms