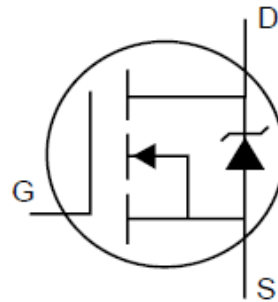
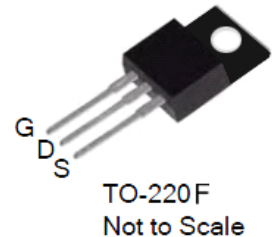
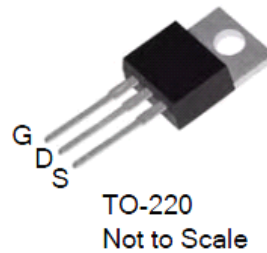


## 600V N-Channel MOSFET GENERAL DESCRIPTION

This Power MOSFET is produced using advanced planar stripe DMOS technology. This latest technology has been especially designed to minimize on-state resistance, Have a high rugged avalanche characteristics. These devices are well suited for high efficiency switched mode power supplies, active power factor correction. electronic lamp ballasts based on half bridge topology.

$V_{DSS}$	$R_{DS(ON)}$	$I_D$
600V	1.3Ω	7A



## Features

- 7A, 600V,  $R_{DS(on)} = 1.3\Omega$  @  $V_{GS} = 10V$
- Low gate charge ( typical 29nC)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

## Ordering Information

PART NUMBER	PACKAGE	BRAND
7N60/7N60F	TO-220/220F	0GFD

**Absolute Maximum Ratings**

TC = 25°C unless otherwise noted

Symbol	Parameter	7N60	7N60F	Units
V <sub>DSS</sub>	Drain-Source Voltage	600		V
I <sub>D</sub>	Drain Current - Continuous (TC = 25°C) - Continuous (TC = 100°C)	7.0	7.0	A
		4.2	4.2	A
I <sub>DM</sub>	Drain Current- Pulsed (Note 1)	28	28	A
V <sub>GSS</sub>	Gate-Source Voltage	± 30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	245		mJ
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	14.7		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P <sub>D</sub>	Power Dissipation (TC = 25°C)	147	48	W
	Derate above 25°C	1.17	0.38	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150		°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

**Thermal Characteristics**

Symbol	Parameter	7N60	7N60F	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	0.85	2.6	°C/W
R <sub>θCS</sub>	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

**Electrical Characteristics**

TC = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	600	--	--	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.7	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA

**On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.5	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A	--	1.05	1.3	Ω

**Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	1000	--	pF
C <sub>oss</sub>	Output Capacitance		--	110	--	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	12.6	--	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 7\text{ A},$ $R_G = 25\ \Omega$	--	20	--	ns
$t_r$	Turn-On Rise Time		--	50	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	80	--	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	70	--
$Q_g$	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 7\text{ A},$ $V_{GS} = 10\text{ V}$	--	29	--	nC
$Q_{gs}$	Gate-Source Charge		--	4.7	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	12.5	--

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	7.0	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	28	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 7\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 7\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	320	--	ns
$Q_{rr}$	Reverse Recovery Charge		(Note 4)	--	3.0	--

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 10\text{ mH}, I_{AS} = 7\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega,$  Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 7\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BVDSS,$  Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\mu\text{s},$  Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

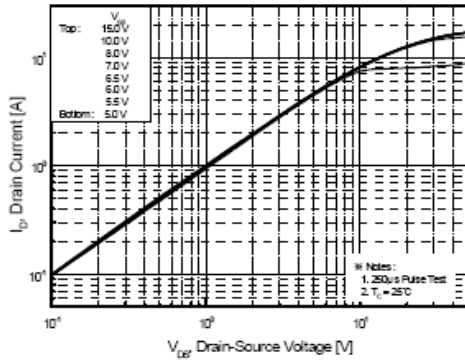


Figure 1. On-Region Characteristics

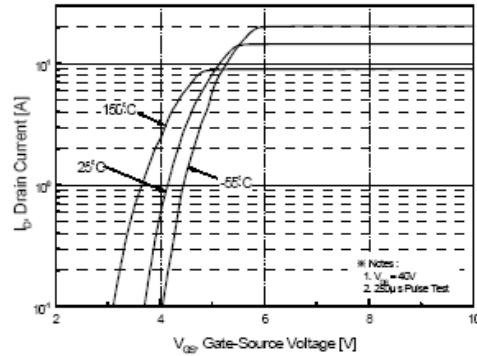


Figure 2. Transfer Characteristics

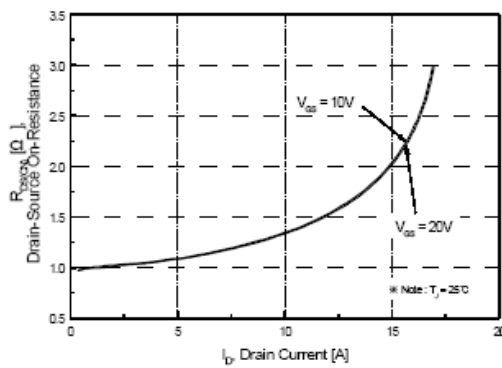


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

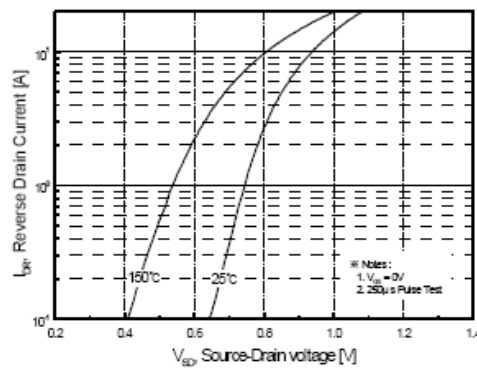


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

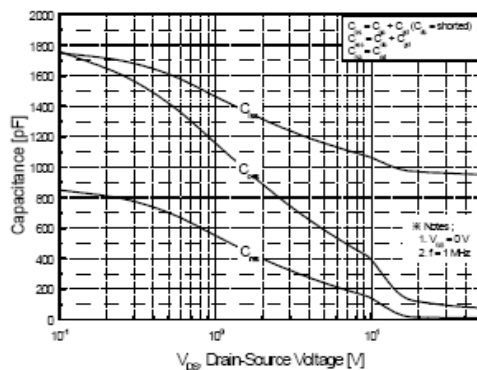


Figure 5. Capacitance Characteristics

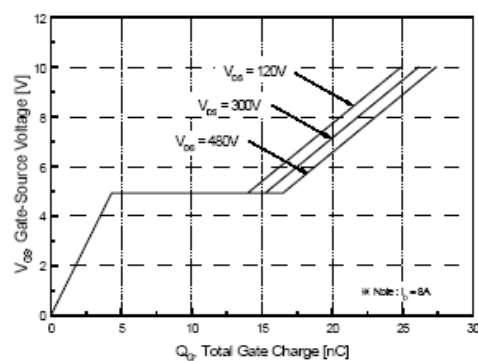


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

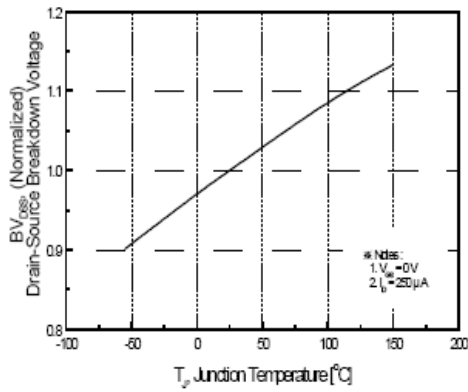


Figure 7. Breakdown Voltage Variation vs Temperature

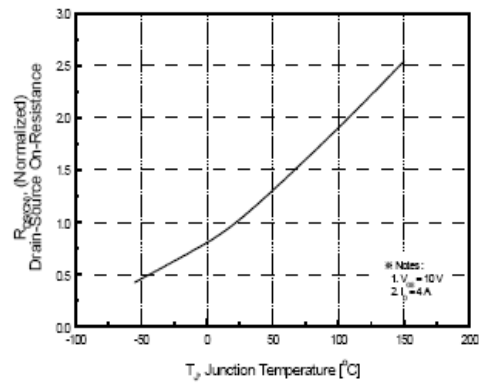


Figure 8. On-Resistance Variation vs Temperature

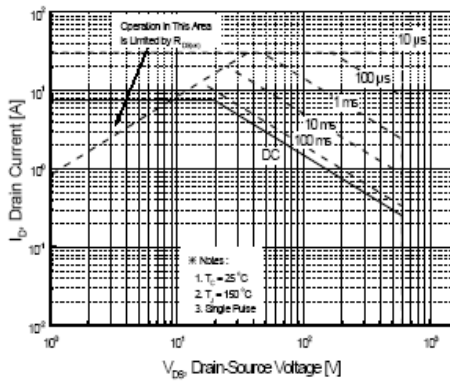


Figure 9-1. Maximum Safe Operating Area for TSP7N60M

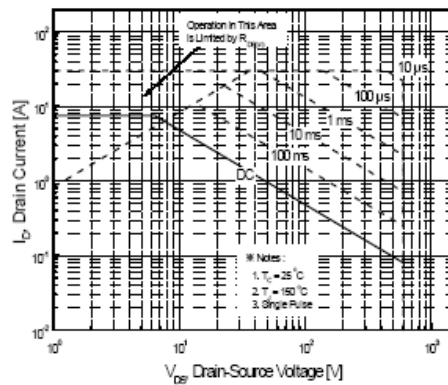


Figure 9-2. Maximum Safe Operating Area for TSF7N60M

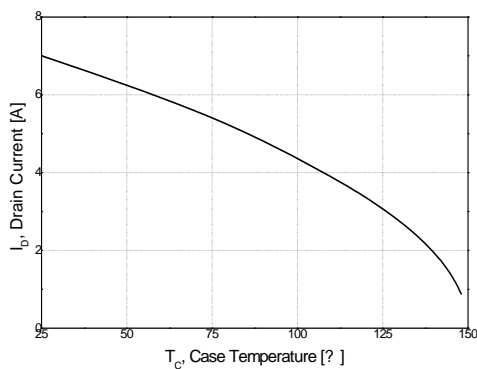


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

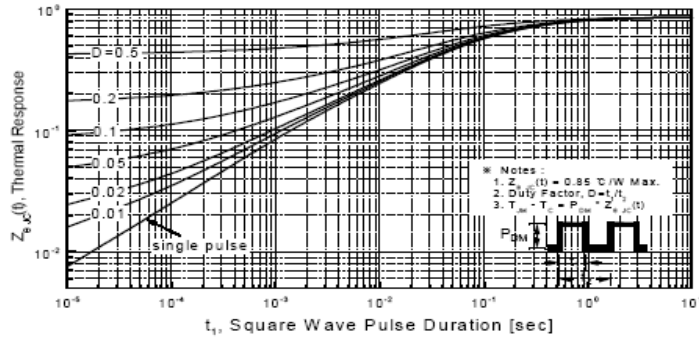


Figure 11-1. Transient Thermal Response Curve for TSP7N60M

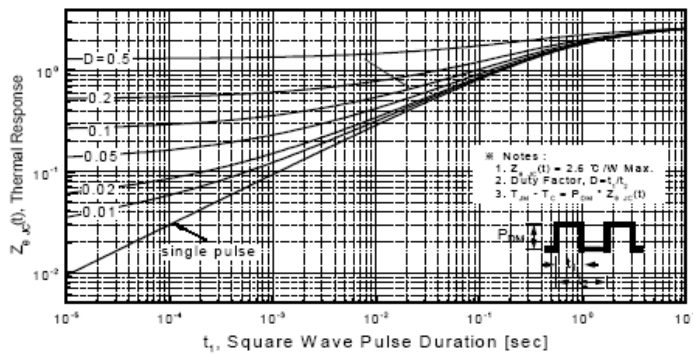
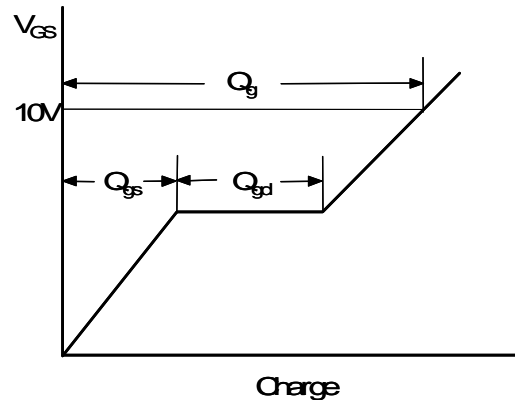
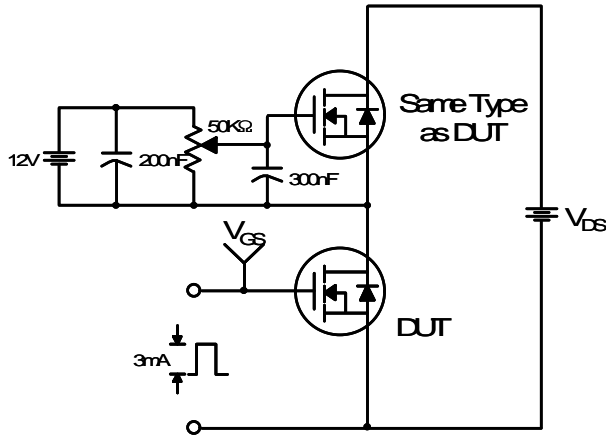
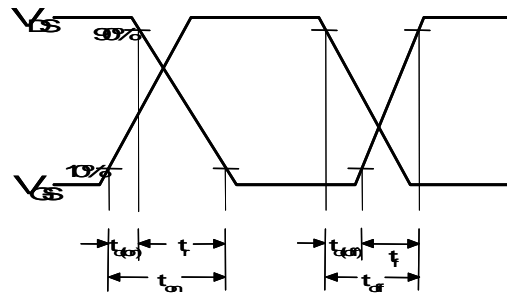
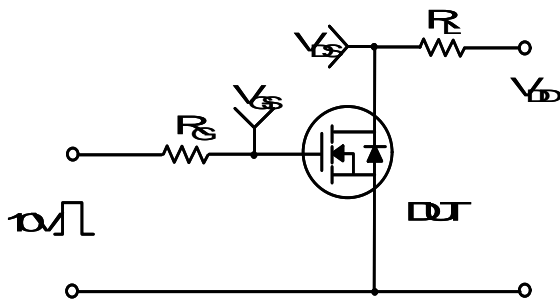


Figure 11-2. Transient Thermal Response Curve for TSF7N60M

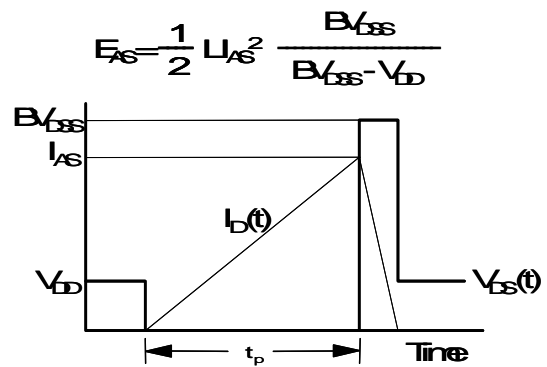
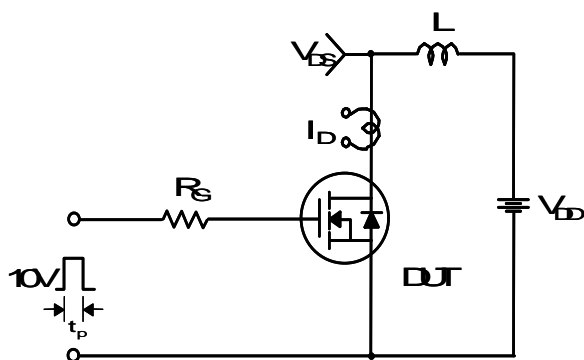
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms





Peak Diode Recovery dv/dt Test Circuit & Waveforms

