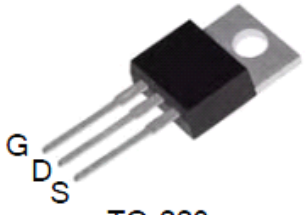
N-Channel MOSFETS

DESCRIPTION

The OGFD 1402TR uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

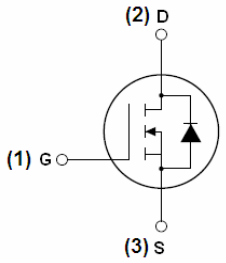
V_{DSS}	$R_{DS(ON)}$	I_D
40V	< 3.2mΩ	210A



TO-220
Not to Scale

Features:

- High density cell design for ultra low Rdson.
- Fully characterized avalanche voltage and current.
- Good stability and uniformity with high E_{AS}.
- Excellent package for good heat dissipation.
- Special process technology for high ESD capability.



Schematic diagram

Applications

- Power switching applications.
- Inverter systems
- Hard switched and high frequency circuits.
- Uninterruptible power supply systems.

Ordering Information

PART NUMBER	PACKAGE	BRAND
1402TR	TO-220	0GFD

Absolute Maximum Ratings (TC=25℃, unless otherwise noted)

Symbol	Parameter	1402TR	Units
V_{DSS}	Drain-to-Source Voltage	40	V
I_D	Continuous Drain Current	210	A
I_{DM}	Pulsed Drain Current@VG=10V	840	
P_D	Power Dissipation	310	W
	Derating Factor above 25℃	2.07	W/℃
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single PulseAvalanche Energy (L=1mH, IAS=40A)C	1800	mJ
dv/dt	Peak Diode Recovery dv/dt	5.0	V/ns
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 175	℃

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	--	--	0.48	℃/W	Water cooled heatsink, PD adjusted for a peak junction temperature of +175℃.
$R_{\theta JA}$	Junction-to-Ambient	--	--	--		1 cubic foot chamber, free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
B_{VDSS}	Drain-to-Source Breakdown Voltage	40	--	--	V	V_{GS}=0, I_D=250uA
I_{GSS}	Gate-to-Source Forward Leakage	--	--	±100	nA	V_{DS}=0V, V_{GS}=±20V
I_{DSS}	Zero Gate Voltage Drain Current	--	--	1	uA	V_{DS}=40V, V_{GS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	--	3.2	mΩ	V_{GS}=10V,I_D=40A
$V_{GS(TH)}$	Gate Threshold Voltage, Figure 12.	2.0	2.7	4.0	V	V_{DS}=10V, I_D=250uA
G_{fs}	Forward Transconductance	160	---	--	S	V_{DS}=24V, I_D=40A

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	11000	--	pF	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ
C_{oss}	Output Capacitance	--	1300	--		
C_{rss}	Reverse Transfer Capacitance	--	1000	--		
Q_g	Total Gate Charge	--	250	--	nC	V_{DS}=30V, V_{GS}=10V, I_D=30A
Q_{gs}	Gate-to-Source Charge	--	48	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	98	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$T_{d(ON)}$	Turn-on Delay Time		40		ns	V_{DD}=30V, R_L=15Ω V_{GS}=10V, R_G=2.5Ω I_D=2A
T_{rise}	Rise Time		38			
$T_{d(OFF)}$	Turn-Off Delay Time		140			
T_{fall}	Fall Time		60			

Drain-Source Diode Characteristics

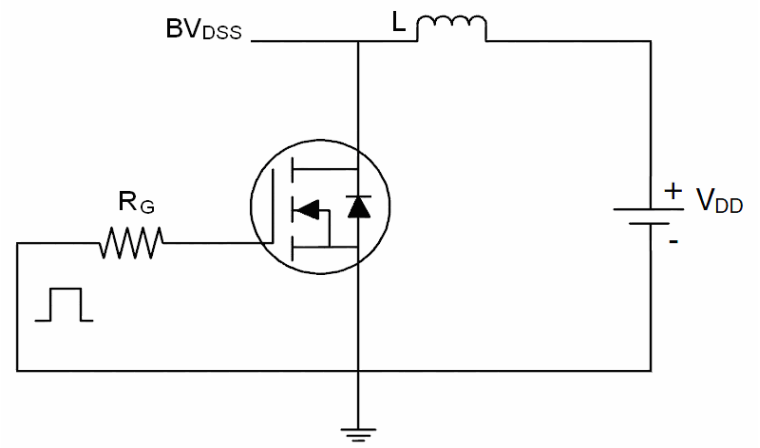
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=20A	--	0.85	1.2	V
Diode Forward Current	I_S	--	--	--	210	A
Reverse Recovery Time	t_{rr}	TJ=25℃,IF=60A Di/dt = 100 A/μs	--	48	--	nS
Reverse Recovery Charge	Q_{rr}		--	78	--	nC
Forword Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD				

Notes:

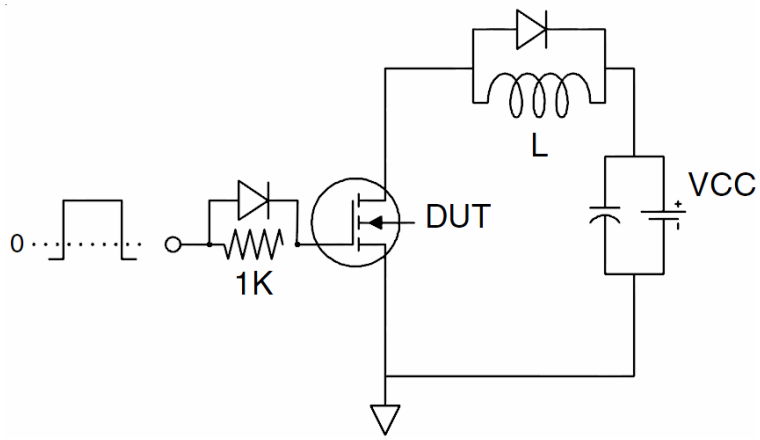
1. Repetitive Rating:Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤10 sec.
3. Pulse Test:Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production.
5. EAS condition: Tj=25℃,V_{DD}=20V,V_G=10V,L=1mH,Rg=25Ω

Test circuit

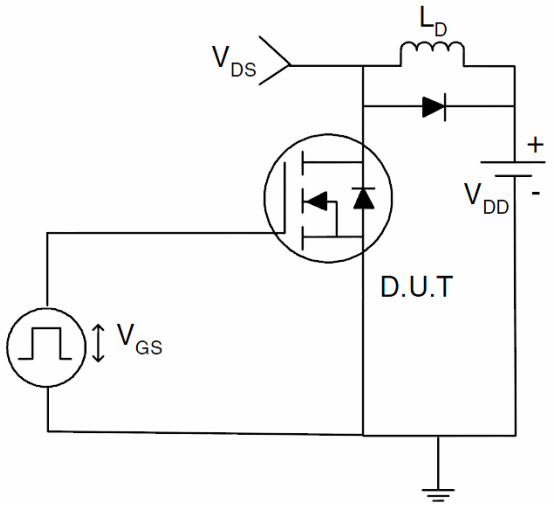
1）E_{AS} test Circuits



2）Gate charge test Circuit:

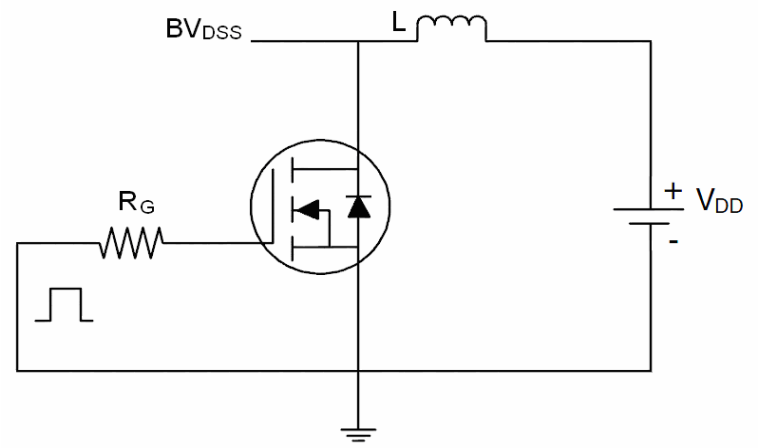


3）Switch Time Test Circuit：

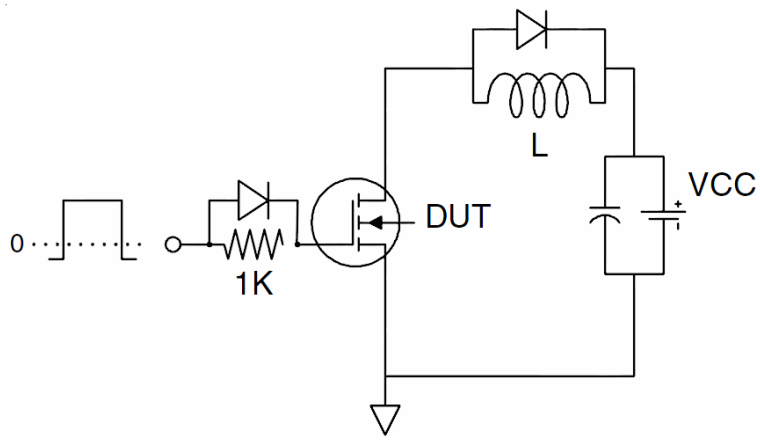


Test circuit

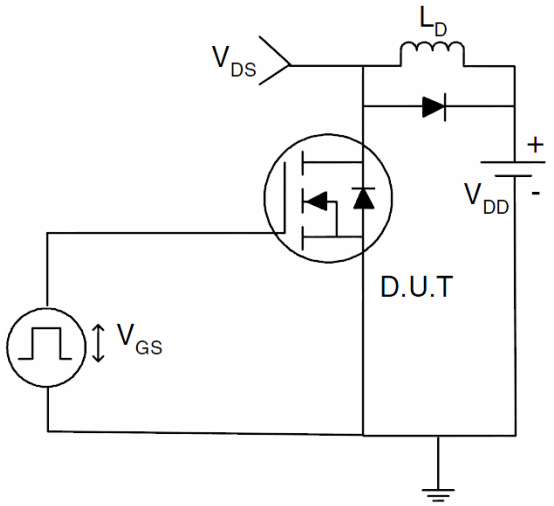
1）E_{AS} test Circuits



2）Gate charge test Circuit:



3）Switch Time Test Circuit：



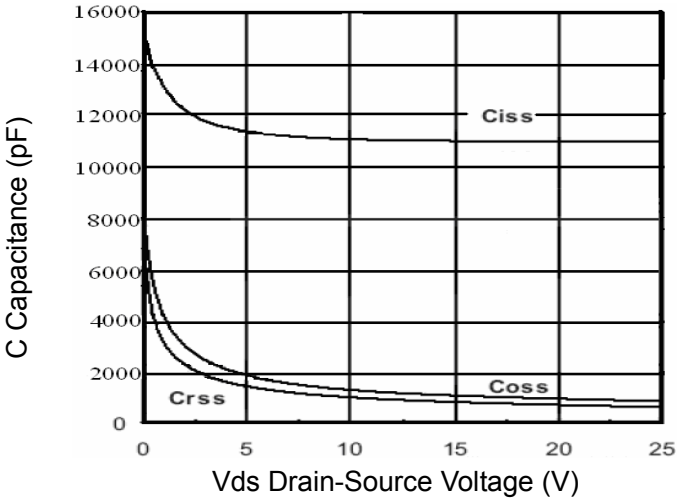


Figure 7 Capacitance vs Vds

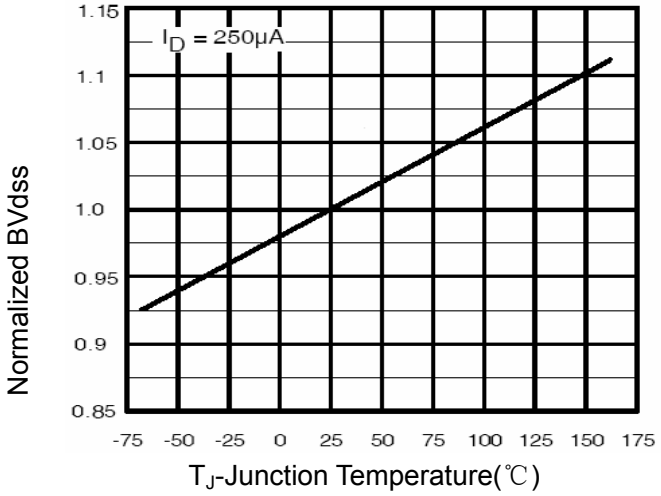


Figure 9 BV_{DSS} vs Junction Temperature

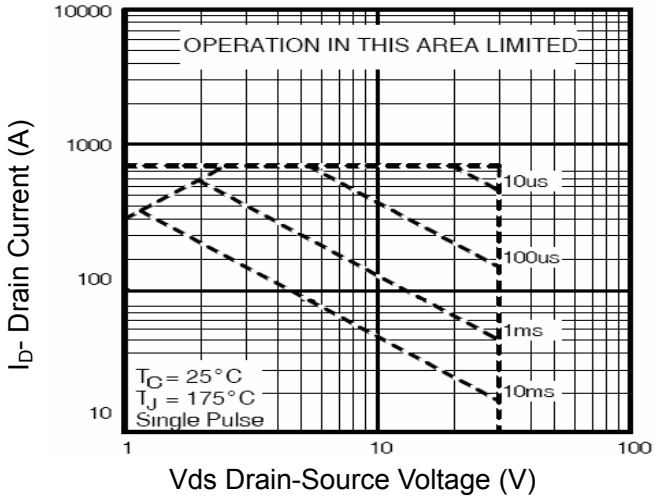


Figure 8 Safe Operation Area

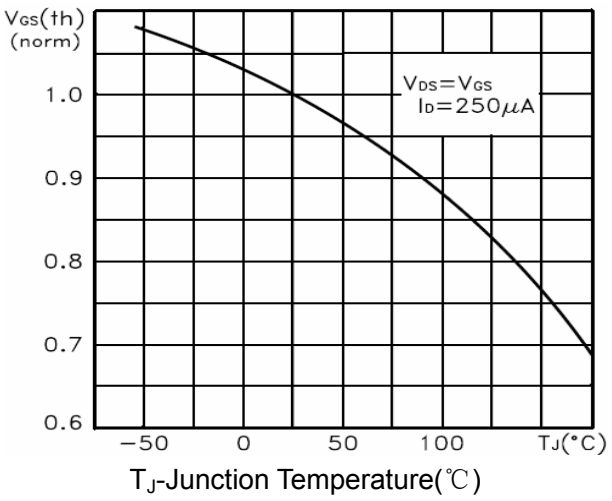


Figure 10 $V_{GS(th)}$ vs Junction Temperatur

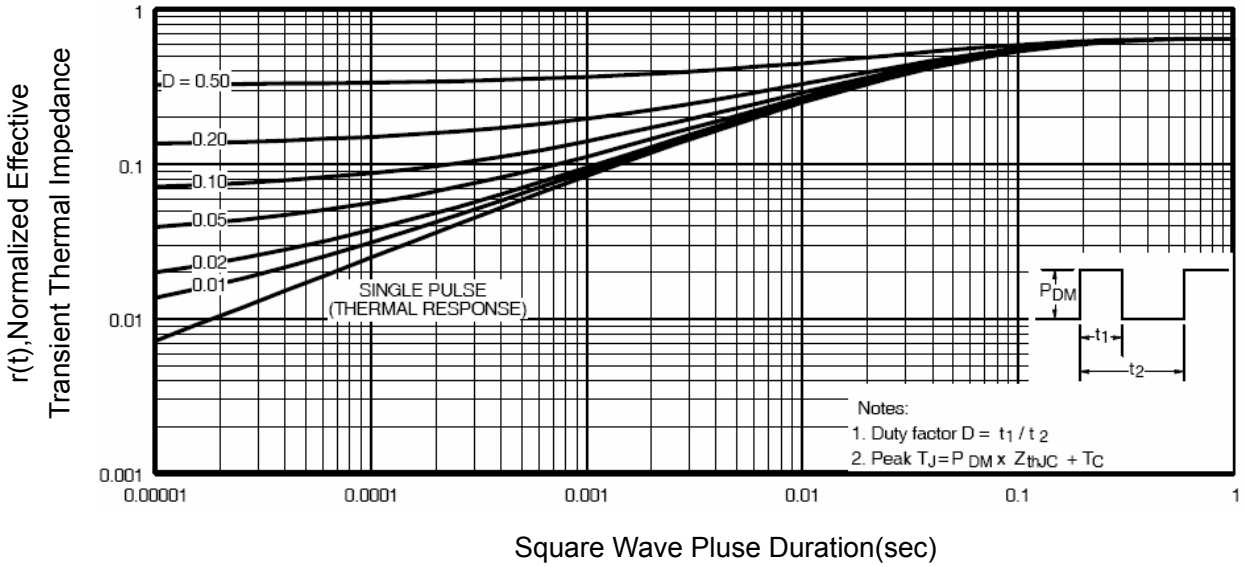


Figure 11 Normalized Maximum Transient Thermal Impedance