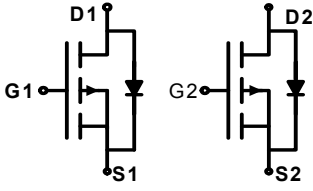
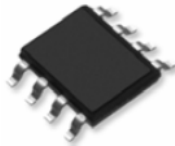


<p><b>Description</b></p> <p>The 4953 uses advanced trench technology to provide excellent <math>R_{DS(ON)}</math>, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a load switch or in PWM applications.</p> <p><b>General Features</b></p> <ul style="list-style-type: none"> <li>● <math>V_{DS} = -30V, I_D = -5.1A</math></li> <li>● <math>R_{DS(ON)} &lt; 105m\Omega @ V_{GS} = -4.5V</math></li> <li>● <math>R_{DS(ON)} &lt; 55m\Omega @ V_{GS} = -10V</math></li> <li>● High Power and current handing capability</li> <li>● Lead free product is acquired</li> <li>● Surface Mount Package</li> </ul> <p><b>Application</b></p> <ul style="list-style-type: none"> <li>● PWM applications</li> <li>● Load switch</li> <li>● Power management</li> </ul>	<div style="text-align: center;">  <p><b>Schematic diagram</b></p> </div> <div style="text-align: center; margin-top: 20px;">  <p><b>SOP-8 top view</b></p> </div>
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**Absolute Maximum Ratings ( $T_A=25^{\circ}C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-5.1	A
Drain Current-Pulsed (Note 1)	$I_{DM}$	-20	A
Maximum Power Dissipation	$P_D$	2.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^{\circ}C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	$^{\circ}C/W$
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**Electrical Characteristics ( $T_A=25^{\circ}C$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-33	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$	-	-	-1	$\mu A$

Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.6	-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-5.1A$	-	48	55	m $\Omega$
		$V_{GS}=-4.5V, I_D=-4.2A$	-	73	105	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-15V, I_D=-4.5A$	4	7	-	S
<b>Dynamic Characteristics</b> (Note4)						
Input Capacitance	$C_{ISS}$	$V_{DS}=-15V, V_{GS}=0V,$ $F=1.0MHz$	-	520	-	PF
Output Capacitance	$C_{OSS}$		-	130	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	70	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-1A,$ $V_{GS}=-10V, R_{GEN}=6\Omega$	-	7	-	nS
Turn-on Rise Time	$t_r$		-	13	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	14	-	nS
Turn-Off Fall Time	$t_f$		-	9	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-15V, I_D=-5.1A, V_{GS}=-10V$	-	12	-	nC
Gate-Source Charge	$Q_{gs}$		-	2.2	-	nC
Gate-Drain Charge	$Q_{gd}$		-	3	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=-1.7A$	-	-	-1.2	V

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

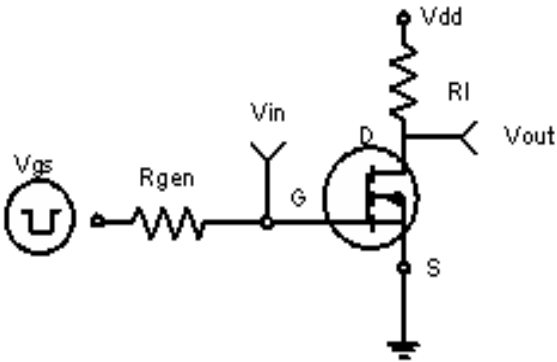


Figure 1: Switching Test Circuit

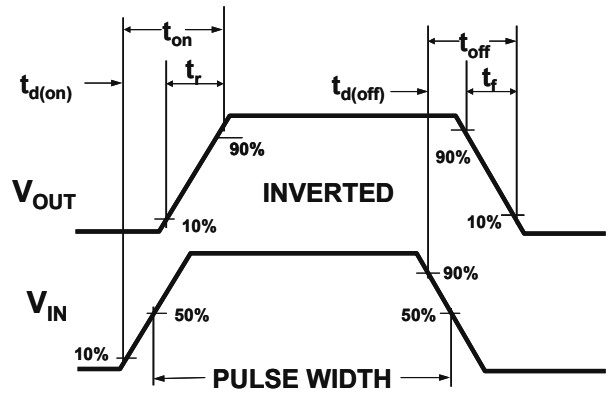


Figure 2: Switching Waveforms

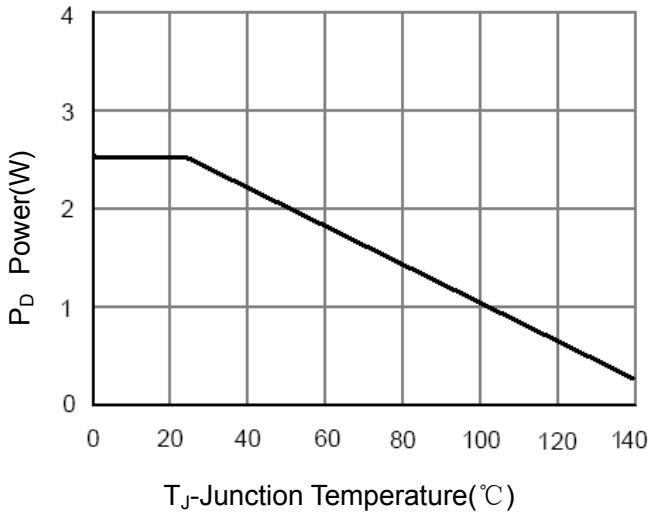


Figure 3 Power Dissipation

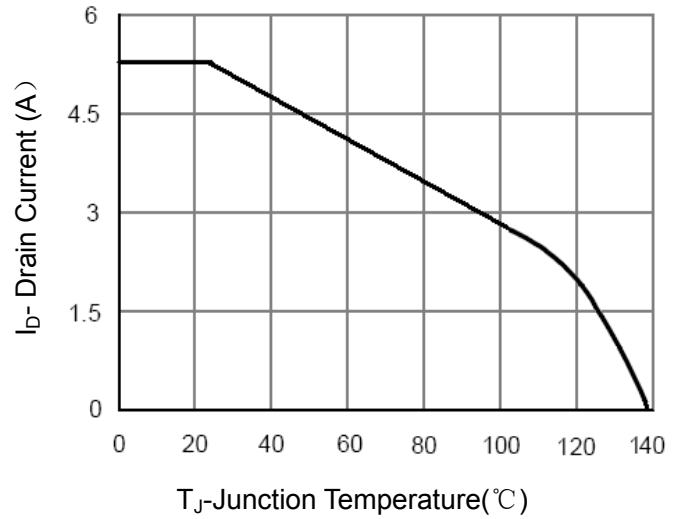


Figure 4 Drain Current

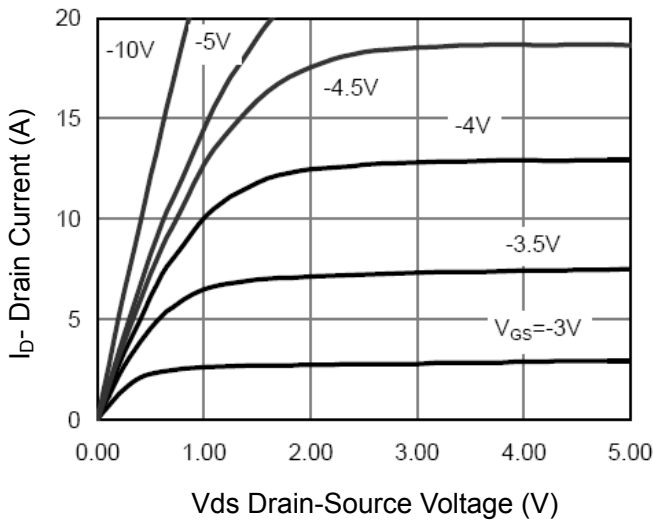


Figure 5 Output Characteristics

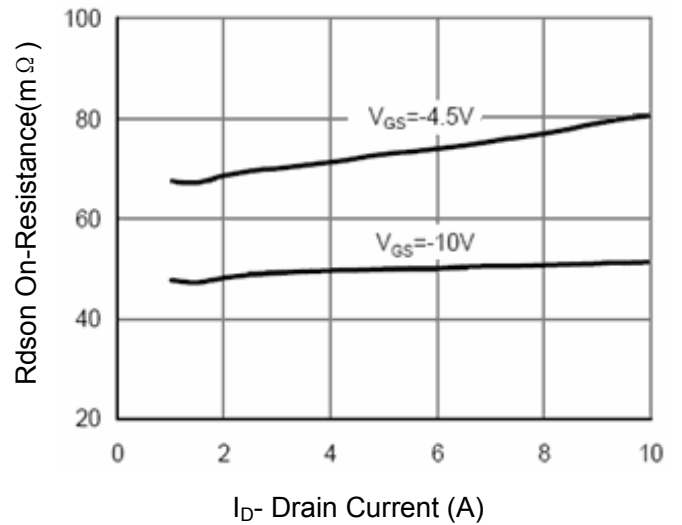
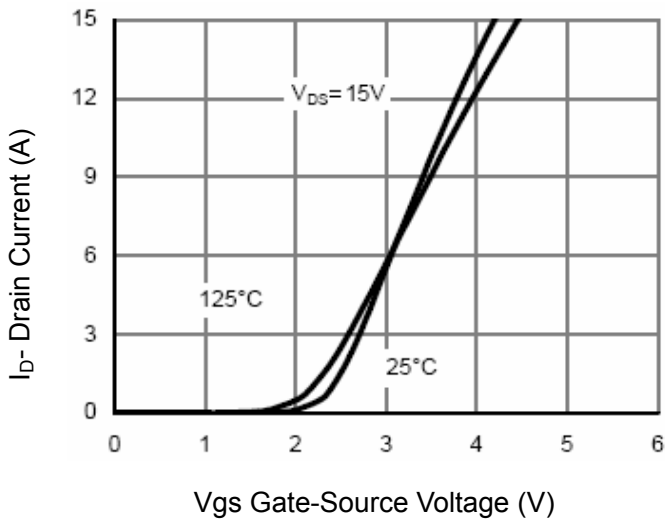
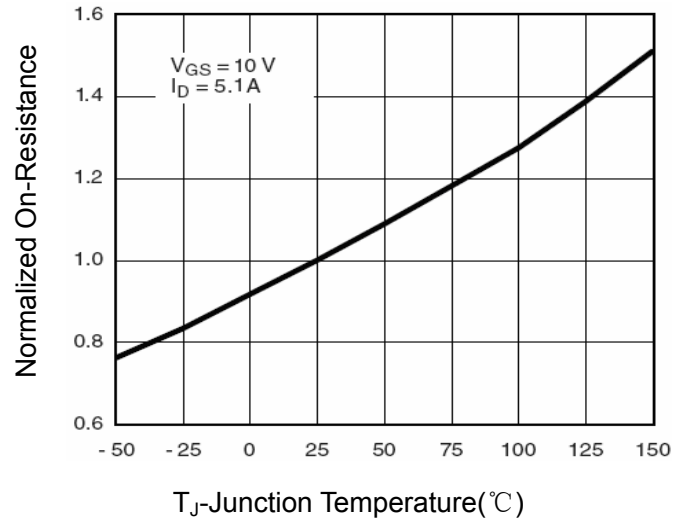


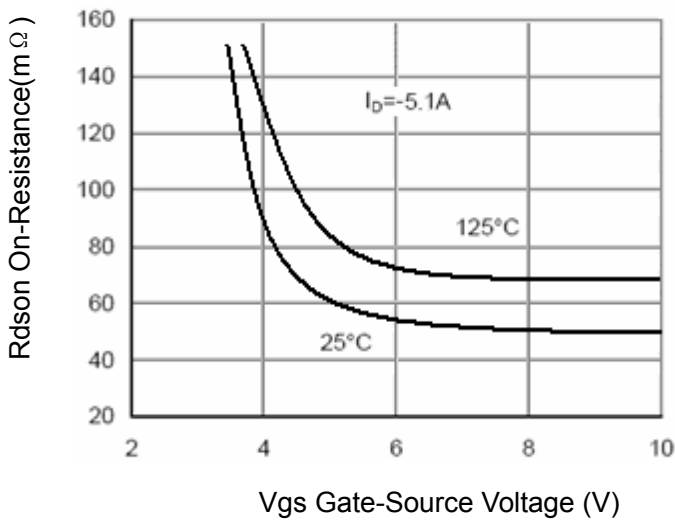
Figure 6 Drain-Source On-Resistance



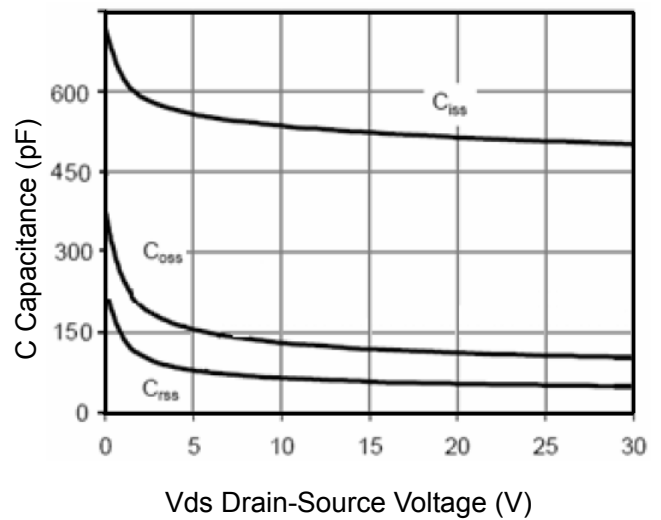
Vgs Gate-Source Voltage (V)  
**Figure 7 Transfer Characteristics**



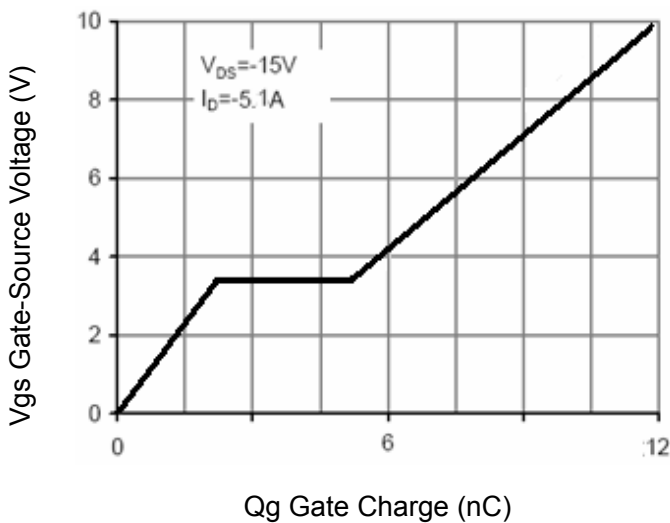
T<sub>J</sub>-Junction Temperature(°C)  
**Figure 8 Drain-Source On-Resistance**



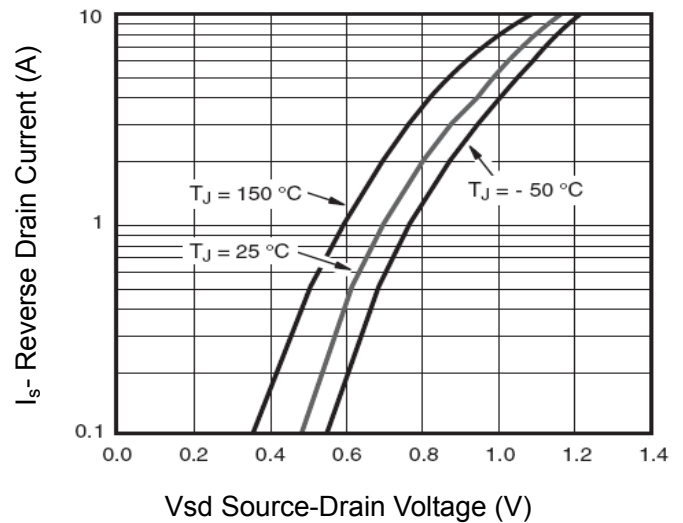
Vgs Gate-Source Voltage (V)  
**Figure 9 Rdson vs Vgs**



Vds Drain-Source Voltage (V)  
**Figure 10 Capacitance vs Vds**



Qg Gate Charge (nC)  
**Figure 11 Gate Charge**



Vsd Source-Drain Voltage (V)  
**Figure 12 Source- Drain Diode Forward**

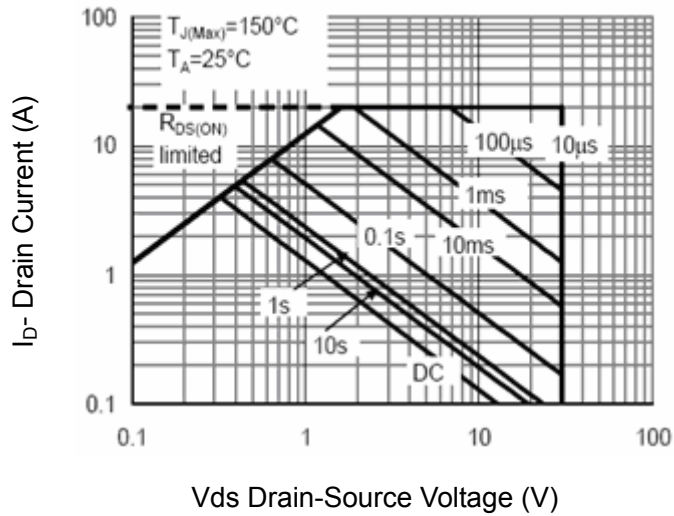


Figure 13 Safe Operation Area

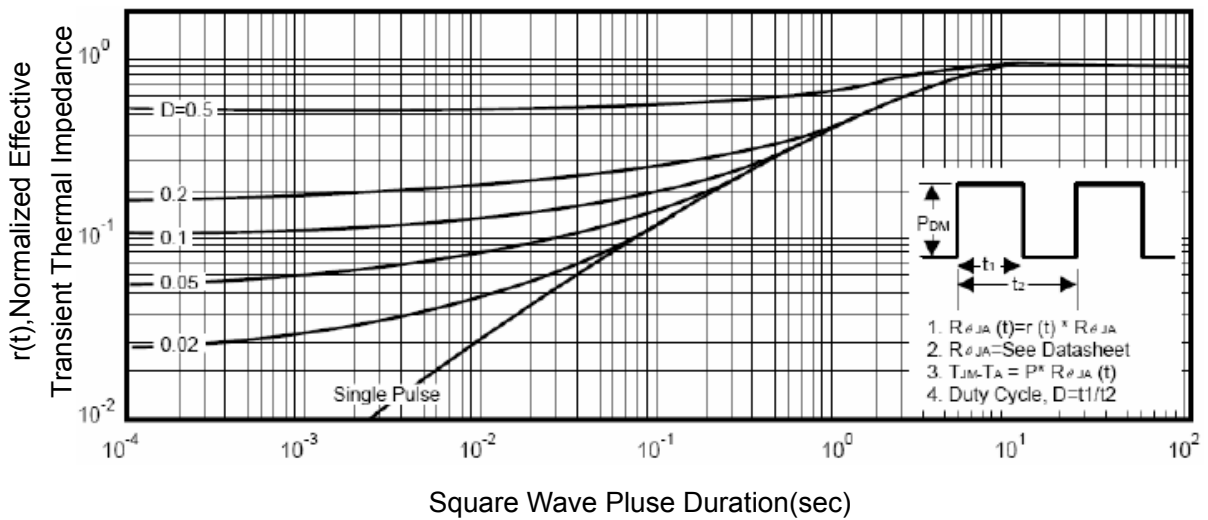


Figure 14 Normalized Maximum Transient Thermal Impedance