

## FDG6301N\_F085 Dual N-Channel, Digital FET

### General Description

These dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs.



### Features

- 25 V, 0.22 A continuous, 0.65 A peak.  
 $R_{DS(ON)} = 4 \Omega @ V_{GS} = 4.5 \text{ V}$ ,  
 $R_{DS(ON)} = 5 \Omega @ V_{GS} = 2.7 \text{ V}$ .
- Very low level gate drive requirements allowing direct operation in 3 V circuits ( $V_{GS(th)} < 1.5 \text{ V}$ ).
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).
- Compact industry standard SC70-6 surface mount package.
- Qualified to AEC Q101
- RoHS Compliant



SC70-6

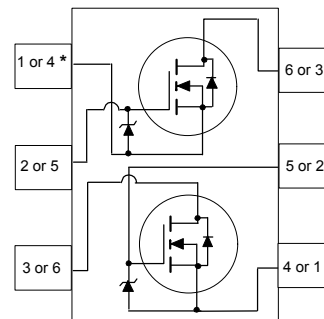
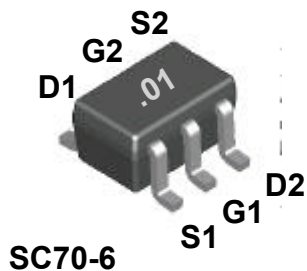
SOT-23

SuperSOT™-6

SuperSOT™-8

SO-8

SOT-223



\* The pinouts are symmetrical; pin 1 and 4 are interchangeable.

Units inside the carrier can be of either orientation and will not affect the functionality of the device.

### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDG6301N_F085	Units
$V_{DSS}$	Drain-Source Voltage	25	V
$V_{GSS}$	Gate-Source Voltage	8	V
$I_D$	Drain/Output Current	- Continuous	0.22
		- Pulsed	0.65
$P_D$	Maximum Power Dissipation (Note 1)	0.3	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model(100 pF / 1500 $\Omega$ )	6.0	kV

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	415	$^\circ\text{C/W}$
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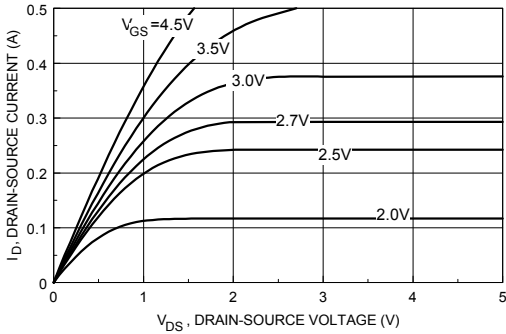
**Electrical Characteristics** ( $T_A = 25\text{ }^\circ\text{C}$  unless otherwise noted )

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		25		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
					10	$\mu\text{A}$
$I_{GSS}$	Gate - Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.65	0.85	1.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		-2.1		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 0.22\text{ A}$		2.6	4	$\Omega$
				5.3	7	
			$T_J = 125\text{ }^\circ\text{C}$	3.7	5	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	0.22			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 0.22\text{ A}$		0.2		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		9.5		pF
$C_{oss}$	Output Capacitance			6		pF
$C_{rss}$	Reverse Transfer Capacitance			1.3		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 5\text{ V}, I_D = 0.5\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 50\text{ }\Omega$		5	10	ns
$t_r$	Turn - On Rise Time			4.5	10	ns
$t_{D(off)}$	Turn - Off Delay Time			4	8	ns
$t_f$	Turn - Off Fall Time			3.2	7	ns
$Q_g$	Total Gate Charge			0.29	0.4	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS} = 5\text{ V}, I_D = 0.22\text{ A},$ $V_{GS} = 4.5\text{ V}$		0.12		nC
$Q_{gd}$	Gate-Drain Charge			0.03		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Source Current				0.25	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.25\text{ A}$ (Note 2)		0.8	1.2	V

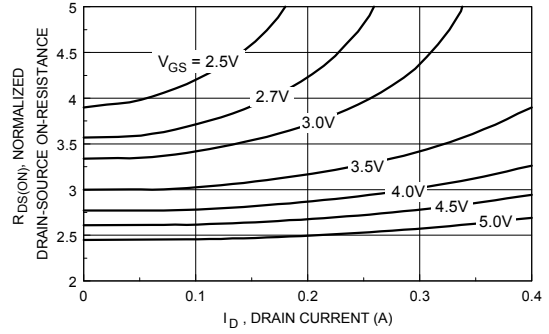
## Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.  $R_{\theta JA} = 415\text{ }^\circ\text{C/W}$  on minimum pad mounting on FR-4 board in still air.
- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

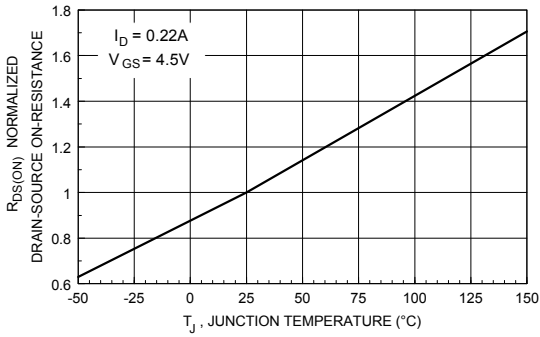
**Typical Electrical Characteristics**



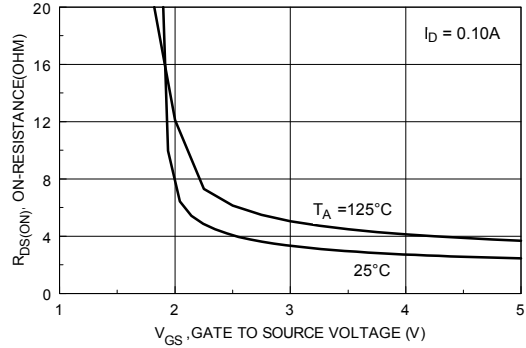
**Figure 1. On-Region Characteristics.**



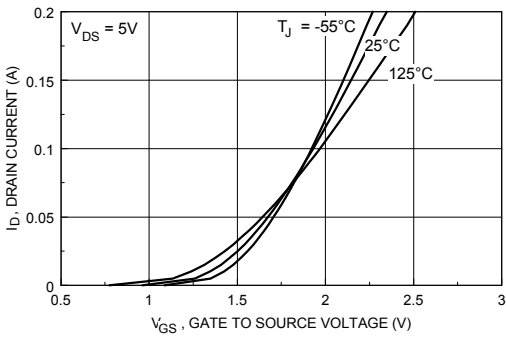
**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**



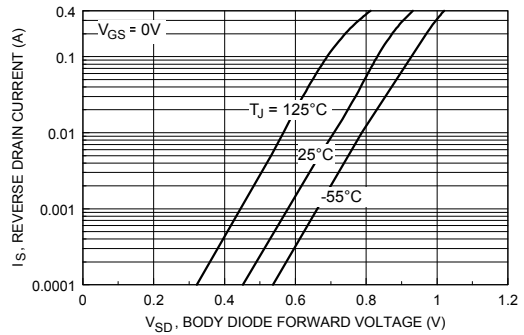
**Figure 3. On-Resistance Variation with Temperature.**



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

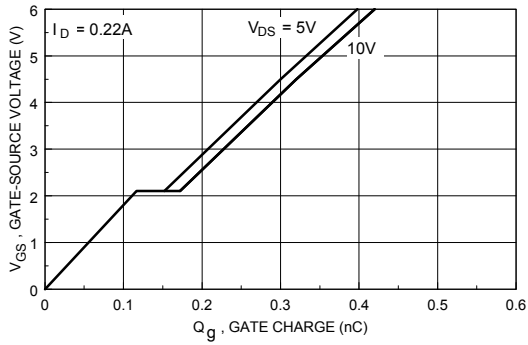


**Figure 5. Transfer Characteristics.**

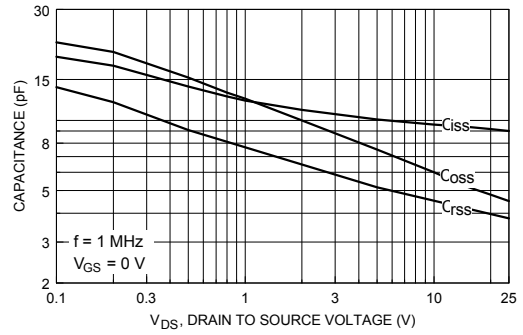


**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

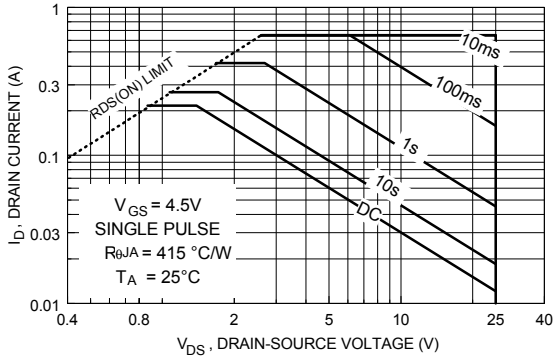
**Typical Electrical Characteristics ( continued)**



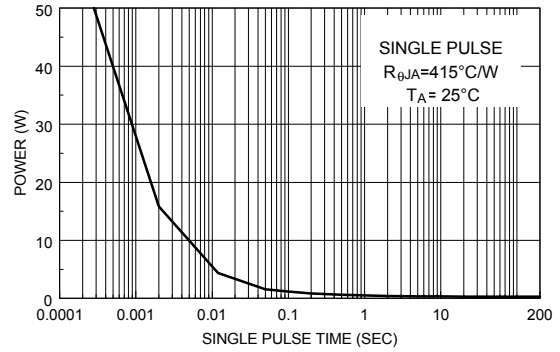
**Figure 7. Gate Charge Characteristics.**



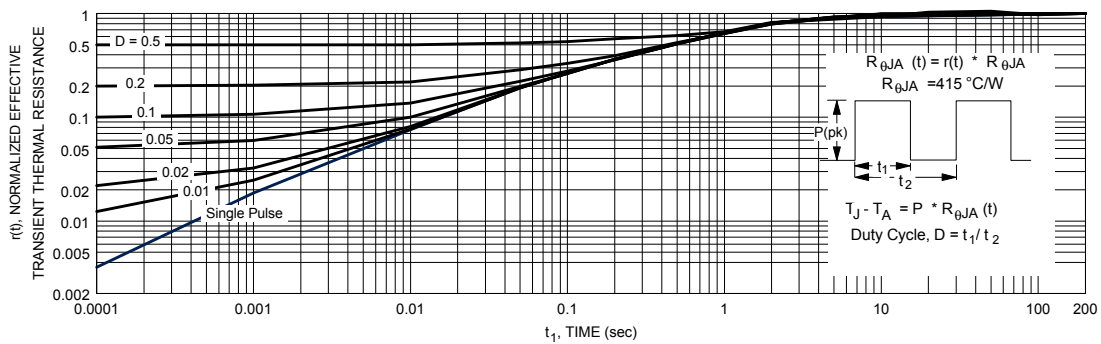
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**









**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in note 1.  
Transient thermal response will change depending on the circuit board design.



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