

Designer's™ Data Sheet

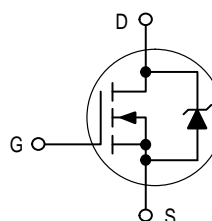
TMOS E-FET™

High Energy Power FET

N-Channel Enhancement-Mode Silicon Gate

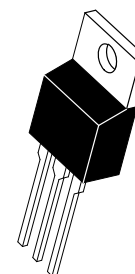
This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



MTP10N40E

TMOS POWER FET
10 AMPERES
400 VOLTS
R_{DS(on)} = 0.55 OHMS



CASE 221A-06, Style 5
TO-220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	400	Vdc
Drain-Gate Voltage (R _{GS} = 1.0 MΩ)	V _{DGR}	400	Vdc
Gate-Source Voltage — Continuous	V _{GS}	±20	Vdc
— Non-repetitive	V _{GSM}	±40	Vpk
Drain Current — Continuous	I _D	10	Adc
— Pulsed	I _{DM}	40	
Total Power Dissipation	P _D	125	Watts
Derate above 25°C		1.0	W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-65 to 150	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain-to-Source Avalanche Energy — T _J = 25°C	W _{DSR(1)}	520	mJ
— T _J = 100°C		83	
Repetitive Pulse Drain-to-Source Avalanche Energy	W _{DSR(2)}	13	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _{θJC}	1.0	°C/W
— Junction to Ambient	R _{θJA}	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	275	°C

(1) V_{DD} = 50 V, I_D = 10 A

(2) Pulse Width and frequency is limited by T_{J(max)} and thermal response

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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MTP10N40E

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	V _{(BR)DSS}	400	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 400 V, V _{GS} = 0) (V _{DS} = 320 V, V _{GS} = 0, T _J = 125°C)	I _{DSS}	— —	— —	0.25 1.0	mAdc
Gate-Body Leakage Current — Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)	I _{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)	I _{GSSR}	—	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mAdc) (T _J = 125°C)	V _{GS(th)}	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 5.0 A)	R _{DS(on)}	—	0.4	0.55	Ohms
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc) (I _D = 5.0 A) (I _D = 2.5 A, T _J = 100°C)	V _{DS(on)}	— —	— —	6.0 4.75	Vdc
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 5.0 A)	g _{FS}	4.0	—	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C _{iSS}	—	1570	—	pF
Output Capacitance		C _{oSS}	—	230	—	
Transfer Capacitance		C _{rSS}	—	55	—	

SWITCHING CHARACTERISTICS*

Turn-On Delay Time	(V _{DD} = 200 V, I _D ≈ 10 A, R _L = 20 Ω, R _G = 9.1 Ω, V _{GS(on)} = 10 V)	t _{d(on)}	—	25	—	ns
Rise Time		t _r	—	37	—	
Turn-Off Delay Time		t _{d(off)}	—	75	—	
Fall Time		t _f	—	31	—	
Total Gate Charge	(V _{DS} = 320 V, I _D = 10 A, V _{GS} = 10 V)	Q _g	—	46	63	nC
Gate-Source Charge		Q _{gs}	—	10	—	
Gate-Drain Charge		Q _{gd}	—	23	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 10 A, di/dt = 100 A/μs)	V _{SD}	—	—	2.0	Vdc
Forward Turn-On Time		t _{on}	—	**	—	ns
Reverse Recovery Time		t _{rr}	—	250	—	

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _s	—	7.5	—	nH

* Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

** Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

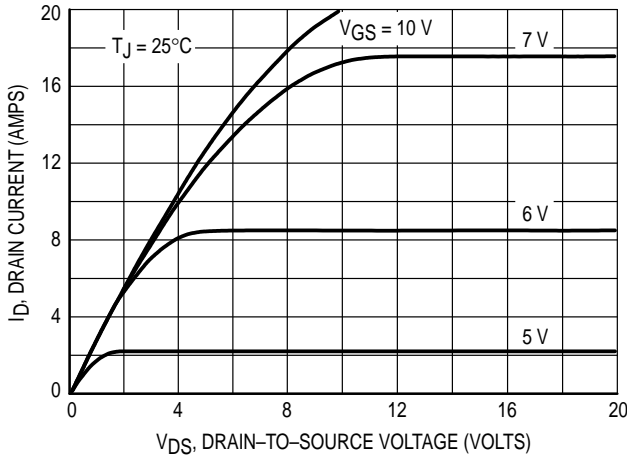


Figure 1. On-Region Characteristics

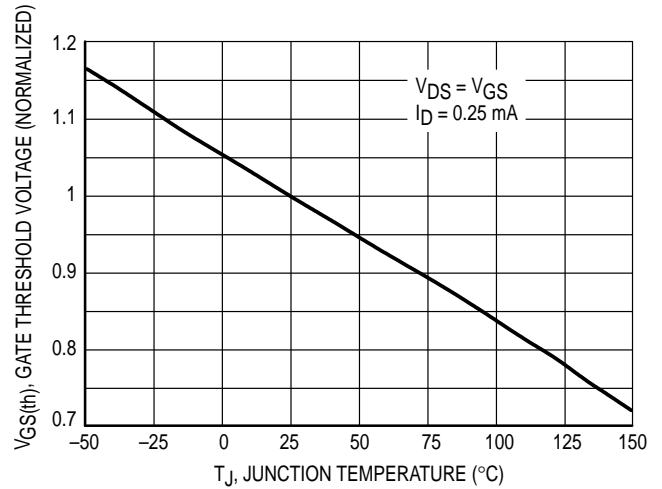


Figure 2. Gate-Threshold Voltage Variation With Temperature

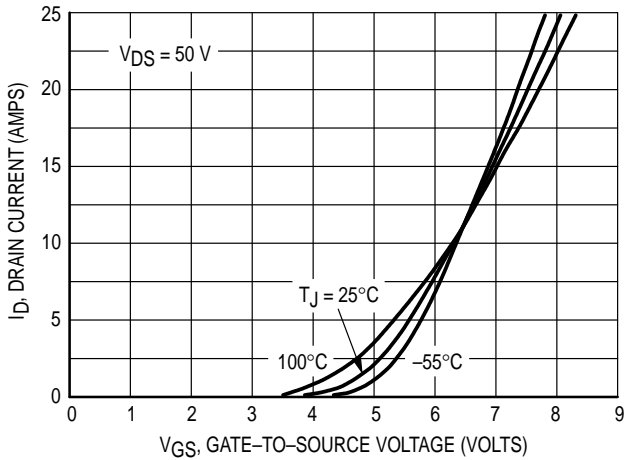


Figure 3. Transfer Characteristics

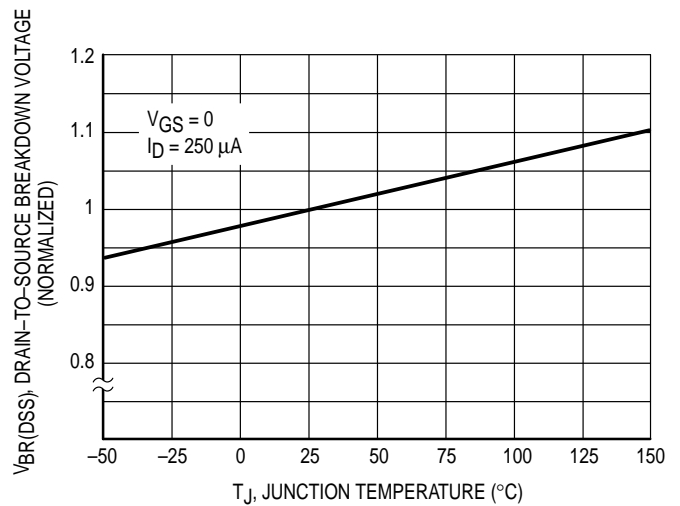


Figure 4. Breakdown Voltage Variation With Temperature

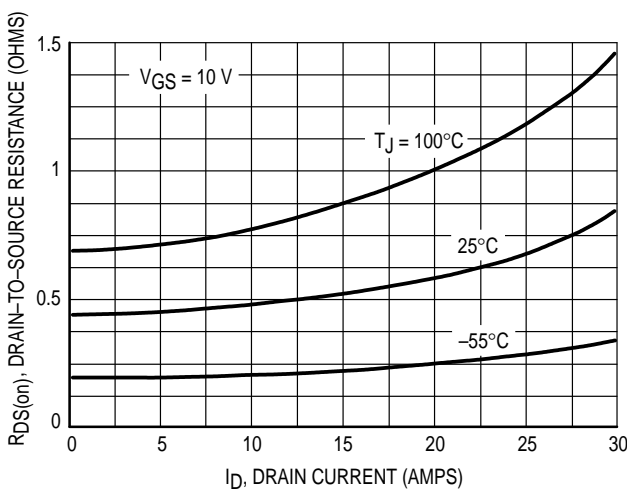


Figure 5. On-Resistance versus Drain Current

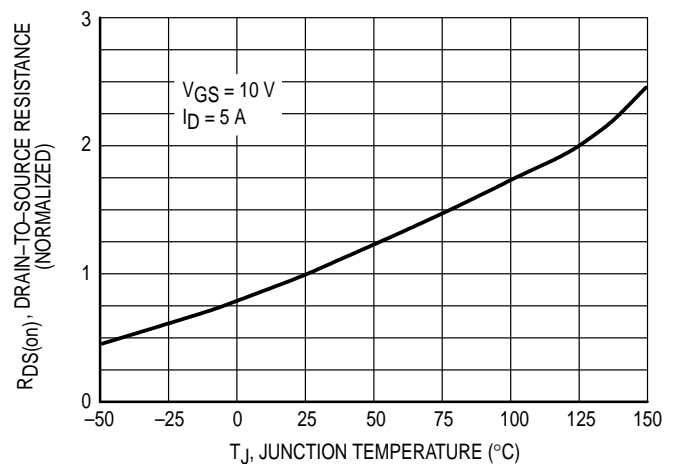


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

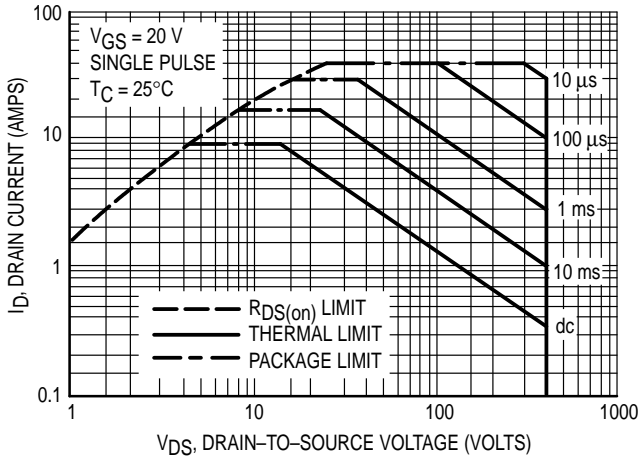


Figure 7. Maximum Rated Forward Biased Safe Operating Area

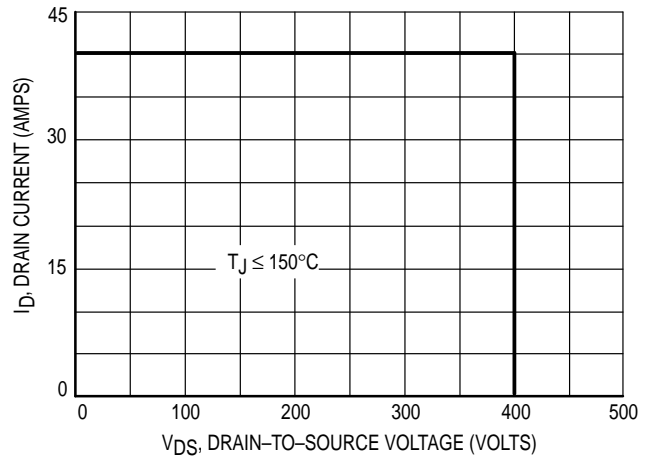


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance—General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V(BR)_{DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_J(max) - T_C}{R_{\theta JC}}$$

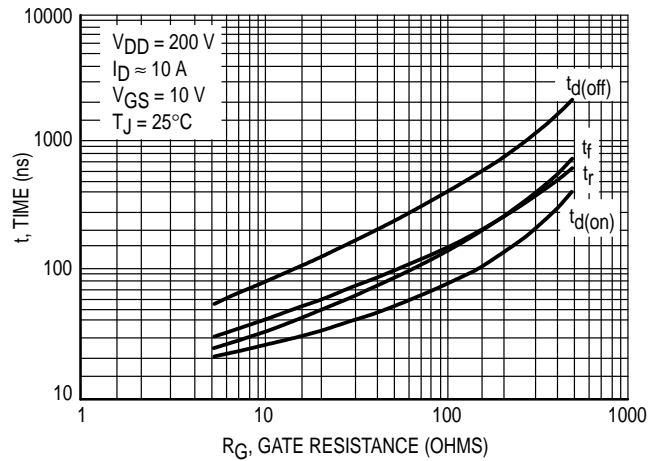


Figure 9. Resistive Switching Time Variation versus Gate Resistance

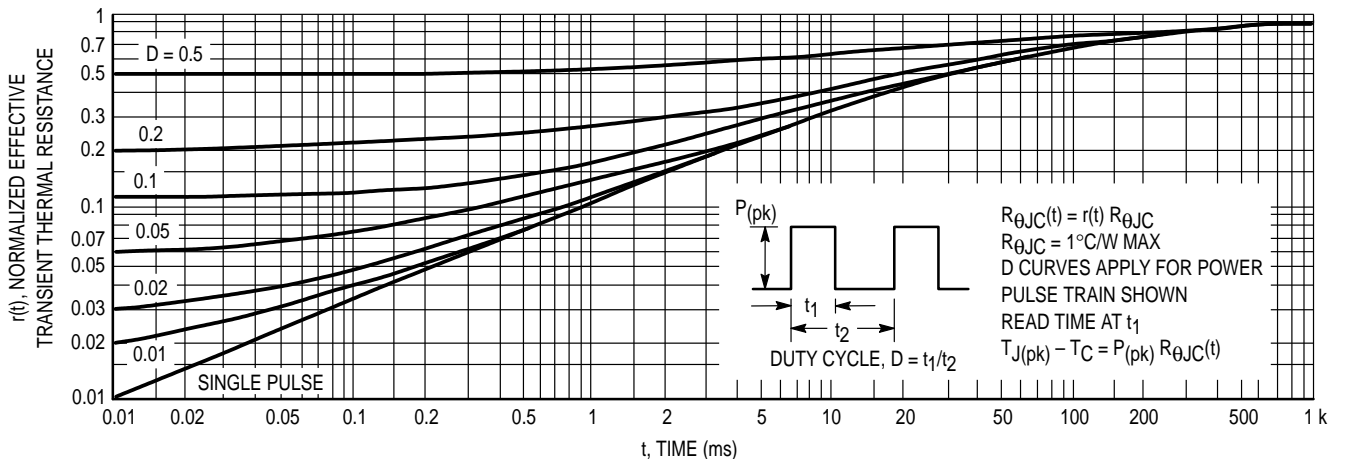


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM} , peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{frr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

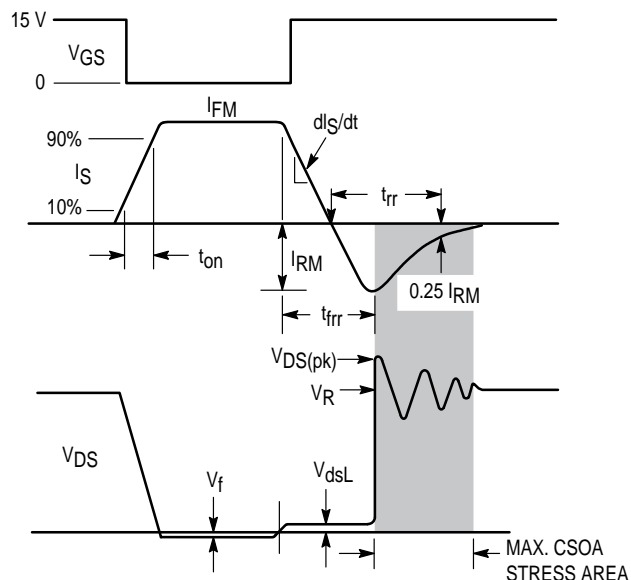


Figure 11. Commutating Waveforms

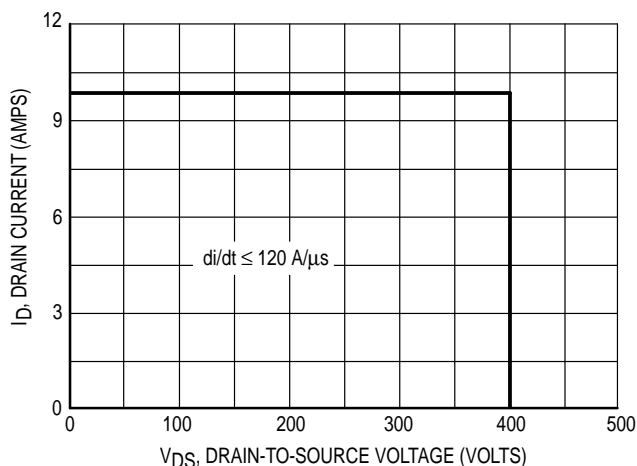


Figure 12. Commutating Safe Operating Area (CSOA)

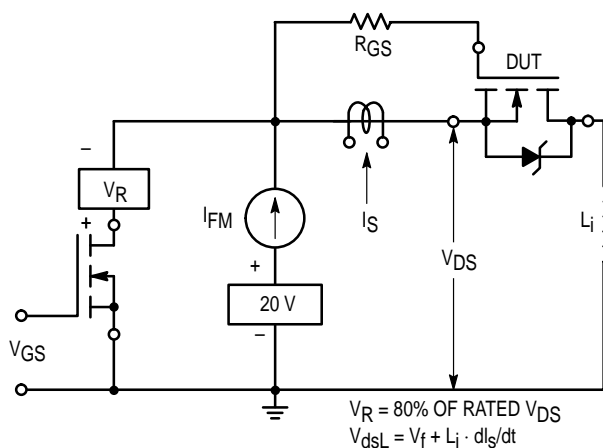


Figure 13. Commutating Safe Operating Area Test Circuit

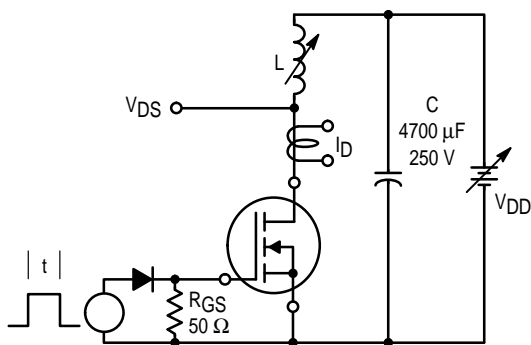


Figure 14. Unclamped Inductive Switching Test Circuit

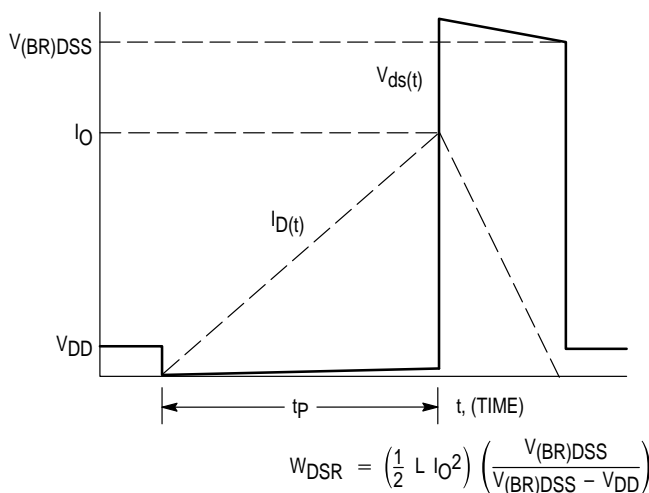


Figure 15. Unclamped Inductive Switching Waveforms

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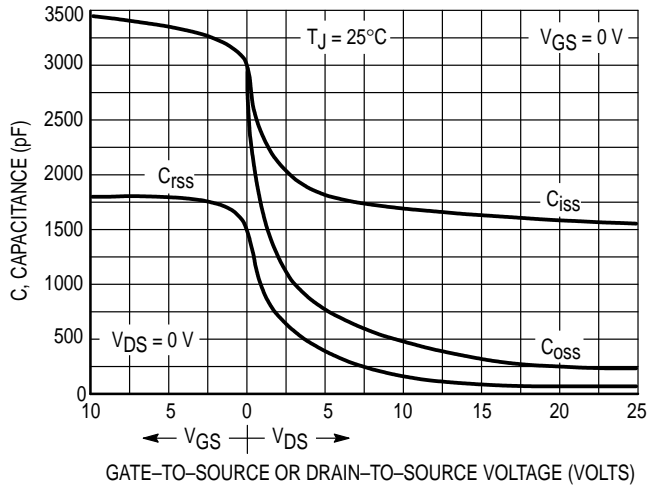


Figure 16. Capacitance Variation

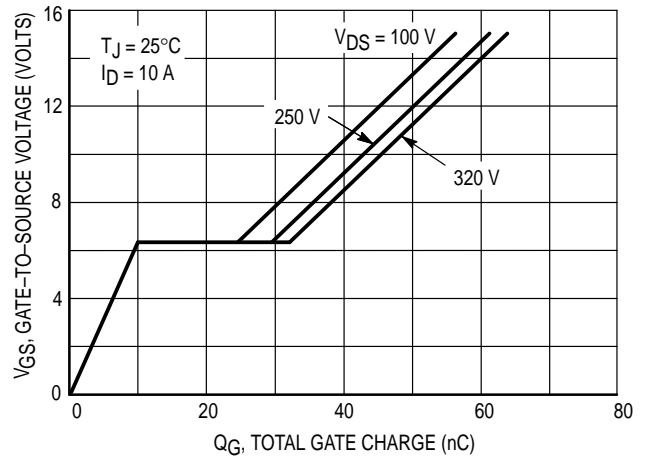
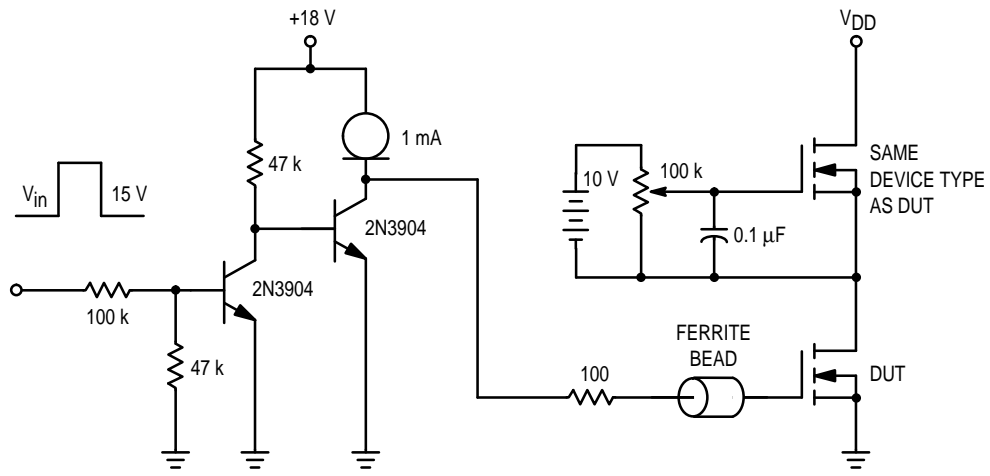


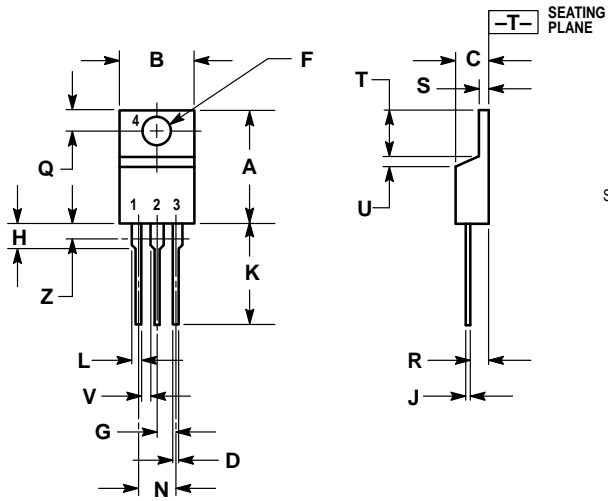
Figure 17. Gate Charge versus Gate-To-Source Voltage



$V_{in} = 15\text{ V}_{pk}$; PULSE WIDTH $\leq 100\ \mu\text{s}$, DUTY CYCLE $\leq 10\%$

Figure 18. Gate Charge Test Circuit

PACKAGE DIMENSIONS




STYLE 5:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-06
 ISSUE Y

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