

Halogens free devices



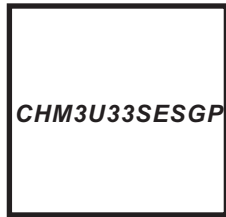
CHENMKO ENTERPRISE CO.,LTD

SURFACE MOUNT

Dual Enhancement Mode Field Effect Transistor

N-channel: VOLTAGE 20 Volts CURRENT 0.2 Ampere

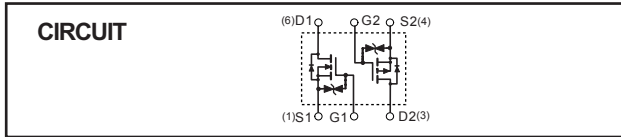
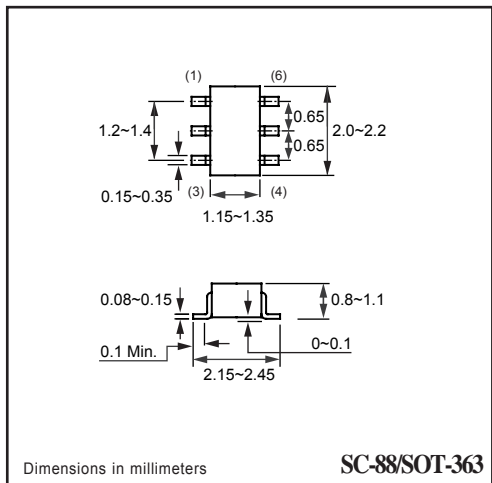
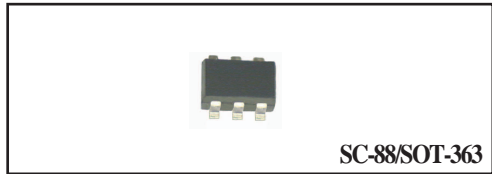
P-channel: VOLTAGE 20 Volts CURRENT 0.2 Ampere



APPLICATION
 * High speed switching , Analog switching

FEATURE
 * Small flat package. (SC-88/SOT-363)
 * Super high dense cell design for extremely low $R_{DS(ON)}$.
 * Lead free product is acquired.
 * High power and current handing capability.
 * ESD protect in input gate 2KV

CONSTRUCTION
 * N-Channel & P-Channel Enhancement in the package



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	20	-20	V
V_{GSS}	Gate-Source Voltage	± 8	± 8	V
I_D	Maximum Drain Current - Continuous	200	-200	mA
	- Pulsed (Note 1)	400	-400	
P_D	Maximum Power Dissipation	150		mW
T_J	Operating Temperature Range	-55 to 150		$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$

Note : 1. $P_w \leq 10\mu\text{s}$, Duty cycle $\leq 1\%$
 2. Pulse Test , Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 3. Repetitive Rating , Pulse width limited by maximum junction temperature
 4. Guaranteed by design , not subject to production testing

ELECTRICAL CHARACTERISTIC (CHM3U33SESGP)

N-Channel Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

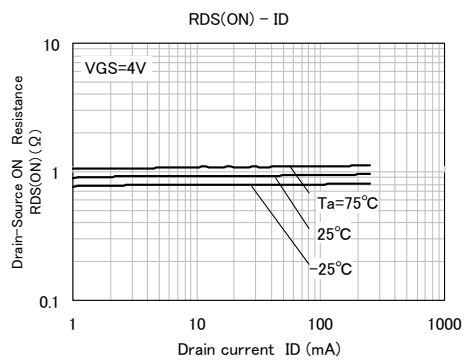
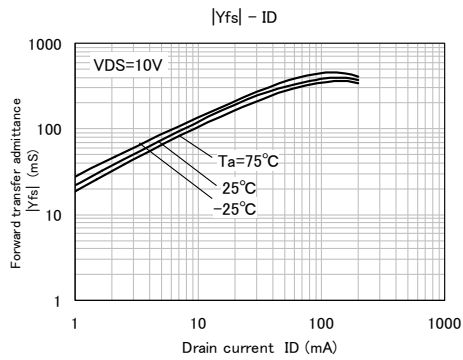
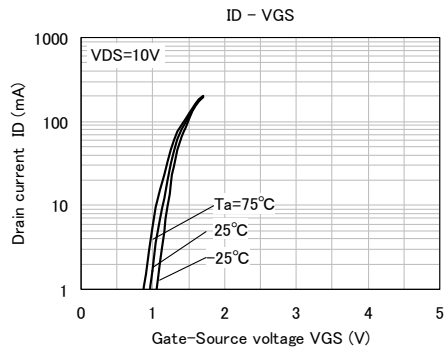
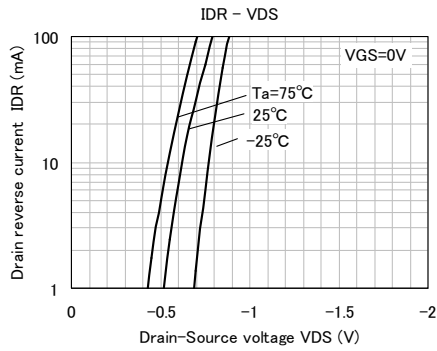
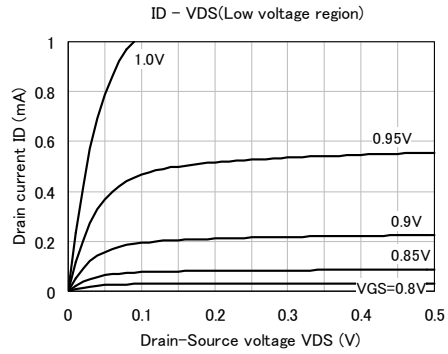
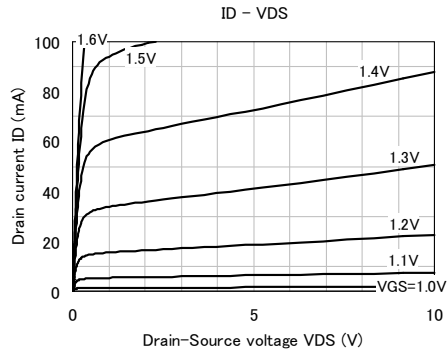
SYMBOL	Parameter	Test conditions				Unit
			Min	Typ	Max	
V(BR)DSS	Drain-source breakdown voltage	$I_D=100\mu\text{A}$, $V_{GS}=0\text{V}$	20	-	-	V
IGSS	Gate-source leak current	$V_{GS}=\pm 5\text{V}$, $V_{DS}=0\text{V}$	-	-	± 0.5	μA
IDSS	Zero gate voltage drain current	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$	-	-	1.0	μA
V _{th}	Gate threshold voltage	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	0.6	-	1.2	V
Y _{fs}	Forward transfer admittance	$V_{DS}=10\text{V}$, $I_D=0.1\text{A}$	-	300	-	mS
RDS(ON)	Static drain-source on-state resistance	$I_D=100\text{mA}$, $V_{GS}=4.0\text{V}$	-	0.9	-	Ω
C _{iss}	Input capacitance	$V_{DS}=10\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	34	-	pF
C _{oss}	Output capacitance		-	8.5	-	
t _{on}	Switching time	$V_{DD}=5\text{V}$, $I_D=10\text{mA}$	-	14	-	ns
t _{off}		$V_{GS}=0\sim 5\text{V}$	-	85	-	

P-Channel Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

SYMBOL	Parameter	Test conditions				Unit
			Min	Typ	Max	
V(BR)DSS	Drain-source breakdown voltage	$I_D=-100\mu\text{A}$, $V_{GS}=0\text{V}$	-20	-	-	V
IGSS	Gate-source leak current	$V_{GS}=\pm 5\text{V}$, $V_{DS}=0\text{V}$	-	-	± 0.5	μA
IDSS	Zero gate voltage drain current	$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$	-	-	-1.0	μA
V _{th}	Gate threshold voltage	$I_D=-250\mu\text{A}$, $V_{DS}=V_{GS}$	-0.6	-	-1.2	V
Y _{fs}	Forward transfer admittance	$V_{DS}=-10\text{V}$, $I_D=-0.1\text{A}$	-	280	-	mS
RDS(ON)	Static drain-source on-state resistance	$I_D=-100\text{mA}$, $V_{GS}=-4.0\text{V}$	-	2.0	-	Ω
C _{iss}	Input capacitance	$V_{DS}=-10\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	37	-	pF
C _{oss}	Output capacitance		-	12	-	
t _{on}	Switching time	$V_{DD}=-5\text{V}$, $I_D=-10\text{mA}$	-	16	-	ns
t _{off}		$V_{GS}=0\sim -5\text{V}$	-	110	-	

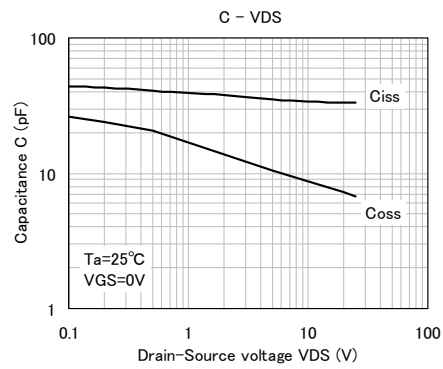
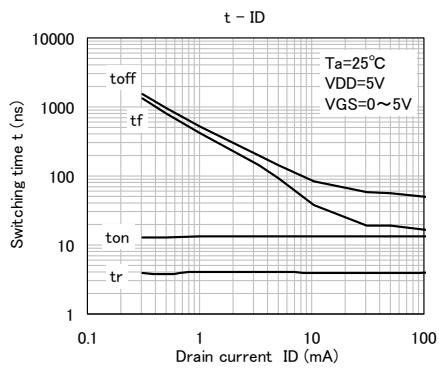
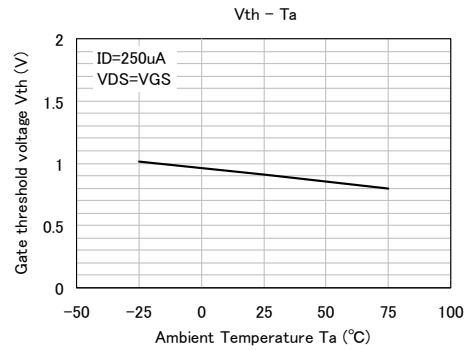
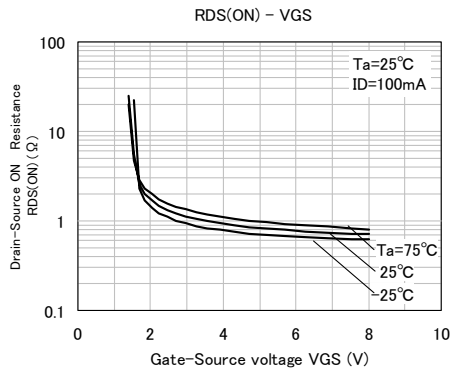
RATING CHARACTERISTIC CURVES (CHM3U33SESGP)

N-MOSFET Typical Electrical Characteristics

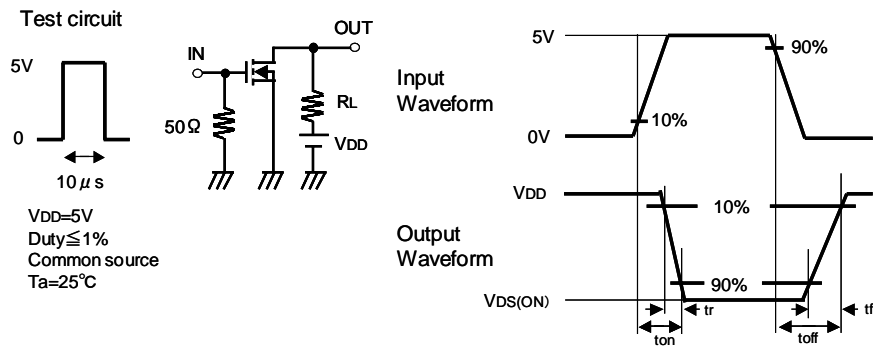


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N-MOSFET Typical Electrical Characteristics

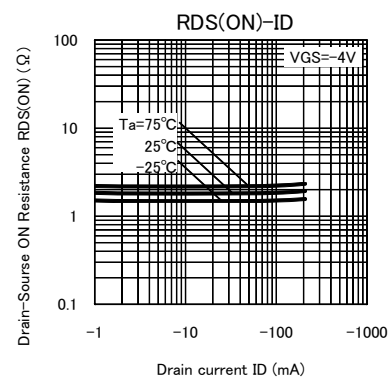
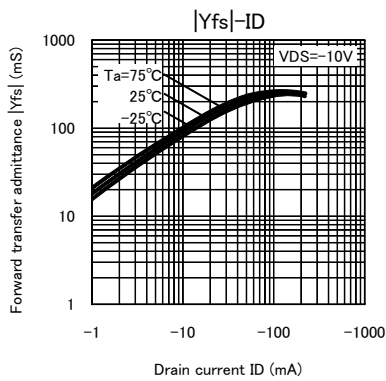
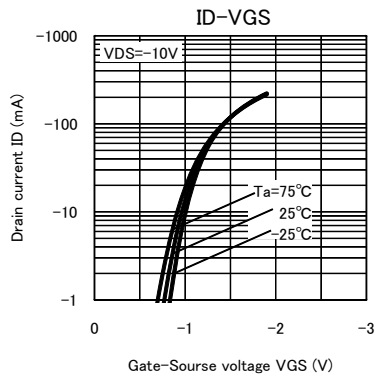
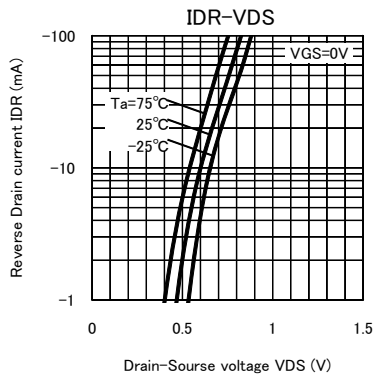
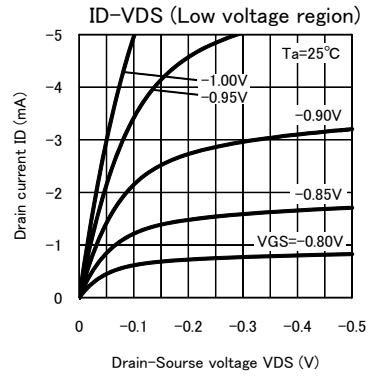
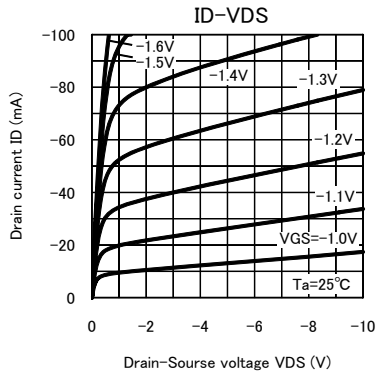


Switching time test condition



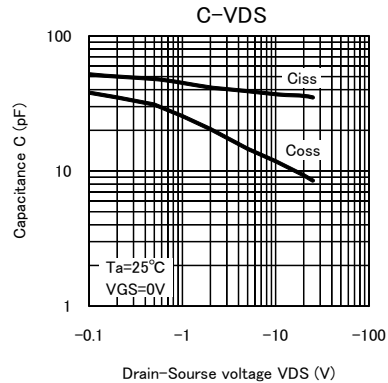
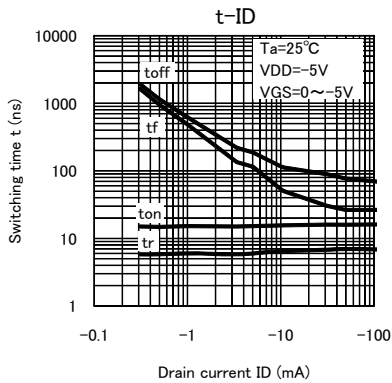
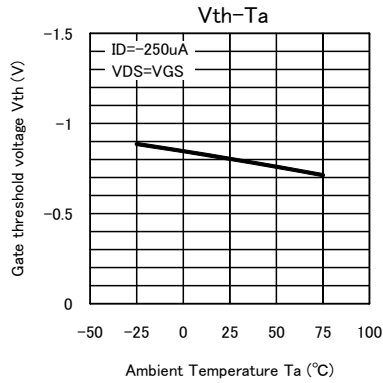
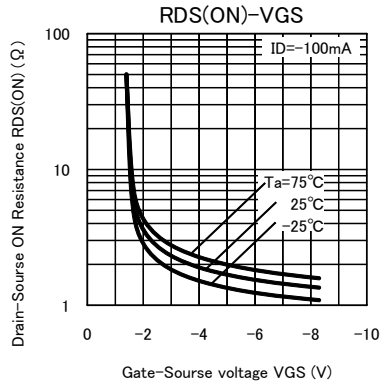
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P-MOSFET Typical Electrical Characteristics



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Switching time test condition

